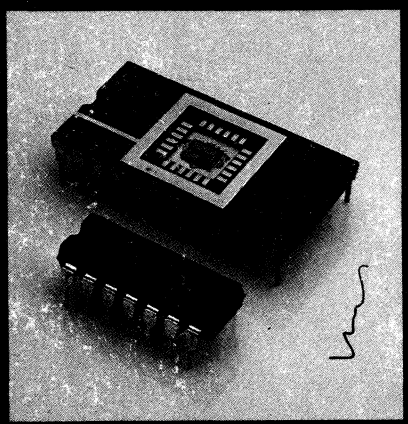


Integrated Circuits

ANALOG DEVICES

How to Find Product Data in This Databook

The Databook contains Data Sheets for all products recommended for new designs, lists of Available Products not databooked here (data sheets upon request), and a Substitution Guide for products no longer available, plus Selection Guides and a wealth of background information.

THERE ARE TWO VOLUMES

VOLUME I contains technical data on our *integrated circuits and hybrids* for data acquisition.
VOLUME II has all data-acquisition products manufactured in the form of *modules, cards, instruments, discrete-assembly subsystems and systems.*

DO YOU KNOW THE MODEL NUMBER?

If you know the model number, turn to the product index on page 1-14 (back of book) and look up the model number. You will find the Volume, Section, and Page location of data sheets bound into Volume I and Volume II.

If you're looking for a form-and-function-compatible version of an integrated circuit or hybrid product originally brought to market by some other manufacturer (second source), add our "AD" prefix (or "ADSP", for digital signal processing ICs) and look it up in the index.

IF YOU DON'T KNOW THE MODEL NUMBER

There are two ways to find a device to perform your function:

1. **FIND YOUR FUNCTION IN THE LIST ON THE OPPOSITE PAGE OR ON PAGE 2–1**
   Turn directly to the appropriate Section (or Volume). You will find one or more functional Selection Guides at the beginning of the Section. The Selection Guides will help you find the products that are closest to satisfying your need, and their Volume-Section-Page locations. Use them to compare all products in the category by salient criteria, no matter which Volume their technical data resides in.

2. **IF THE FUNCTION IS NOT LISTED BY A NAME THAT YOU RECOGNIZE**
   Find it in the diagram (opposite page). It will help you find the Selection Guides for products in that functional category. Then use the Selection Guide(s) to find the Volume-Section-Page locations of products that will come closest to satisfying your need.

A RELATED PRODUCT MAY BE WHAT YOU REALLY WANT

Text in each section often mentions related or complementary product categories having a greater or lesser degree of functional integration.

IF YOU CAN'T FIND IT HERE . . . ASK!

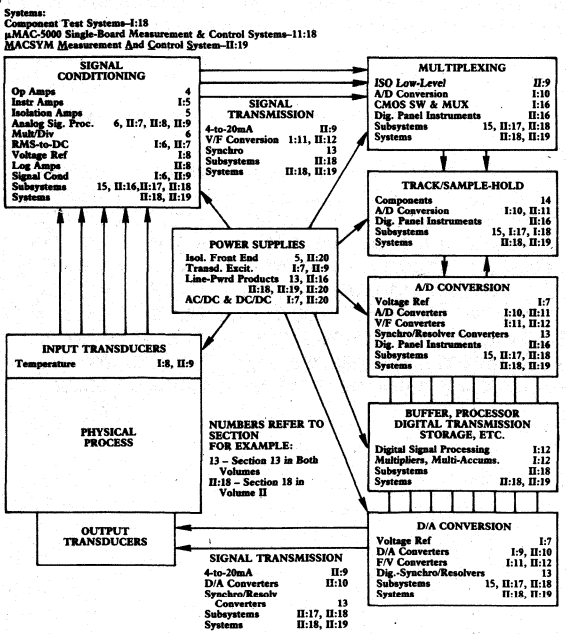
See Worldwide Service Directory, 1–12 and 1–13, at the back of this volume.

ANALOG DEVICES

DATA-ACQUISITION DATABOOK 1984

VOLUME I
INTEGRATED CIRCUITS

PICTORIAL GUIDE TO PRODUCT CATEGORIES



DATA-ACQUISITION DATABOOK 1984

VOLUME I
INTEGRATED CIRCUITS

Products in this book may be covered by one or more of the following patents. Additional patents are pending. See individual data sheets for further information:

U.S.: 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,747,088, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,872,466, 3,887,863, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,270,118, 4,268,759, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,338,591, 4,349,811, 4,363,024, 4,374,314, 4,383,222, 4,395,647, 4,399, 345, 4,400,689, 4,400,690, DES 233,909. U.K.: 964,513, 1,310,591, 1,310,592, 1,364,233, 1,470,673, 1,470,674, 1,537,542, 1,531,931, 1,571,869, 1,590,136, 1,590,137, 1,599,538, 2,008,876, 2,012,135, 2,032,659, 2,040,087, 2,050,740, 2,081,040. France: 70.10561, 71.28952, 74.25263, 75-27557, 76 01788, 76 08238, 77 20799, 79 24021, 80 00960, 111 833. West Germany: 20 14 034, 21 39 560, MR 9379. Italy: 933,798. Japan: 452,263, 1,092,928, 1,101,824, 1,180,463. Canada: 984,015, 1,006,236, 1,025,558, 1,035,464, 1,054,248, 1,141,034, 1,141,820, 1,143,306, 1,150,414, 1,153,607, 1,157,571. Sweden: 7603320-8.

Contents

General Introduction

Analog Devices designs, manufactures, and sells worldwide sophisticated electronic components and subsystems for use in precision measurement and control. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including bipolar, I^2L, CMOS, and hybrid integrated circuits–and assembled products in the form of potted modules, printed-circuit boards, and instrument packages.

State-of-the-art technologies have been utilized (and, in many cases, invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Nearly twenty years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens the leadership position of Analog Devices in data-acquisition products.

MAJOR PROGRESS

Since the publication of our two-volume *1982 Databook* and its 1983 companion update volume, nearly 50 significant new products have been introduced. They are identified by bullets (•) in the index and in the table of contents for each section of this Databook. Examples of these new products include: The AD7226 Quad DAC – 4 bus-interfaced voltage-output 8-bit DACs on a single monolithic CMOS chip; the AD670 8-bit "ADCPORT," a complete ready-to-go monolithic μP-compatible 8-bit a/d converter with on-chip instrumentation amplifier; the AD667 complete 12-bit voltage-output D/A converter with 2μs voltage-settling time; the AD9700 monolithic DAC for raster displays; the ADSP-1110 single-port 16-bit multiplier/accumulator for digital signal-processing; and the complete, expandable, stand-alone μMAC-5000 single-board measurement-and-control system, programmable in powerful μMACBASIC.

INTEGRATED CIRCUITS

The list of product-category "bleed tabs" opposite the "How to Find It" Guides on the inside front cover of this Volume is a functional summary of our integrated-circuit and hybrid component and subsystem product classes. The complete table of contents, starting on page 2-1, provides a detailed panorama of products and functions, irrespective of technology, appearing in both Volumes of this Databook.

TECHNICAL SUPPORT

Analog Devices offers extensive technical literature, which discusses the technology and applications of products for precision measurement and control. Besides comprehensive data sheets, of which there are many outstanding examples in this book, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several serial publications; for example, *Analog Productlog*, which provides brief information on new component products being introduced and *Analog Dialogue*, our technical magazine, which provides-in-depth discussions of new developments in analog and digital circuit technology as applied to data-acquisition and control. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to data-book catalogs–such as this one–we also publish several short-form catalogs, on specific product families. You will find typical publications described on page 1-11 at the back of the book.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory appears on pages 1-12 and 1-13 at the back of the book.

PRODUCTS NOT CATALOGUED HERE

For maximum usefulness to designers of new equipment, without unwieldy size, we have limited the contents of the Databook to products most likely to be used for the design of new circuits and systems. If the data sheet for a product you are interested in is not in either Volume turn to page 1-9, at the back of this book, where you will find a list of older products for which data sheets are available upon request. On page 1-10 you will find a guide to substitutions for products no longer available.

PRICES

At Analog Devices, we recognize that accurate, up-to-date prices of our products are an important consideration in making a choice among the many available product families. However, since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

(this section continues at the back of the book)

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Operational Amplifiers – Section 4

•New product since publication of *1982 – 1983 Databook Update.*

Instrumentation & Isolation Amplifiers – Section 5

Analog Signal Processing Components – Section 6

•New product since publication of *1982–1983 Databook Update*.

Voltage References – Section 7

Temperature Measurement Components – Section 8

•New product since publication of *1982–1983 Databook Update*.

Digital-to-Analog Converters – Section 9

LOGDAC is a registered trademark of Analog Devices, Inc.

•New product since publication of *1982–1983 Databook Update*.

Digital-to-Analog Converters – Section 9 (continued)

Analog-to-Digital Converters – Section 10

•New product since publication of *1982–1983 Databook Update.*

Analog-to-Digital Converters – Section 10 (continued)

Voltage-to-Frequency & Frequency-to-Voltage Converters – Section 11

Digital Signal Processing Components – Section 12

•New product since publication of *1982–1983 Databook Update*.

Synchro & Resolver Converters – Section 13

Sample/Track-Hold Amplifiers – Section 14

Data Acquisition Subsystems – Section 15

•New product since publication of *1982–1983 Databook Update.*
Inductosyn is a registered trademark of Farrand Industries, Inc.

CMOS Switches & Multiplexers – Section 16

Monolithic Chips – Section 17

BIPOLAR INTEGRATED CIRCUIT CHIPS

•New product since publication of *1982–1983 Databook Update*.
DACPORT is a registered trademark of Analog Devices, Inc.

Monolithic Chips – Section 17 (continued)

Component Test Systems – Section 18

Package Information – Section 19

Application Notes – Section 20

•New product since publication of *1982–1983 Databook Update.*

Ordering Guide

Contents

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

Many of the data sheets in the Databook have an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. I.C. and hybrid part numbers are created using one of these two systems:

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3- or 4-digit model number, an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows the somewhat different numbering scheme used by our Computer Labs Division for hybrid circuits. The number starts with a three-character alphabetic prefix, followed by a hyphen, a three- or four-digit number, and alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

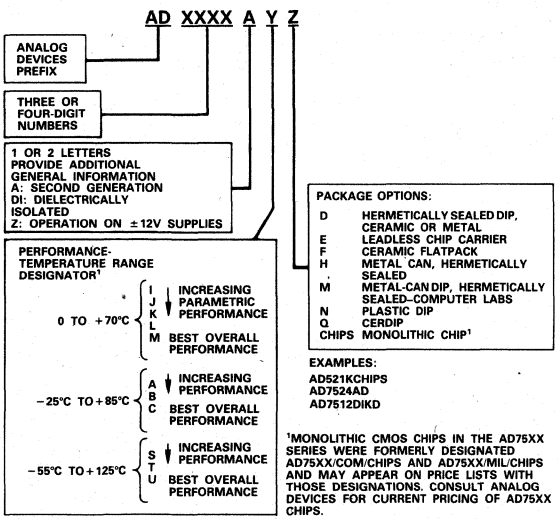

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products

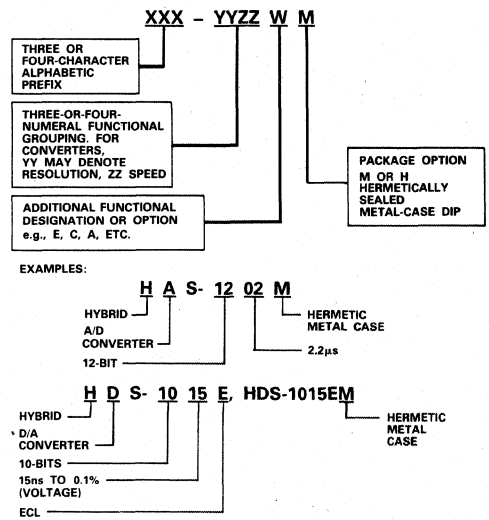

Figure 2. Computer Labs Video Hybrid Product Designations

SECOND SOURCE

In addition to our many proprietary products, we also manufacture devices that are fit-, form-, and function-compatible (and often superior in performance and reliability) to popular products that originated elsewhere. For such products, we add the prefix "AD" to the familiar model number (example: ADDAC85C-CBI-V).

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via TWX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. On all orders under fifty dollars ($50.00), a five-dollar ($5.00) processing charge is required.

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and μMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Operational Amplifiers

Contents

•New product since publication of *1982–1983 Databook Update.*

Selection Guide
Operational Amplifiers

General Purpose

		171	AD503	AD506	AD542	AD642	AD644	AD544	AD611	AD101 Series	AD741
		FET INPUT						WIDEBAND			
Monolithic Technology	Bipolar Input									•	•
	J-FET				•			•	•		
	Dual J-FET					•	•				
Multi-Device Technology	Hybrid		•	•							
	Module	•									
High Open Loop Gain	⩾100dB	•			•	•					
	⩾140dB										
High CMR	>100dB	•									
Low Offset Voltage	⩽5mV			•	•	•	•	•	•	•	•
	⩽1mV	•			•	•	•	•	•		
	⩽50μV										
Low Offset V, vs. Temp	⩽5μV/°C				•	•	•	•			
	⩽1μV/°C										
	⩽0.6μV/°C										
Low Bias Current	⩽50pA	•	•	•	•	•	•	•	•		
	⩽5pA										
	⩽0.5pA										
Fast Settling	⩽1μs to 0.1%						•	•	•		
	⩽5μs to 0.01%						•	•	•		
Wideband (Unity Gain)	⩾2MHz	•					•	•	•	•	
	⩾10MHz										
High Slew Rate	⩾10V/μs	•					•	•	•	•	
	⩾30V/μs										
	⩾100V/μs										
	⩾1000V/μs										
Low Noise (0.1 to 10Hz) 2μV p-p					•	•	•	•	•	•	
High Voltage Out	⩾100V	•									
High Current Out	⩾20mA										
Low Power	⩽75mW				•	•	•	•	•	•	•
Second Source										•	•
Temperature Range 0 to +70°C		•	•	•	•	•	•	•	•	•	•
-25°C to +85°C										•	
-55°C to +125°C			•	•	•	•	•	•	•	•	•
Dice Availability					•	•	•	•			
Volume		II	I	I	I	I	I	I	I	I	I
Page		4-21	4-35	4-35	4-75	4-95	4-99	4-79	4-91	4-17	4-107

Shading indicates new product since publication of *1982–1983 Databook Update*.

High Accuracy

		LOW V_{OS} DRIFT					LOW BIAS CURRENT			FET INPUT				
		AD504	AD510	AD OP-07	AD OP-27	AD OP-37	AD517	234[1]	235[1]	AD545	AD547	AD647	AD515	52
Monolithic Technology	Bipolar Input	•	•	•	•	•	•							
	J-FET										•			
	Dual J-FET											•		
Multi-Device Technology	Hybrid									•			•	
	Module							•	•					•
High Open Loop Gain	⩾100dB	•	•	•	•	•	•	•	•		•	•		•
	⩾140dB							•	•					
High CMR	>100dB	•	•	•	•	•	•							•
Low Offset Voltage	⩽5mV	•	•	•	•	•	•			•			•	•
	⩽1mV										•	•		•
	⩽50μV			•	•	•	•	•	•					
Low Offset V, vs. Temp	⩽5μV/°C	•	•	•	•	•	•			•	•	•		•
	⩽1μV/°C							•	•		•	•		•
	⩽0.6μV/°C	•	•	•	•	•		•	•					
Low Bias Current	⩽50pA								•	•	•	•	•	
	⩽5pA									•			•	•
	⩽0.5pA												•	
Wideband (Unity Gain)	>500kHz								•					
	>2MHz				•	•		•						
High Slew Rate	⩾10V/μs					•								
	⩾30V/μs							•						
	⩾100V/μs													
	⩾1000V/μs													
Low Noise (0.1 to 10Hz)														
⩽4μV p-p											•	•		
⩽2μV p-p			•	•			•		•					•
⩽1μV p-p		•			•	•		•	•					
High Voltage Out	⩾100V													
High Current Out	⩾20mA													
Low Power	⩽75mW									•	•	•	•	
Second Source				•	•	•								
Temperature Range														
0 to +70°C		•	•	•	•	•	•		•	•	•	•	•	•
-25°C to +85°C														
-55°C to +125°C		•	•	•	•	•	•				•	•		
Dice Availability				•			•				•			
Volume		I	I	I	I	I	I	II	II	I	I	I	I	II
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NOTE

[1] Chopper Stabilized

Shading indicates new product since publication of *1982–1983 Databook Update*.

Selection Guide
Operational Amplifiers

Fast/Wideband

		FET INPUT											UNITY GAIN BUFFER	
		AD507	AD509	AD518	AD380	AD381	AD382	AD3554	50, 51	HOS-050	HOS-060	ADLH0032	ADLH0033	HOS-100
Monolithic Technology	Bipolar Input	•	•	•										
	J-FET								•					
	Dual J-FET													
Multi-Device Technology	Hybrid				•	•	•	•		•	•	•	•	•
	Module								•					
High Open Loop Gain	⩾100dB	•				•	•	•		•	•			
	⩾140dB													
High CMR	>100dB													
Low Offset Voltage	⩽5mV	•	•		•		•	•	•			•	•	
	⩽1mV					•					•			
	⩽50μV													
Low Offset V, vs. Temp	⩽5μV/°C					•	•							
	⩽1μV/°C													
	⩽0.6μV/°C													
Low Bias Current	⩽50pA					•	•	•				•	•	
	⩽5pA													
	⩽0.5pA													
Fast Settling	⩽1μs to 0.1%	•	•	•		•	•		•	•	•	•	•	•
	⩽5μs to 0.01%				•			•	•	•	•	•		
Wideband (Unity Gain)	⩾2MHz					•	•							
	⩾10MHz	•	•	•	•			•		•	•	•	•	•
	⩾50MHz								•					
High Slew Rate	⩾10V/μs	•		•										
	⩾30V/μs					•	•							
	⩾100V/μs		•		•				•	•	•	•	•	•
	⩾1000V/μs							•						
Low Noise (0.1 to 10Hz) ⩾2μV p-p						•	•							
High Voltage Out	⩾100V													
High Current Out	⩾20mA	•			•		•	•	•	•	•		•	•
Low Power	⩽75mW													
Second Source		•	•					•				•	•	
Temperature Range														
0 to +70°C		•	•	•	•	•	•		•					
-25°C to +85°C								•				•	•	
-55°C to +125°C		•	•	•	•	•	•	•		•	•	•	•	•
Dice Availability				•										
Volume		I	I	I	I	I	I	I	II	I	I	I	I	I
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Orientation
Operational Amplifiers

The amplifiers listed in this catalog are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more-general requirements in electronic circuits. The technical data included here* cover the properties of some 36 op-amp families, comprising about 100 distinct types. Some are general purpose, others provide near-optimum performance for specific classes of applications.

They differ in a variety of ways, for example, circuit technology, circuit architecture, input properties, output properties, operating temperature range and in terms of the many performance specifications.

BACKGROUND

The operational amplifier is today the most-widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control), and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 4-16 a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. It should come as no surprise to successful users of Analog Devices op amps that a number of the references are to the applications sections of data sheets included in this catalog.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.* Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.

2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.* Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to translate these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels, and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier, or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks", and linear circuit books, as well as in application notes and data sheets.

2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of parameters, and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high-frequency performance and transient behavior of the op-amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist, which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.

3. The designer must then relate acceptable performance of the op-amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows the next section.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier.

*In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, DC offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gain-bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If DC information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and all of the "drift" specifications may usually be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where DC information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

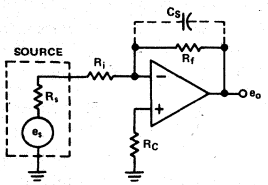
1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_s, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier R_{cm}.

2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy. For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b), and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.



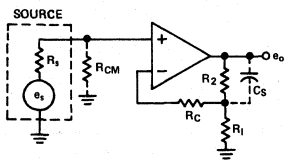
$$e_o = -\frac{R_f}{R_i}\underbrace{\left[e_s + e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i\right]}_{\text{Signal}\quad \text{Input Drift Error} = V_d} \qquad \begin{matrix}\text{For } R_C = 0 \\ \text{and } R_s \ll R_i\end{matrix}$$

$$e_o = -\frac{R_f}{R_i}\underbrace{\left[e_s + e_{os}\frac{R_f + R_i}{R_f} + i_d R_i\right]}_{\text{Signal}\quad \text{Input Drift Error} = V_d} \qquad \begin{matrix}\text{For } R_C = R_i R_f/(R_i + R_f) \\ \text{and } R_s \ll R_i\end{matrix}$$

Input Impedance $R_{IN} \approx R_i$

% Drift Error $= \dfrac{100V_d}{e_s}$

Figure 1A. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\underbrace{\left[e_s + e_{os} + i_b R_s\right]}_{\text{Signal}\quad \text{Drift Error} = V_d} \text{ for } R_C = 0$$

$$e_o = \frac{R_2 + R_i}{R_i}\underbrace{\left[e_s + e_{os} + i_d R_s\right]}_{\text{Signal}\quad \text{Drift Error} = V_d} \text{ for } R_C = R_s - \frac{R_i R_2}{R_i + R_2}$$

Input Impedance $R_{IN} \approx R_{CM}$

% Drift Error $= \dfrac{100V_d}{e_s}$

Figure 1B. Noninverting Configuration

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_S for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

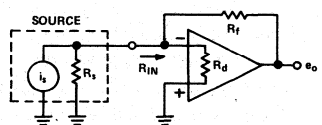
Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from +25°C need be considered. For example, over the range of -25°C to +85°C, the maximum temperature excursion (ΔT) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm},

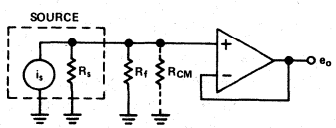


$$e_o = -R_f\underbrace{\left[i_s + e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b\right]}_{\text{Signal}\quad \text{Drift error} = I\epsilon}$$

Input Impedance $R_{IN} = \left(\dfrac{R_f R_d}{R_f + R_d}\right)\left(\dfrac{1}{1 + A\beta}\right)$

where $1/\beta = 1 + \dfrac{R_f (R_s + R_d)}{R_s \quad R_d}$ % Drift Error $= \dfrac{100\, I\epsilon}{i_s}$

Figure 2A. Current Amplifier



$$e_o = \underbrace{R_f i_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_f}_{\text{Drift Error} = V_d} \text{ for } R_s > R_f$$

Input Impedance $R_{IN} \approx R_f$

% Drift Error $= \dfrac{100V_d}{R_f\ i_s}$

Figure 2B. Voltage Amplifier with Sampling Resistor

for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_e referred to the input, use the following expression.

$$\Delta I_e = \left[\frac{\Delta e_{os}}{\Delta T}\left(\frac{R_f + R_s}{R_f R_s}\right) + \frac{\Delta i_B}{\Delta T}\right]\Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_e, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μsec, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm, and stray capacitance, C_S, were one picofarad then the closed loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in turn is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_s will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

For greater emphasis wideband applications can be separated into two categories – steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is DC coupling required?* If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.

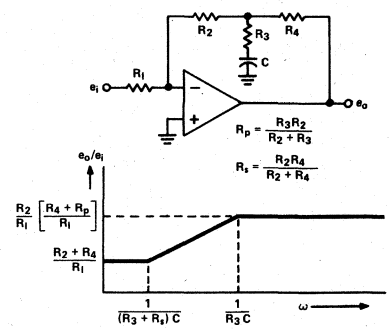


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, $f_{c1}(-3dB)$. For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta$ = A/G). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

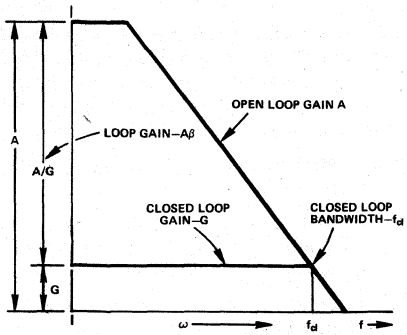


Figure 4. Closed Loop Bandwidth and Loop Gain

a. Closed loop gain stability = $\Delta G/G$
$\Delta G/G = (\Delta A/A)\ [1/(1 + A\beta)]$ where $\Delta A/A$ is the open loop gain stability, usually about 1%/°C.

b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, usually 200 to 5000 ohms.

c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?* You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier.

For some monolithic amplifier designs available today their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

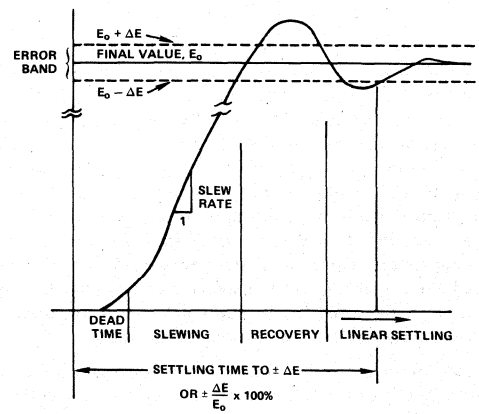


Figure 5. Typical Settling Time Characteristics

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

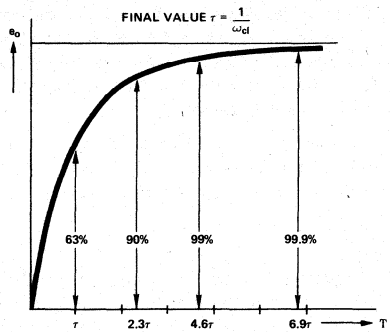


Figure 6. Step Response for Linear 6dB/Octave Amplifier

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:

$e_n = \sqrt{4KTBR}$

where e_n = the rms value of the noise voltage

K = Boltzman's Constant (1.38×10^{-23} joules/°K)

T = absolute temperature of the resistance, °K

B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldy for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

(1) Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n \text{ (rms)} = (40\text{nV}/\sqrt{\text{Hz}})\left(\sqrt{\frac{R}{100\text{k}\Omega}\ (\text{BW})}\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

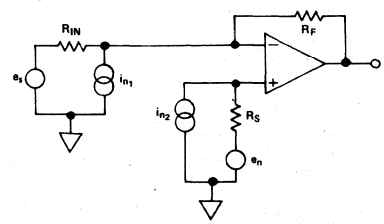
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots\ e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 7A illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a RMS fashion.



COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4KTBR_{IN}}\ (R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4KTBR_S}\ (R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4KTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\ (R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\ (R_F/R_{IN}+1)$

TOTAL NOISE = $\sqrt{(e_{R_{IN}}\ G)^2 + [e_{R_S}\ (G+1)]^2 + e^2{}_{R_F} + (i_{n_1} R_F)^2 + [(i_{n_2} R_S)\ (G+1)]^2 + [e_n\ (G+1)]^2}$

Figure 7A. Noise Components

Figure 7B illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, AD504, or a low noise type amplifier is being used with a 50kΩ source impedance. The two major noise sources, in addition to the AD504M input voltage noise of 0.6μV p-p, are the Johnson noise (58μV p-p) and current noise (2.5μV p-p).

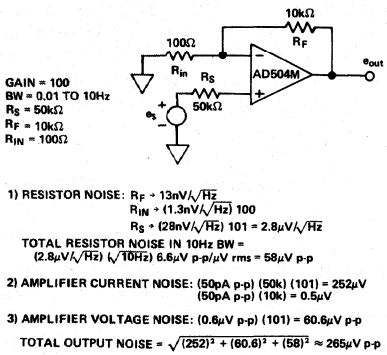


Figure 7B. Design Example

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide, in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations.

Temperature Range and Nomenclature. Analog Devices operational-amplifier nomenclature uses suffixes to permit ready identification of the temperature range for which device operation to meet critical specifications has been designed or selected. The most popular range comprises the "commercial" temperatures from 0 to 70°C; it is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD741L). Also popular is the "extended" range, -55°C to +125°C, designated by S, T, U, (e.g., AD510S); not all families have types with specified performance in this range. There are a few types designed for operation in the "industrial" range, -25°C to +85°C, designated by A, B. Wide-range types will generally meet the same or better specs in a narrower temperature range. A few types are second-sources for products originally introduced by other manufacturers. In those instances, the generic nomenclature is used (AD741C) or enlarged upon, if superior selections are offered (e.g., AD301AL).

1. *General-Purpose ICs.* Amplifiers in this group include our lowest-cost devices. They are best-suited for general purpose designs with moderate drift requirements, down to 5μV/°C max (AD301AL), and gain-bandwidth to 8MHz (AD301A). Typical applications include summing, inverting, impedance buffering (followers), and active filtering. They are also useful for developing nonlinear transfer functions, with appropriate external circuitry.

Bipolar monolithic technology is used for all types. The AD741 is internally compensated; it does not require external capacitance for frequency compensation. On the other hand, the AD301A's ability to be externally compensated, by either lag or feedforward circuitry, permits circuits with a wide range of dynamic performance characteristics to be handled. Extended-temperature-range equivalents are the AD101A, AD201A, and AD741.

2. *Low Bias-Current, High Input-Impedance, FET-Input ICs.* These types use the inherently high impedance and low leakage current of junction field-effect transistors (FET's) to deal with configurations that either provide the measurement of low currents or require the use of high-resistance circuitry.

Typical applications range from general-purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to measurements with high-impedance transducers, such as photomultipliers, flame detectors, pH cells, and radiation detectors.

The performance range is from the 75fA (75 x 10^{-15} A) maximum bias current of the AD515L electrometer to the 100pA max of the general purpose, lowest-cost AD611. The AD542 is a low-cost, laser-wafer-trimmed (LWT) monolithic implanted FET input amplifier with low offset and drift. The AD544 is similar, but has higher speed. Low bias current does not necessarily imply large voltage offsets; the AD515K combines a 150fA (0.15pA) max bias current with 1.0mV max offset and 15μV/°C max voltage drift; comparable figures for the AD547L are 25pA, 0.25mV and 1μV/°C.

The types of amplifiers in this group either are completely monolithic or employ matched FET's and a special bipolar amplifier chip designed to accommodate the input FET's electrically. In nearly all the IC's, thin-film resistors are deposited on the chip at critical circuit locations to ensure stability; low offsets and drift are achieved by laser-trimming of circuit balance. All FET-input op amps from Analog Devices are manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmed-up bias current). Our published max bias-current specification applies to either input (some manufacturers call "bias current" the *average* of the two input currents). Bias current of junction FET's approximately doubles for every 10°C increase of temperature.

3. *FET-Input Dual ICs.* The AD642, AD644, and AD647 are a single-chip pair of trimmed implanted-FET-input (TRIFET) op amps similar to the AD542, AD644, and AD547 with low warmed-up bias current (35pA max – K, L, S), low offset voltage (0.5mV max – L), low offset-voltage drift (2.5μV/°C max – L), and excellent V_{os} matching (0.25mV max – L). Besides applications calling for more than one FET-input op amp at low cost per function, the AD647 is especially useful

in applications calling for matched duals, such as log-ratio amplifiers, FET-input instrumentation amplifiers, and buffering of differential signals. The AD644, a wideband version, was designed for fast DAC amplifiers, sample and hold, filters and wideband instrument amplifiers.

4. *Electrometers.* This class comprises the lowest bias-current devices, the AD515. The AD515L, with its 75fA input bias current, 1mV max offset, and 25μV/°C offset tempco, has differential inputs, and can be used in voltage measurements at high impedance, as a follower, or in current measurements, as an inverter, or even differentially.

5. *High-Accuracy Low-Drift Differential-Input ICs.* "Chopperless" low-drift designs with differential inputs, optimized for voltage offset and drift, dc open-loop gain, and CMR, should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators, and for impedance buffer designs.

Performance of internally compensated premium amplifiers in this group ranges from the ADOP-07A's 25μV max offset voltage and 0.6μV/°C drift, and the AD517L's 50μV max offset voltage and 1.3μV/°C drift, combined with 1nA max bias current (1.5nA max over the temperature range), and CMR of 110dB min, to the low-cost AD741L's maximum offset of 0.5mV and max offset tempco of 5μV/°C, with 100nA max bias current over the temperature range, and CMR of 90dB min.

The ADOP-07 is a superior second source to other OP-07 families; for example, ADOP-07AH has minimum gain of 3×10^6 V/V compared to 3×10^5 V/V.

Among *uncompensated* op amps, the premium range is from the AD OP-27 with 25μV maximum offset voltage, 0.6μV/°C max drift, 40nA max bias current over the temperature range, and 114dB CMR, to the low-cost AD301AL, with max offset of 0.5mV, max drift of 5μV/°C, max bias current of 45nA over the temperature range, and minimum CMR of 90dB. For applications in which low noise is essential, the AD OP-27 has 100%-tested guaranteed maximum voltage noise of 0.18μV p-p, for the frequency range 0.1 to 10Hz, and maximum spot noise of 5.5 and 3.8V/$\sqrt{\text{Hz}}$ and 4.0 and 0.6pA/$\sqrt{\text{Hz}}$, at 10Hz, and 1000Hz, respectively.

The AD741J/K/L and the AD301AL are selected from production lots of the generic AD741 and AD101A types. The AD504, AD510, and AD517 are thermally balanced for low drift and high gain (independent of output loading), with inputs that are bootstrapped for high CMR and protected against overloads to prevent bias-current degradation due to reverse breakdown. Thin-film resistors, deposited on the chip, are another key to the stability of these amplifiers. The AD510 and the AD517 employ super-beta input transistors to achieve low bias current, and they are laser-trimmed at the wafer-probe stage (LWT) to achieve their excellent offset-voltage specifications at low cost. Since the bias currents are always of one polarity, they can be nulled at a given temperature with simple circuitry; and the change over the temperature range will be considerably less than for low-cost FET-input amplifiers having comparable specifications.

Extended-temperature-range equivalents are AD504S, AD510S, AD714S, and AD517S.

6. Wide Bandwidth, Fast-Settling ICs. High-speed op amps are characterized by high slewing rates, fast settling time, and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data, in buffers, d/a converters, and multiplexer circuitry; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimal distortion, since the large-signal bandwidth is closely related to the slewing rate.

The products in this category with outstanding specifications are models HOS-050, AD3554 and AD380. Settling of the hybrid HOS-050 is to within 0.01% in 300ns in the inverting connection. Model AD3554 max slewing rate is 1000V/μs inverting, and small-signal unity-gain bandwidth is 70MHz; full-power bandwidth is 16MHz, min. In addition, all of these devices will deliver ±100mA of output current at ±10V, an important factor in video and line-driver circuitry, and in driving capacitive loads. For example, the current required to sustain 500V/μs in a 100pF load is I = C dV/dt = 50mA. AD380 is optimized for settling time: 250ns maximum to 0.01%, inverting or noninverting, with output of ±50mA at ±10V.

There are three families of monolithic ICs listed in this category, with slewing rates ranging from 25V/μs min to 100V/μs min. The AD509S is the fastest slewing (100V/μs min) and settling (500ns min to 0.1% and 2.5μs min to 0.01%). The AD507K is the best all-around performer, with small-signal bandwidth of 35MHz, slewing rate of 25V/μs min, and typical settling to 0.1% within 900ns, in addition to open-loop dc gain of 10^5 min, drift of 15μV/°C max, and bias current of 15nA max. The AD518J is the lowest in cost, yet it slews at 50V/μs min, and typically settles to within 0.1% in 800ns, with single-capacitor compensation.

Extended-temperature-range equivalents are models AD507S, AD509S and AD518S.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage
Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, in some applications, such as voltage comparators, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection
An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is often expressed logarithmically: CMR (in dB) = 20 $\log_{10}$ (CMRR).

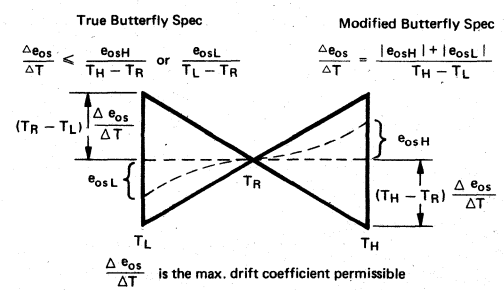
The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified (on the other hand, the incremental CMR may be less in the neightborhood of large CMV). Published CMR specifications for op amps pertain to very low-frequency voltages, unless specified otherwise; CMR decreased with increasing frequency.

Common-Mode Voltage, Maximum
For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connection.

Drift vs. Supply
Offset voltage, bias current, and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature
Offset voltage, bias current, and difference current all change, or "drift", from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature ranges); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more-) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drifts in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less



than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").

The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time
Offset voltage, bias current, and difference current change with time as components age. It is important to realize that drift with time is random, and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift for a chopper-stabilized amplifier might be quoted at 1μV/day, whereas cumulative drift over 30 days might not exceed 5μV, or 15μV in a year (e.g., model 235). A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response
The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a

sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. There is no industry-wide accepted value for the distortion level which determines the full-linear-response limitation, but we use 3% as a maximum acceptable limit for modules.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more-serious effect (often overlooked) is an effect equivalent to a dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often if interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current

Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average.* For single-ended amplifiers (i.e., chopper types), bias current refers to the current at the input terminal.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature* (some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" spec used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current

Difference current is defined as the difference between the bias currents at the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

Input Impedance

Differential input impedance is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the non-inverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage

Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise

Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. The primary difference is that, when evaluating noise performance, bandwidth must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise", resistor noise, or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some types, spectral-density plots or "spot noise", at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain

Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response.*

Overload Recovery

Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output

Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate

The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response

Unity-gain small-signal response is the frequency at which the open-loop gain falls to 1V/V, or 0dB under a specified compensation condition. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification. For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and non-inverting configurations. However, if feedforward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

A BRIEF BIBLIOGRAPHY ON OP AMPS

BOOKS (Not available from Analog Devices except where noted)

IC Op-Amp Cookbook by Walter Jung, Howard Sams & Co., Second Edition, 1980, down-to-earth and practical paperback

Linear Integrated Circuit Applications by George B. Clayton, The Macmillan Press Ltd., London, 1975

Modern Operational Circuit Design, by J. I. Smith, John Wiley & Sons, Inc., 1971

Nonlinear Circuits Handbook, edited by D. H. Sheingold. 1976. $5.95. Analog Devices, Box 796, Norwood, MA 02062

Operational Amplifiers and Linear IC's, by R. F. Coughlin and F. F. Driscoll, Prentice-Hall, Second Edition, 1982. Practical textbook

Operational Amplifiers, Theory and Practice, by J. K. Roberge, J. Wiley & Sons, 1975. Authoritative book on op amp principles and circuitry; contains extensive material on compensation to optimize dynamic performance

Transducer Interfacing Handbook, edited by D. H. Sheingold. 1980. $14.50. Analog Devices, Box 796, Norwood, MA 02062

ARTICLES AND APPLICATION NOTES (Available Upon Request; ask for specific issue of Analog Dialogue)

"Analog Signal Handling for High Speed and Accuracy" by A. P. Brokaw, ANALOG DIALOGUE 11-2

"Current Inverter with Wide Dynamic Range" by Barrie Gilbert, ANALOG DIALOGUE 9-1, 1975

"How to Select Operational Amplifiers", Application Note Section 20 of Volume I

"An IC-Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. P. Brokaw, Application Note Section 20 of Volume I

"Laser-Trimming on the Wafer, A Powerful New Tool for IC's" by R. Wagner, ANALOG DIALOGUE 9-3, 1975

"Simple Rules for Choosing Resistance Values in Adder-Subtractor Circuits" by D. Sheingold, ANALOG DIALOGUE 10-1, 1976

"Specifying and Measuring a Low-Noise FET-Input IC Op Amp" by Bill Maxwell, ANALOG DIALOGUE 8-2, 1974

"How to Test Operational Amplifier Parameters", Application Note Section 20 of Volume I

USEFUL TUTORIAL MATERIAL IN DATA SHEETS

Electrometer Circuitry, see AD515

High-Speed Amplifiers, see AD518 and Models 50/51

Low-Drift Differential Op Amp Performance, see AD504

Low-Level Applications of Chopper-Stabilized Amplifiers:
Inverting, see Models 234, 235
Non-Inverting, see Model 261

ANALOG DEVICES

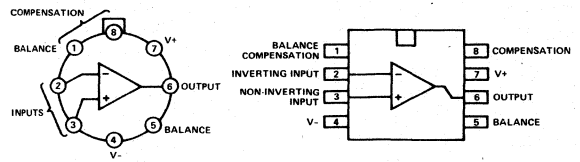
General Purpose Low Cost IC Operational Amplifier

AD101A, AD201A, AD301A, AD301AL

FEATURES

- **Low Bias and Offset Current**
- **Single Capacitor External Compensation for Operating Flexibility**
- **Nullable Offset Voltage**
- **No Latch-Up**
- **Fully Short Circuit Protected**
- **Wide Operating Voltage Range**

AD101 SERIES FUNCTIONAL BLOCK DIAGRAMS



TO-99 **MINI DIP**

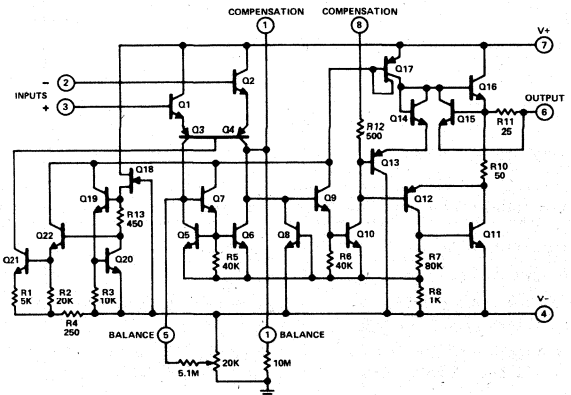
TOP VIEW

GENERAL DESCRIPTION

The Analog Devices AD101A, AD201A, AD301A and AD301AL are high performance monolithic operational amplifiers. All the circuits feature full short circuit protection, external offset voltage nulling, wide operating voltage range, and the total absence or "latch-up". Because frequency compensation is performed externally with a single capacitor (30pF maximum), the AD101A, AD201A, AD301A and AD301AL provide greater flexibility than internally compensated amplifiers since the degree of compensation can be fitted to the specific system application.

The AD101A and AD201A have identical specifications in the TO-99 package; the former guaranteed over the -55°C to +125°C temperature range, and the latter over -25°C to +85°C. The AD201A is also available in the mini-DIP package for high performance operation over the 0 to +70°C temperature range. The AD301A is specified for operation over the 0 to +70°C temperature range in both the TO-99 and mini-DIP packages. The AD301AL is the highest accuracy version of this series. Improved processing and additional electrical testing allow the user to achieve precision performance at low cost. The device provides substantially increased accuracy by reducing errors due to offset voltage (0.5mV max), offset voltage drift (5.0μV/°C max), bias current (30nA max), offset current (5nA max), voltage gain (80,000 min), PSRR (90dB min), and CMRR (90dB min). The AD301AL is also specified from 0 to +70°C and is available in the TO-99 can or 8-pin mini-DIP.

SCHEMATIC DIAGRAM



SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

ABSOLUTE MAXIMUM RATINGS	AD101A, AD201A, AD301A, AD301AL unless otherwise specified
Supply Voltage	
AD101A, AD201A	±22V
AD301A, AD301AL	±18V
Power Dissipation[1]	
TO-99 (Metal Can)	500mW
Dual In-Line (Mini-DIP)	500mW
Differential Input Voltage	±30V
Input Voltage[2]	±15V
Output Short Circuit Duration[3]	Indefinite
Operating Temperature Range	
AD101A	−55°C to +125°C
AD201A (TO-99)	−25°C to +85°C
AD201A (Mini-DIP)	0 to +70°C
AD301A, AD301AL	0 to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)[4]

		AD101A/AD201A			AD301A			AD301AL			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage	$R_S \leq 50k\Omega$		0.7	2.0		2.0	7.5		0.3	0.5	mV
Input Offset Current			1.5	10		3	50		3	5	nA
Input Biz											
Input Bias Current			30	75		70	250		15	30	nA
Input Resistance		1.5	4		0.5	2		1.5	4		MΩ
Supply Current	V_S = ±20V		1.8	3.0							mA
	V_S = ±15V					1.8	3.0		1.8	3	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	50	160		25	160		80	300		V/m
The Following Specifications Apply Over the Operating Temperature Ranges[4]											
Input Offset Voltage	$R_S \leq 10k\Omega$			3.0			10		0.5	1	mV
Input Offset Current				20			70		5	10	nA
Average Temp. Coefficient of Input Offset Voltage	$T_A(min) \leq T_A \leq T_A(max)$		3.0	15		6.0	30		2	5	μV/
Average Temp. Coefficient of Input Offset Current	+25°C $\leq T_A \leq T_A$(max)		0.01	0.1		0.01	0.3		0.01	0.1	nA/
	T_A (min) $\leq T_A \leq$ +25°C		0.02	0.2		0.02	0.6		0.01	0.1	nA/
Input Bias Current				100			300		30	45	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	25			15			40	100		V/m
Input Voltage Range	V_S = ±20V	±15									V
	V_S = ±15V				±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	90		90	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	96		90	100		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±14		±12	±14		±12	±14		V
	V_S = ±15V, R_L = 2kΩ	±10	±13		±10	±13		±10	±13		V
Supply Current	$T_A = T_A$(max), V_S = ±20V		1.2	2.5					1.8	3	mA

NOTES

[1] The maximum desirable junction temperature of the AD101A is +150°C; that of the AD201A, AD301A and AD301AL is +100°C. For operating at elevated temperatures, devices must be derated based upon a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. The thermal resistance of the Dual In-Line package is +160°C/W, junction to ambient.

[2] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

[3] For the AD301A and AD301AL continuous short circuit is allowed for case temperatures to +70°C and ambient temperatures to +55°C.

[4] Unless otherwise specified, these specifications apply for supply voltages and ambient temperatures of ±5V to ±20V and −55°C to +125°C for the AD101A, ±5V to ±20V and −25°C to +85°C for the AD201AH (0 to +70°C for the AD201AN), and ±5V to ±15V and 0 to +70°C for the AD301A and AD301AL.

Specifications subject to change without notice.

ORDERING GUIDE

MODEL	TEMP RANGE	ORDER NUMBER*	PACKAGE OPTION**
AD301AL	0 to +70°C	AD301AL	TO-99, N8A
AD201A	−25°C to +85°C	AD201A	TO-99, N8A
AD301A	0 to +70°C	AD301A	TO-99, N8A
AD101A	−55°C to +125°C	AD101AH	TO-99

*Add package type leter: H = TO-99, N = Mini DIP.
**See Section 19 for package outline information.

FREQUENCY COMPENSATION CIRCUITS

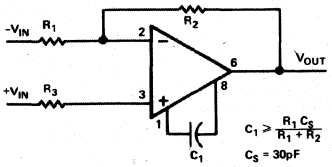


Figure 1. Single Pole Compensation

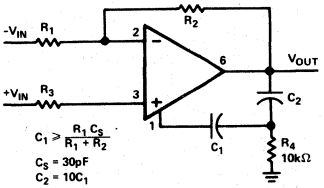


Figure 2. Two Pole Compensation

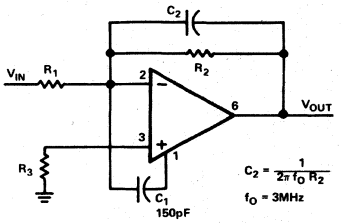
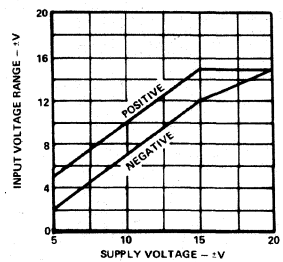
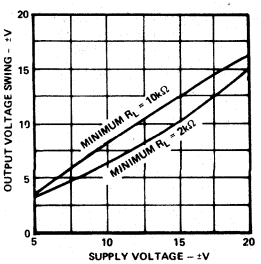


Figure 3. Feedforward Compensation

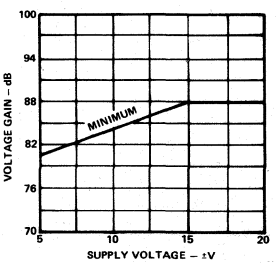
GUARANTEED PERFORMANCE CURVES (Curves apply over the Operating Temperature Ranges)



Input Voltage Range

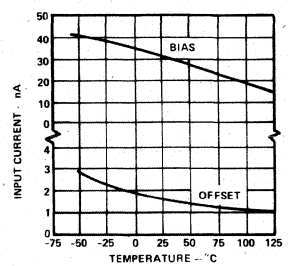


Output Swing

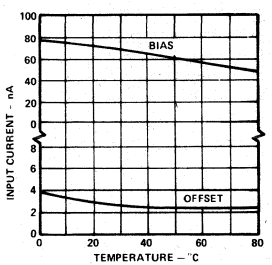


Voltage Gain

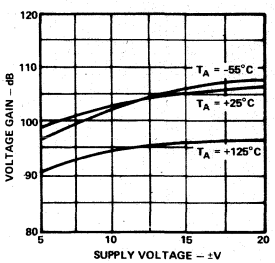
TYPICAL PERFORMANCE CURVES[4]



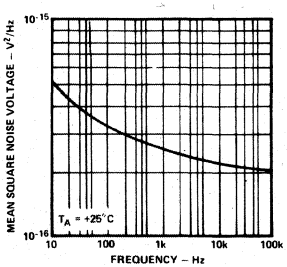
Input Current AD101A, AD201A



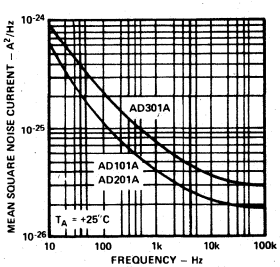
Input Current – AD301A



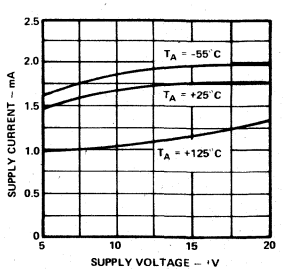
Voltage Gain



Input Noise Voltage

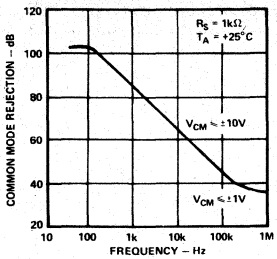


Input Noise Current

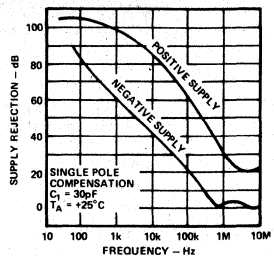


Supply Current

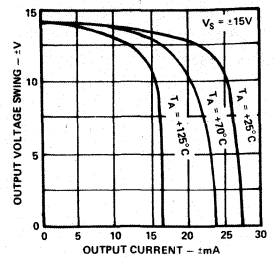
TYPICAL PERFORMANCE CURVES



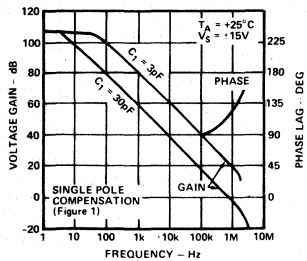
Common Mode Rejection



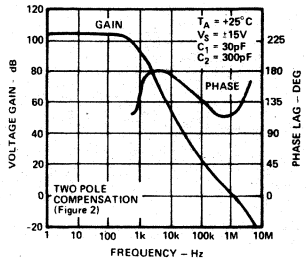
Power Supply Rejection



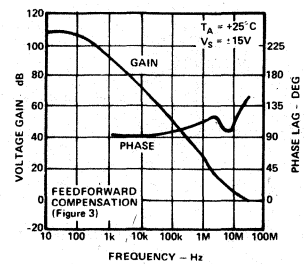
Current Limiting



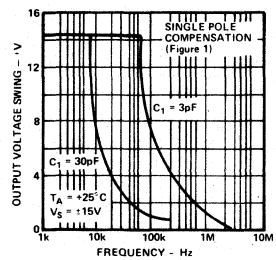
Open Loop Frequency Response



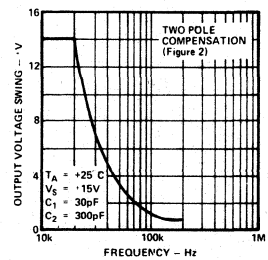
Open Loop Frequency Response



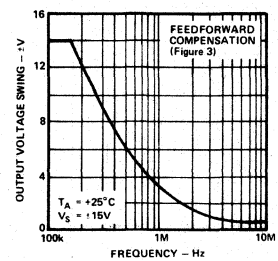
Open Loop Frequency Response



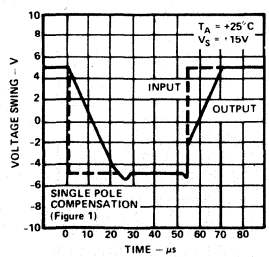
Large Signal Frequency Response



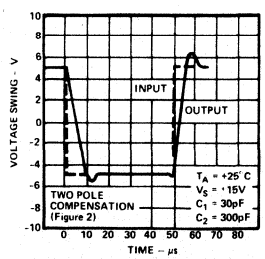
Large Signal Frequency Response



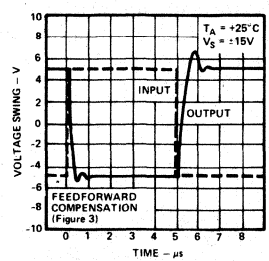
Large Signal Frequency Response



Voltage Follower Pulse Response



Voltage Follower Pulse Response



Inverter Pulse Response

ANALOG DEVICES

Wideband, Fast-Settling FET-Input Op Amp

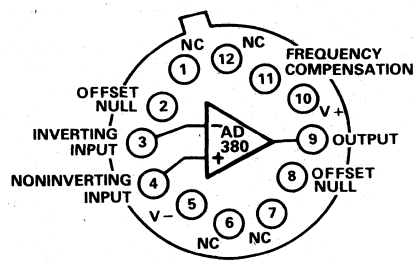
AD380

4

FEATURES

High Output Current: 50mA @ ±10V
Fast Settling to 0.1%: 130ns
High Slew Rate: 330V/μs
High Gain-Bandwidth Product: 300MHz
High Unity Gain Bandwidth: 40MHz
Low Offset Voltage (1mV for AD380K, L, S)

AD380 FUNCTIONAL BLOCK DIAGRAM



12-PIN TO-8 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD380 is a hybrid operational amplifier that combines the low input bias current advantages of a FET input stage with the high slew rate and line driving capability of a fast, high power output amplifier.

The AD380 has a slew rate of 330V/μs and will output ±10V at ±50mA. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate, or settling time for the given application.

A true differential input ensures equally superior performance in all system designs whether they are inverting, noninverting, or differential.

The AD380 is especially designed for use in applications, such as fast A/D, D/A and sampling circuits, that require fast and smooth settling and FET input parameters.

The AD380 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one extended temperature version, the S, specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans.

PRODUCT HIGHLIGHTS

1. The AD380's high output current (50mA @ ±10V) makes it suitable for driving terminated 200Ω twisted pairs.
2. The fast settling output (250ns to 0.01%) makes the AD380 an ideal choice for video A/D and D/A converters and sample and hold applications.
3. The settling wave forms are not only fast but are also very smooth. The absence of large overshoot and oscillations makes the AD380 a very predictable and dependable system element.
4. The high gain-bandwidth product (300MHz) ensures low distortion in high frequency applications.
5. Quick, symmetrical overdrive recovery time (250ns) is assured by an internal antisaturation diode. This is useful in applications where large transient signals may occur.
6. The precision input (1mV offset, max), along with fast settling and high current output make the AD380 an excellent choice for:
   - ATE pin drivers
   - precision coax buffers
   - signal conditioning on pulse waveforms
   - high resolution graphics displays.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD380JH	AD380KH	AD380LH	AD380SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, no load	40,000 min	*	*	*
V_{OUT} = ±10V, $R_L \geq 200\Omega$	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 200Ω, T_A = min to max	±12V (±10V min)	*	*	*
Output Impedance (Open Loop)	100Ω	*	*	*
Short Circuit Current	100mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	40MHz	*	*	*
Gain-Bandwidth Product, f = 100kHz, C_C = 1pF	300MHz (200MHz min)	*	*	*
Full Power Response	6MHz	*	*	*
Slew Rate, C_C = 1pF, 20V Swing	330V/μs (200V/μs min)	*	*	*
Settling Time: 10V Step to 1%	90ns	*	*	*
10V Step to 0.1%	130ns	*	*	*
10V Step to 0.01%	250ns	250ns (400ns max)	**	**
INPUT OFFSET VOLTAGE	2.0mV max	1.0mV max	**	**
vs. Temperature[1], T_A = min to max	50μV/°C max	20μV/°C max	10μV/°C max	50μV/°C max
vs. Supply	1mV/V max	*	*	*
INPUT BIAS CURRENT				
Either Input, Initial[2]	10pA (100pA max)	*	*	*
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{11}\Omega \| 6pF$	*	*	*
Common Mode	$10^{11}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[3]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	60dB min	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(6 to 20)V	*	*	*
Quiescent Current	12mA (15mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz to 100Hz	3.3μV p-p (0.5μV rms)	*	*	*
100Hz to 10kHz	6.6μV p-p (1μV rms)	*	*	*
10kHz to 1MHz	40μV p-p (6μV rms)	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance θ_{JA}	100°C/W	*	*	*
θ_{JC}	70°C/W	*	*	*
PACKAGE[4]				
TO-8 Style	H12A	*	*	*

NOTES
[1]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of offset nulled.
[2]Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures see Figure 16.
[3]Defined as the maximum safe voltage between inputs such that neither exceeds ±10V from ground.
[4]See Section 19 for package outline information.

*Specifications same as AD380JH.
**Specifications same as AD380KH.
Specifications subject to change without notice.

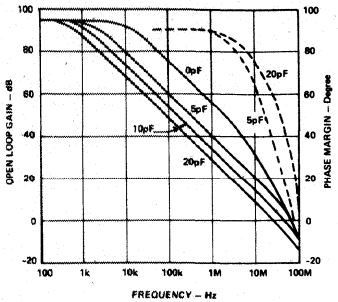


Figure 1. Open Loop Frequency Response

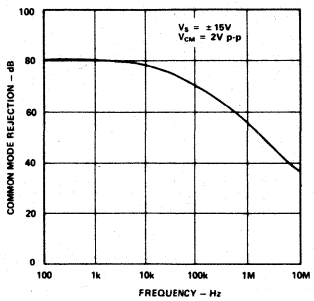


Figure 2. CMRR vs. Frequency

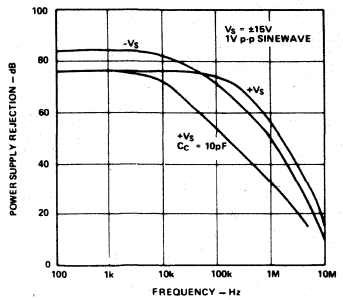


Figure 3. PSRR vs. Frequency

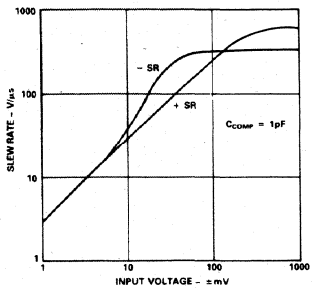


Figure 4. Slew Rate vs. Differential Input Voltage

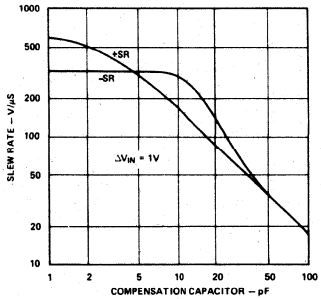


Figure 5. Slew Rate vs. Compensation Capacitor

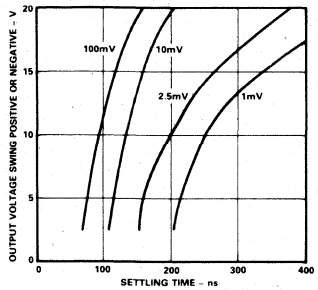


Figure 6. Output Settling Time vs. Output Voltage Swing and Error

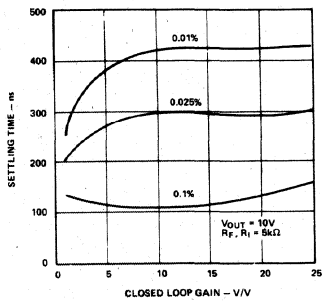


Figure 7. Settling Time vs. Closed Loop Gain

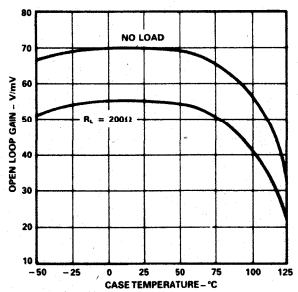


Figure 8. Gain vs. Temperature

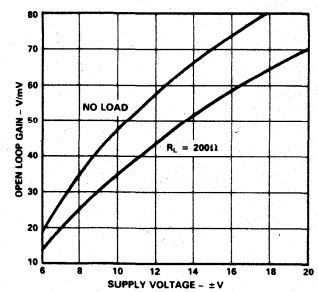


Figure 9. Gain vs. Supply Voltage

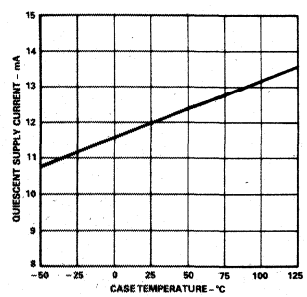


Figure 10. Supply Current vs. Temperature

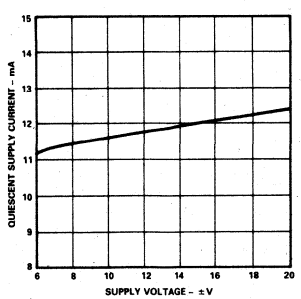


Figure 11. Supply Current vs. Supply Voltage

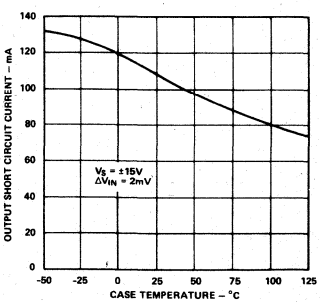


Figure 12. I_{SC} vs. Temperature

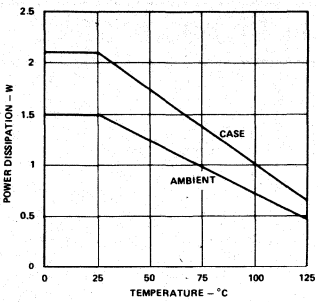


Figure 13. Power Dissipation vs. Temperature

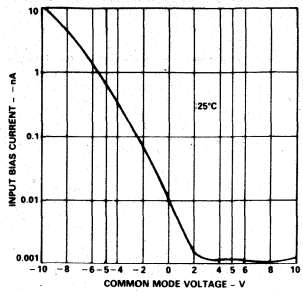


Figure 14. Input Bias Current vs. Common Mode Voltage

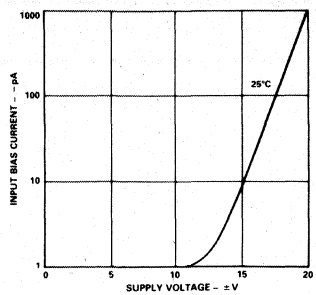


Figure 15. Input Bias Current vs. Supply Voltage

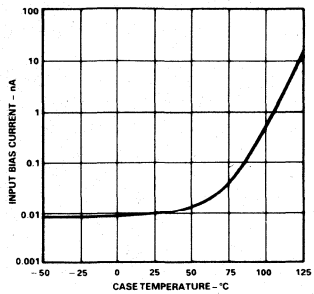


Figure 16. Input Bias Current vs. Temperature

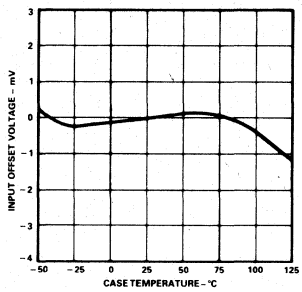


Figure 17. Offset Voltage vs. Temperature

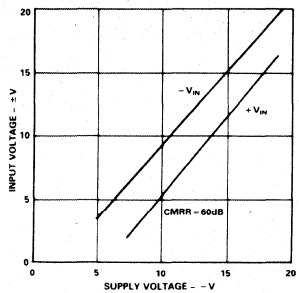


Figure 18. Input Voltage Range vs. Supply Voltage

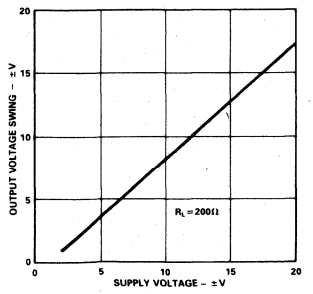


Figure 19. Output Voltage Swing vs. Supply Voltage

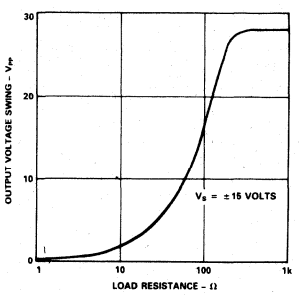


Figure 20. Output Voltage Swing vs. Load Resistance

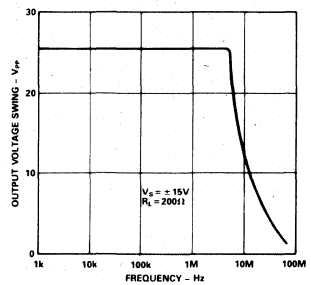


Figure 21. Large Signal Frequency Response

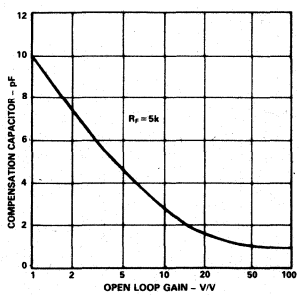


Figure 22. Recommended Compensation Capacitor vs. Closed Loop Gain

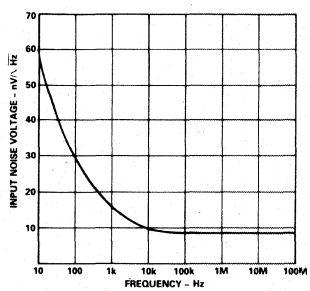


Figure 23. Input Noise Voltage Spectral Density

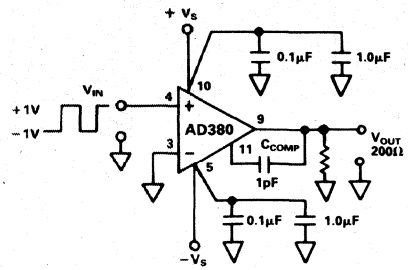


Figure 24a. Overdrive Recovery Test Circuit

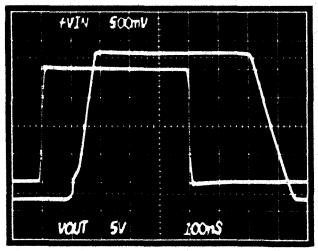


Figure 24b. Overdrive Recovery Response (Symmetrial 20ns Version Available)

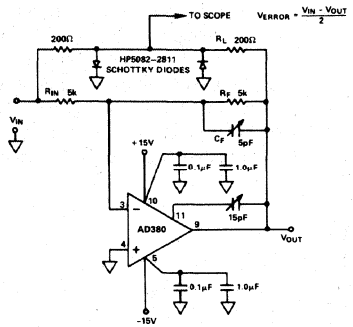


Figure 25a. Unity Gain Inverter Settling Time Test Circuit

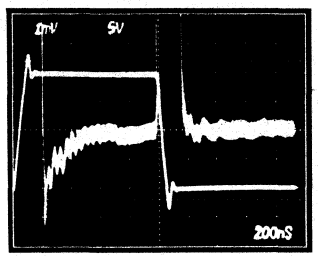


Figure 25b. Unity Gain Inverter Large Signal Response

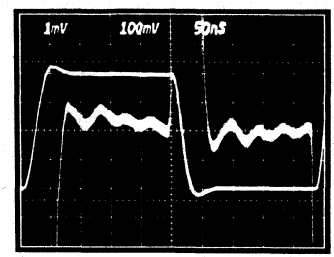


Figure 25c. Unity Gain Inverter Small Signal Response

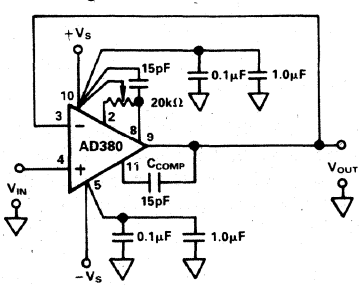


Figure 26a. Unity Gain Buffer Circuit

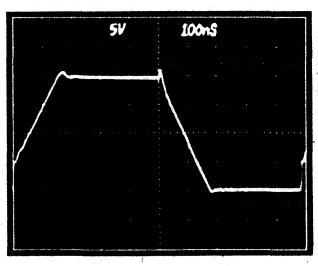


Figure 26b. Unity Gain Buffer Large Signal Response

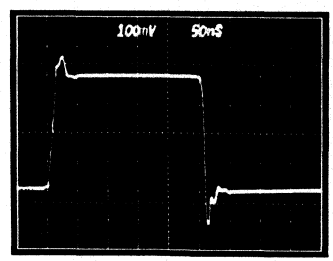


Figure 26c. Unity Gain Small Signal Response

APPLICATIONS INFORMATION

Compensation Capacitor

For low gain applications a 5pF to 27pF capacitor between the frequency compensation input (pin 11) and the output (pin 9) will reduce the risk of oscillation by adding phase margin. A compensation capacitor is especially needed when driving capacitive loads. For gains greater than 30 a 1pF compensation capacitor is recommended; see Figure 22.

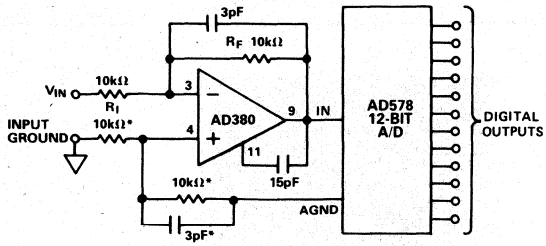
For unity gain buffer applications it may be necessary to add a small (10pF to 20pF) capacitor between pins 8 and 10 for improved phase margin; see Figure 26a.

Offset Null

If the initial offset voltage is not low enough for the user's application offset nulling is required. To null the offset tie a 20kΩ potentiometer between the offset null pins (pins 2 and 8). The wiper of the potentiometer is tied to the positive supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

To minimize the effects of offset voltage drift as a function of temperature, null the offset at the midpoint of the operating temperature range. For example, if the operating environment is 0°C to 70°C do the offset nulling at 35°C. This will insure a maximum offset voltage drift of 35 times the V_{OS} drift specification at either temperature extreme.

Typical Circuits



*Optional Differential Input Components Used to Reject Noise Between Input Ground and the A/D Analog Ground.

Figure 27. Fast-Settling Buffer

Its quick recovery from load variations makes the AD380 an excellent buffer for fast successive approximation A/D converters; see Figure 27.

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

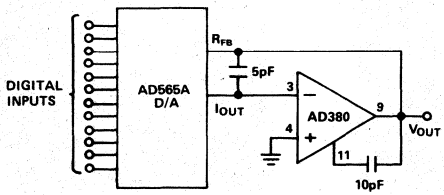


Figure 28. 12-Bit Voltage Output DAC Circuit Settles to 1/2LSB in 300ns

The AD565A 12-bit digital to analog converter with an AD380 output amplifier will give a voltage output that typically settles to within 1/2LSB in less than 300ns. Total settling time is the root mean square of the DAC current output settling time and the output amplifier settling time.

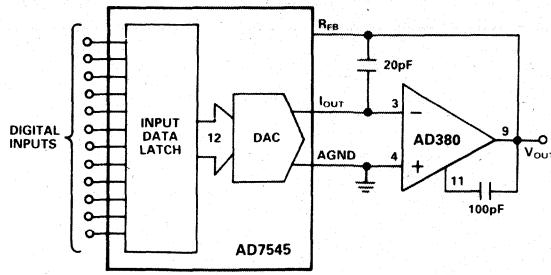


Figure 29. CMOS DAC Output Amplifier

CMOS DAC output amplifiers require low offset voltage op amps. The output impedance of CMOS DACs varies with input code. This can cause a code dependent error term at the output that approaches the op amps' offset voltage. If the DAC has a differential nonlinearity of 1/2LSB, it will require an output amplifier with less than 1/2LSB offset error to remain monotonic. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus, the AD380KH, with only 1mV offset maximum, will contribute less than 1/2LSB to differential linearity error.

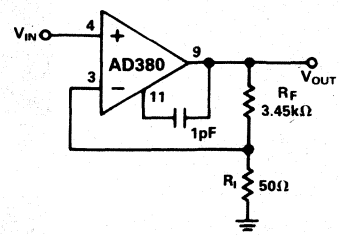


Figure 30. Video Amplifier

The high output current capability of the AD380 makes it suitable for video speed driver applications. In the circuit above the closed loop gain of 70 (37dB) is available over a bandwidth of 5MHz. Note that a 1pF compensation capacitor is required in this high gain application.

ANALOG DEVICES

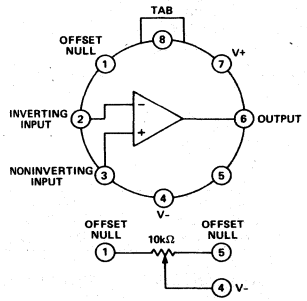
High Speed, Low Drift FET Operational Amplifier

AD381/AD382

4

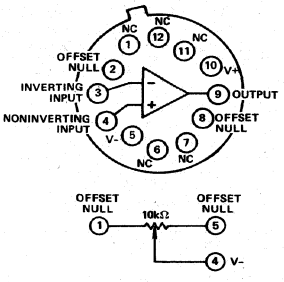
FEATURES
- **High Slew Rate 30V/μs**
- **Fast Settling to 0.1%: 750ns**
- **High Output Current: 50mA for AD382 (10mA for AD381)**
- **Low Drift (5μV/°C–L Grades)**
- **Low Offset Voltage (0.25mV–L Grades)**
- **Low Input Bias Currents**
- **Low Noise (2μV p-p)**

AD381 PIN CONFIGURATION



TOP VIEW

AD382 PIN CONFIGURATION



TOP VIEW

PRODUCT DESCRIPTION

The AD381/AD382 are hybrid operational amplifiers combining the very low input bias current advantages of a FET input stage with high slew rate and line driving capability of a high power output stage.

The offset voltage (0.25mV maximum for the L grades) and offset voltage drift (5μV/°C maximum for the L grades) are exceptionally low for high speed operational amplifiers.

In addition to superior low drift performance, the AD381 and AD382 offer the lowest guaranteed input bias currents of any wideband FET amplifier with 100pA max for the J grades of each and 50pA max for the AD382L grade. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our FET amplifiers are specified under actual operating conditions.

The AD381 and AD382 are especially designed for use in applications, such as precision high speed data acquisition systems and signal conditioning circuits, that require excellent input parameters and a fast, high power output.

The AD381 and AD382 are offered in three commercial versions, J, K and L specified from 0 to +70°C, and one extended temperature version, the S specified from −55°C to +125°C. All grades are packaged in hermetically sealed metal cans.

PRODUCT HIGHLIGHTS

1. Laser trimming techniques reduce offset voltage drift to 5μV/°C max and reduce offset voltage to only 0.25mV max on the L grade versions.
2. Analog Devices FET processing provides 100pA max (20pA typical) bias currents specified after 5 minutes of warm-up.
3. Internal frequency compensation, low offset voltage, and full device protection eliminate the need for external components and adjustments. This reduces circuit size and complexity and increases reliability.
4. The fast settling output (750ns to 0.1%) makes the AD381 and AD382 ideal for D/A and A/D converter amplifier applications.
5. The AD382's high output current (50mA minimum at ±10 volts) makes it suitable for driving terminated (200Ω) twisted pair outputs over the commercial temperature ranges.
6. The high slew rate (30V/μs) and high gain bandwidth product (5MHz) make the AD381 and AD382 an ideal choice for sample and holds and for high speed integrator circuits.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD381JH AD382JH	AD381KH AD382KH	AD381LH AD382LH	AD381SH AD382SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$ (AD381)	60,000 min	100,000 min	**	**
V_{OUT} = ±10V, R_L = 200Ω (AD382)	25,000 min	35,000 min	**	**
R_L = 10kΩ (AD382)	100,000	150,000	**	**
OUTPUT CHARACTERISTICS (AD382)				
Voltage @ R_L = 200Ω	±12V (±10V min)	*	*	Note 1
Voltage @ R_L = 10kΩ	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	80mA	*	*	*
OUTPUT CHARACTERISTICS (AD381)				
Voltage @ R_L = 1kΩ, T_A = min to max	±12V (±10V min)	*	*	Note 2
Voltage @ R_L = 2kΩ, T_A = min to max	±12V (±10V min)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	20mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	5MHz	*	*	*
Full Power Response	500kHz	*	*	*
Slew Rate, Unity Gain	30V/μs (20V/μs min)	*	*	*
Settling Time: 10V Step to 0.1%	700ns	*	*	*
10V Step to 0.01%	1.2μs	1.2μs (2.0μs max)	**	**
INPUT OFFSET VOLTAGE	1.0mV max	0.5mV max	0.25mV max	*
vs. Temperature, T_A = min to max[3]	15μV/°C max	10μV/°C max	5μV/°C max	10μV/°C max
vs. Supply	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT[4]				
Either Input	20pA (100pA max)	10pA (50pA max)(* for AD381)	** (* for AD381)	** (* for AD381)
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 7pF$	*	*	*
Common Mode	$10^{12}\Omega \| 7pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	70dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	
Quiescent Current AD382	3.4mA (6mA max)	*	*	*
AD381	3.2mA (5mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz–10Hz	2μV p-p	*	*	*
10Hz	35nV/√Hz	*	*	*
100Hz	22nV/√Hz	*	*	*
1kHz	18nV/√Hz	*	*	*
10kHz	16nV/√Hz	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance−θJA (AD382)	100°C/W	*	*	*
Thermal Resistance−θJC (AD382)	70°C/W	*	*	*

NOTES

[1]The AD381SH has an output voltage of ±12V (±10V min) for a 1kΩ load from T_{min} to +70°C. From +70°C to +125°C the output current is 7mA.

[2]The AD382SH has an output voltage of ±12V (±10V min) for a 200Ω load from T_{min} to +100°C. To +125°C the output current is 35mA.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C for every mV of offset nulled.

[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as J grade.

**Specifications same as K grade.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Initial Offset	Offset T.C.	Output	Package[1]
AD381JH	1mV	15μV/°C	10mA	H08B
AD381KH	0.5mV	10μV/°C	10mA	H08B
AD381LH	0.25mV	5μV/°C	10mA	H08B
AD381SH	1mV	10μV/°C	10mA	H08B
AD382JH	1mV	15μV/°C	50mA	H12A
AD382KH	0.5mV	10μV/°C	50mA	H12A
AD382LH	0.25mV	5μV/°C	50mA	H12A
AD382SH	1mV	10μV/°C	50mA	H12A

NOTE

[1]See Section 19 for package outline information.

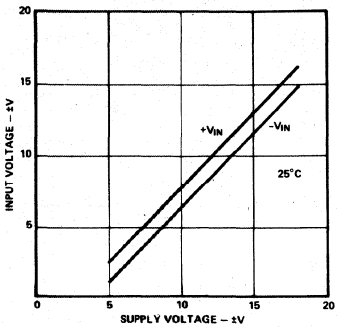


Figure 1. Input Voltage Range vs. Supply Voltage

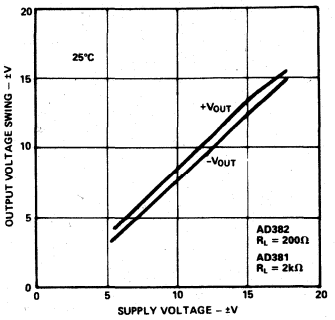


Figure 2. Output Voltage Swing vs. Supply Voltage

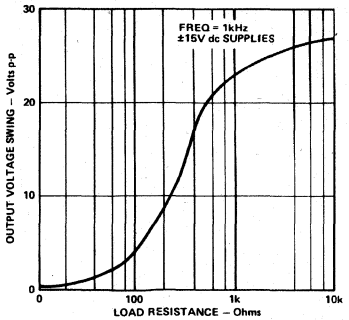


Figure 3a. Output Voltage Swing vs. Load Resistor for AD381

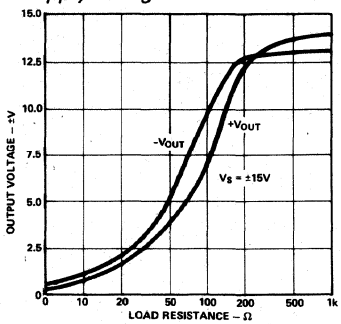


Figure 3b. Output Voltage Swing vs. Load Resistor for AD382

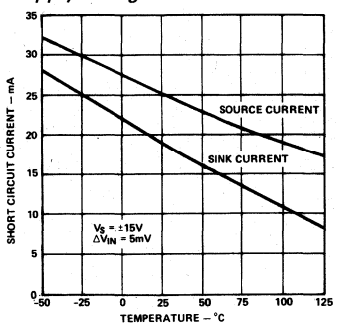


Figure 4a. Short Circuit Current vs. Temperature for AD381

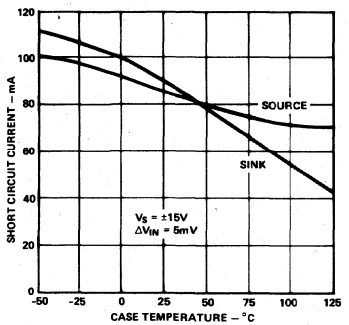


Figure 4b. Short Circuit Current vs. Temperature for AD382

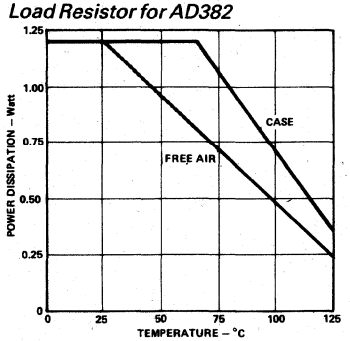


Figure 5. Permitted Dissipation vs. Temperature for AD382

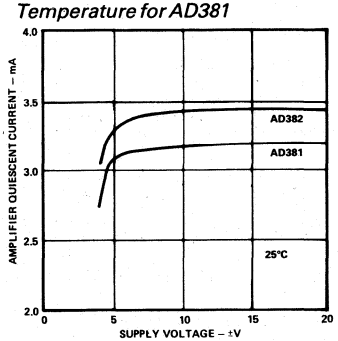


Figure 6. Quiescent Current vs. Supply Voltage

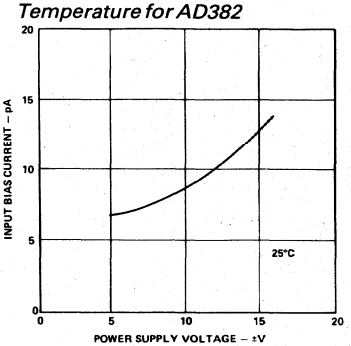


Figure 7. Input Bias Current vs. Supply Voltage

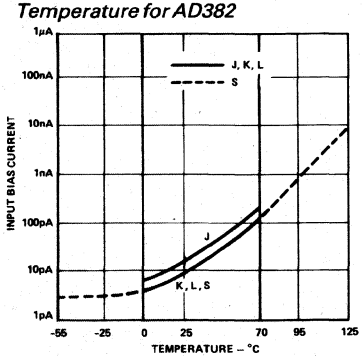


Figure 8. Input Bias Current vs. Temperature

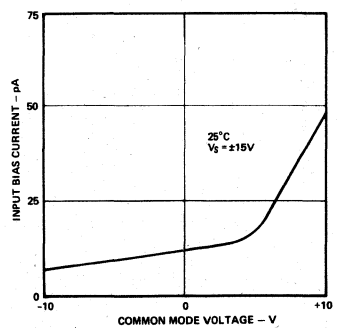


Figure 9. Input Bias Current vs. CMV

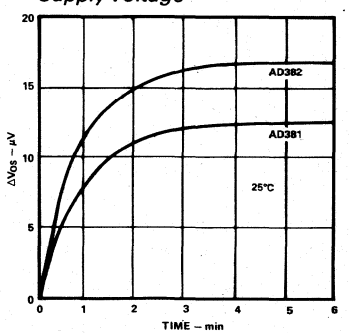


Figure 10. Input Offset Voltage Turn On Drift vs. Time

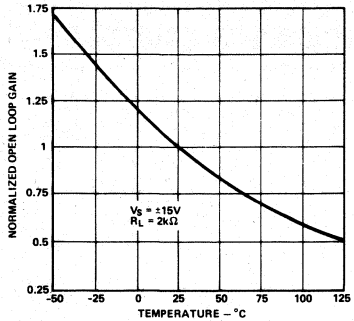


Figure 11a. Open Loop Gain vs. Temperature for AD381

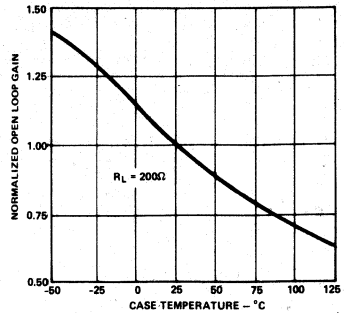


Figure 11b. Open Loop Gain vs. Temperature for AD382

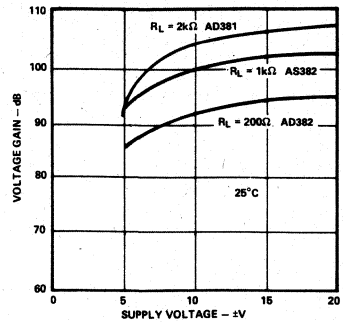


Figure 12. Open Loop Voltage Gain vs. Supply Voltage

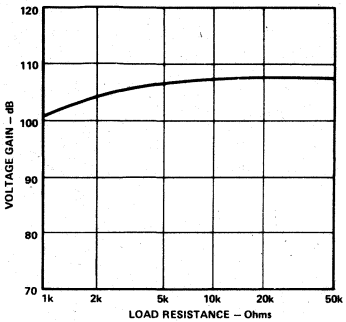


Figure 13a. Voltage Gain vs. Load Resistance for AD381

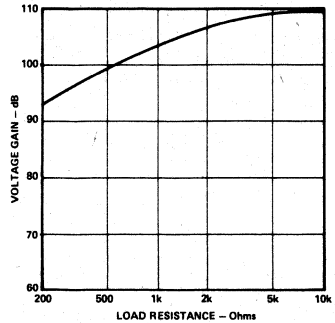


Figure 13b. Voltage Gain vs. Load Resistance for AD382

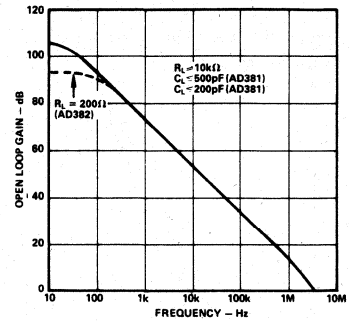


Figure 14. Open Loop Gain vs. Frequency

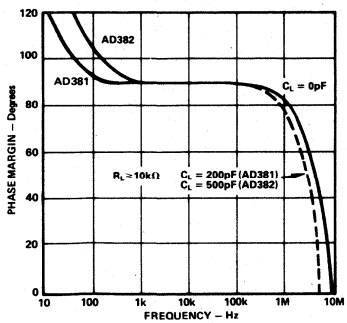


Figure 15. Phase Margin vs. Frequency

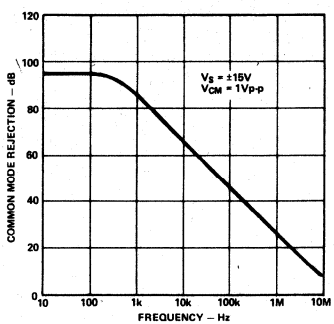


Figure 16. Common-Mode Rejection vs. Frequency

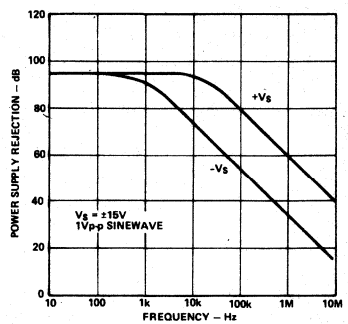


Figure 17. Power Supply Rejection vs. Frequency

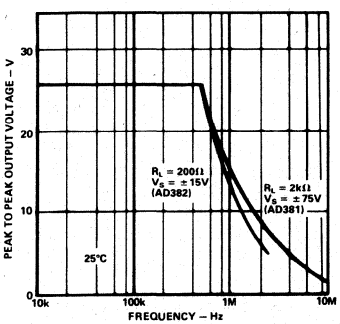


Figure 18. Large Signal Frequency Response

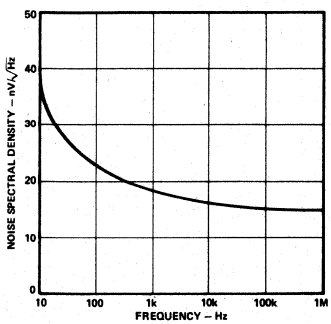


Figure 19. Noise vs. Frequency

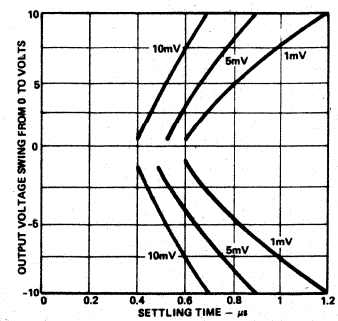


Figure 20a. AD381 Output Settling Time vs. Output Voltage Swing and Error (Circuit of Figure 22a)

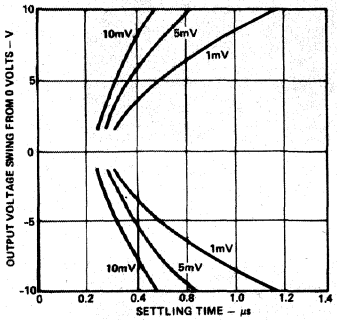


Figure 20b. AD382 Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

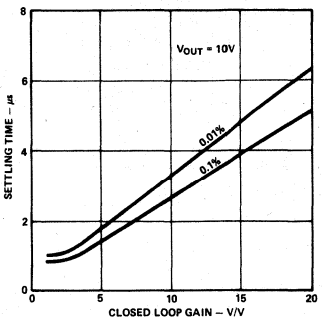


Figure 21. Settling Time vs. Closed Loop Gain (Circuits of Figures 22a & 23a)

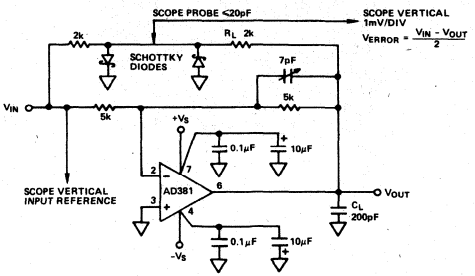


Figure 22a. AD381 Unity Gain Inverter and Settling Time Test Circuit

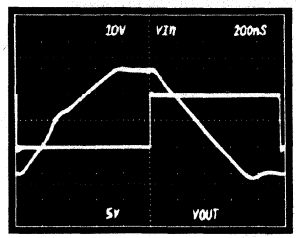


Figure 22b. AD381 Unity Gain Inverter Pulse Response (Large Signal)

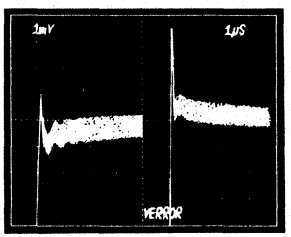


Figure 22c. AD381 Unity Gain Inverter Pulse Response (Large Signal Error Voltage)

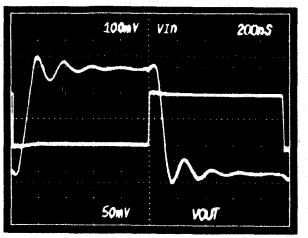


Figure 22d. AD381 Unity Gain Inverter Pulse Response (Small Signal)

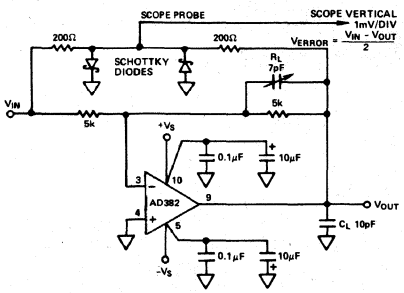


Figure 23a. AD382 Unity Gain and Settling Time Test Circuit

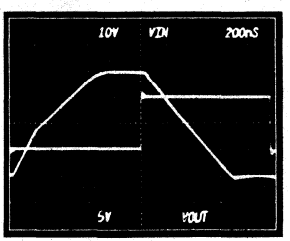


Figure 23b. AD382 Unity Gain Inverter Pulse Response (Large Signal)

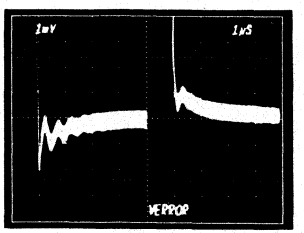


Figure 23c. Unity Gain Inverter Pulse Response (Large Signal Error Voltage)

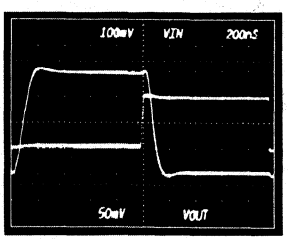


Figure 23d. AD382 Unity Gain Inverter Pulse Response (Small Signal)

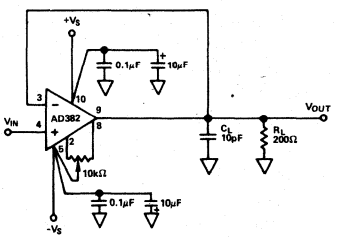


Figure 24a. AD382 Unity Gain Follower

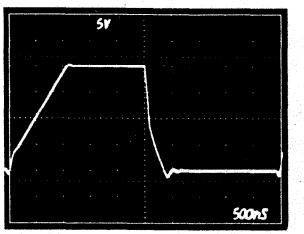


Figure 24b. AD382 Unity Gain Follower Pulse Response (Large Signal)

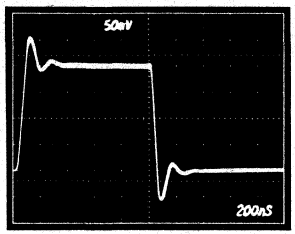


Figure 24c. AD382 Unity Gain Follower Pulse Response (Small Signal)

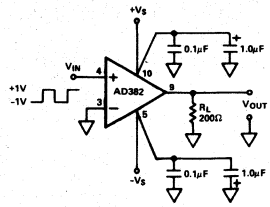


Figure 25a. AD382 Overdrive Recovery Test Circuit

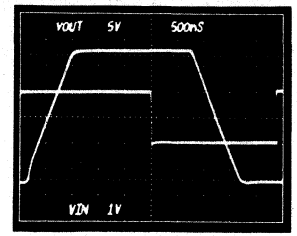


Figure 25b. AD382 Overdrive Recovery Response

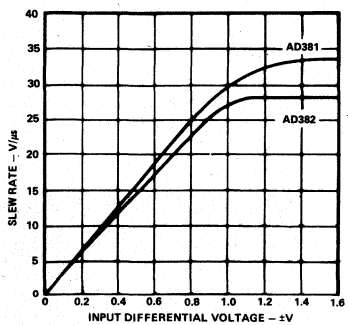


Figure 26. Slew Rate vs. Input Voltage

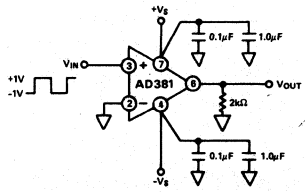


Figure 27a. AD381 Overdrive Recovery Test Circuit

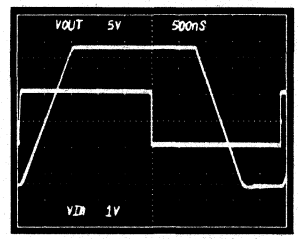


Figure 27b. AD381 Overdrive Recovery Response

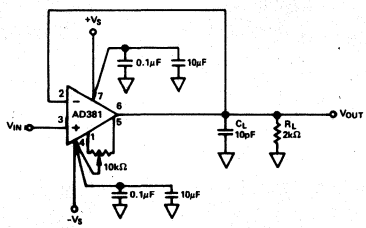


Figure 28a. AD381 Unity Gain Follower

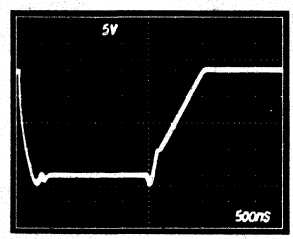


Figure 28b. AD381 Unity Gain Follower Large Signal Pulse Response

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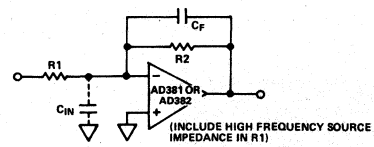
Compensation Capacitor

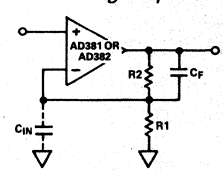
The AD381 and AD382 have sufficient phase margin to insure stability in most applications without compensation. However, in applications with capacitive load, very high speed, low gain or high resistor values ($R_{IN} \geq 5k\Omega$) the high frequency noise rejection will be improved by adding a compensation capacitor. The AD381 and AD382 have an input capacitance of 7pF. When soldered on a printed circuit board or inserted in a socket the total input capacitance could be 10pF. This input capacitance can lower the 0° phase margin crossover point from 8MHz, as shown in Figure 14, to around 1MHz.

By adding a small compensation capacitor in the feedback loop we can cancel the effects of the input capacitance and reduce high frequency noise gain. 5 to 10pF will suffice in most applications. In some current output, digital-to-analog converter applications the output capacitance of the DAC may be 200pF which would require a large compensation capacitor in the amplifier feedback loop.

A scheme for compensating inverting and noninverting circuits is shown in Figure 29. Choose $C_F = C_{IN} \frac{R1}{R2}$.



a. Inverting Amplifier



b. Noninverting Amplifier

Figure 29.

Offset Null

The AD381/AD382 should not have to be offset nulled for most applications because of its low initial offset voltage. If nulling is required for very high precision applications, such as an output amplifier for 13-bit or better digital-to-analog converters, connect a 10kΩ potentiometer between the offset null pins (pins 1 and 5 for the AD381 and pins 2 and 8 for the AD382). The wiper of the potentiometer is tied to the negative supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

AD382 Heat Sinking

A heat sink for convection cooling is required if operating at full power and at ambient temperatures greater than 70°C. As shown in Figure 5 the free air power dissipation curve for the AD382 crosses the full power dissipation point (0.75W) at 70°C. The power dissipation can be improved by using a heat sink up to the case power dissipation curve (also referred to as the infinite heat sink power dissipation curve). We recommend connecting the heat sink to the AD382 case and keeping the combination ungrounded.

TYPICAL CIRCUITS

In many digital-to-analog converter applications, including automatic test equipment, the load may be large enough to require a buffer amplifier. The AD382 can supply ±10V into a 200Ω load. The AD381 can supply up to ±10V into a 1kΩ load.

The AD381 and AD382 are also well suited for CMOS DAC output amplifier applications due to their low initial offset voltage.

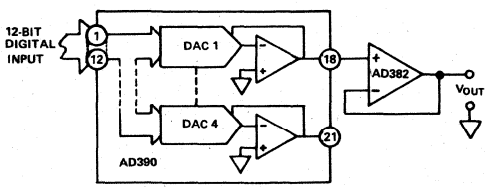


Figure 30. Buffer Amplifier to a 12-Bit Voltage Output DAC

No external trims are required with 12-bit CMOS DACs. Since the output impedance of CMOS DACs varies with input code, the output voltage could appear nonmonotonic if the offset voltage is greater than 1/2LSB. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus the AD381 and AD382, with only 1mV of offset maximum, assure monotonic performance without external trims.

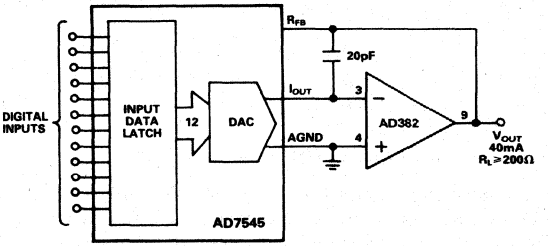
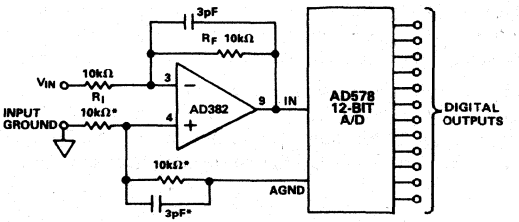


Figure 31. CMOS DAC Output Amplifier



*Optional Differential Input Components Used to Reject Noise Between Input Ground and the A/D Analog Ground.

Figure 32. Fast-Settling Buffer

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

Its quick recovery from load variations makes the AD382 an excellent buffer for fast successive approximation A/D converters.

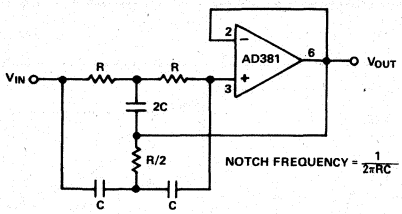


Figure 33. High Q Notch Filter

The above notch filter will have a notch of −55dB. To obtain a Q of 100 the capacitors should be well matched. Polystyrene, Teflon or NPO ceramic capacitors and metal-film resistors are recommended. For low frequency filter applications resistor values will be large. The AD381 is well suited for this application due to its low input bias current. It is also good for high frequency filtering because of its wide gain bandwidth product. This filter is capable of driving 1kΩ loads over a ±10V output range.

Figure 34 shows a fast sample and hold circuit that can acquire a sample to 0.01% in 2μs (20 volt swing). The AD381 is well suited for fast 12-bit sample/hold amplifier circuits. R1 and R2 set the circuit gain. R3 is adjusted for minimum ac feedthrough. Potentiometer R4 is set for minimum sample/hold offset voltage. R6 improves the settling time and circuit stability by adding phase margin. Bias resistors R7 and R8 insure complete shut-off of the D-MOS FET switches at TTL logic zero. Pull up resistors R9 and R10 lower the on resistance of the D-MOS switches. The SD5000 D-MOS switch is recommended for its fast transition speed and low on resistance.

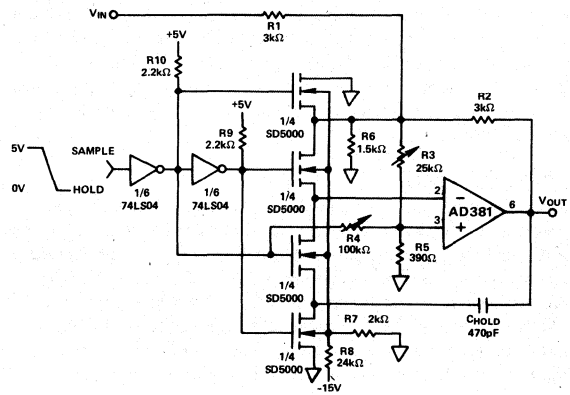


Figure 34. Fast Sample/Hold Amplifier

ANALOG DEVICES

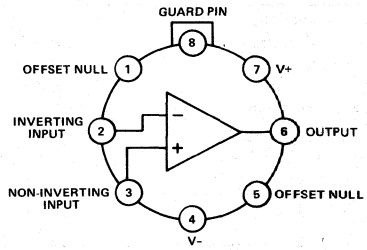
High Accuracy Low Offset IC FET-Input Op Amps

AD503, AD506

FEATURES

Low I_b: 15pA max (AD503J, AD506J)
5pA max (AD506L)
Low V_{OS}: 1mV max (AD506L)
Low Drift: 25μV/°C max (AD503K, AD506K)
10μV/°C max (AD506L)

AD503, AD506 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD503J/AD506J, AD503K/AD506K, AD506L and AD503S/AD506S are IC FET input op amps that provide the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The devices achieve maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. They are free from latch-up and are short circuit protected. No external compensation is required as the internal 6dB/octave rolloff provides stability in closed loop applications.

The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance. The AD506, with specifications otherwise similar to the AD503, offers significant improvement in offset voltage and nulled offset voltage drift by supplementing the AD503 configuration with internal laser trimming of thin film resistors to provide typical offset voltages below 1mV.

The AD503 and AD506 are especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the noninverting "buffer" connection is used). The AD503 and AD506 IC FET input amplifiers, therefore, are of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

All the circuits are supplied in the TO-99 package; the AD503J, K and AD506J, K and L are specified for 0 to +70°C temperature range operation; the AD503S and AD506S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD503 and AD506 op amps meet their published input bias current and offset voltage specs after full warmup. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD503 and AD506 are specified as a maximum for *either* input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Offset voltage nulling of the AD503 and AD506 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±0.8μV/°C per millivolt of nulled offset for the AD506 and ±2.0μV/°C per millivolt of nulled offset for the AD503, compared to several times this for other IC FET op amps.
4. The gain of the AD503 and AD506 is measured with the offset voltage nulled. Nulling a FET input op amp can cause the gain to decrease below its specified limit. The gain of the AD503 and AD506 is fully guaranteed with the offset voltage both nulled and unnulled.
5. Bootstrapping of the input FET's achieves a superior CMRR of 80dB, while reducing bias currents and maintaining them constant through the CMV range.

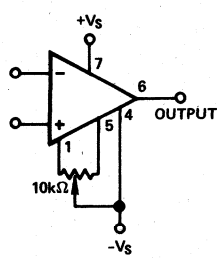
SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/μs min (6.0V/μs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10μs	*	*
INPUT OFFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs. Temperature, T_A = min to max	75μV/°C max (30μV/°C typ)	25μV/°C max (10μV/°C typ)	50μV/°C max (20μV/°C typ)
vs. Supply, T_A = min to max	400μV/V max (200μV/V typ)	200μV/V max (100μV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	$10^{11}\Omega \| 2pF$	*	*
Common Mode	$10^{12}\Omega \| 2pF$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*
5Hz to 50kHz	5.0μV (rms)	*	*
f = 1kHz (spot noise)	$30.0nV/\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*
PACKAGE OPTIONS:[6] TO-99 Style (H08B)	AD503JH	AD503KH	AD503SH

NOTES
[1] Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2] A conservative design would not exceed 500pF of load capacitance.
[3] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4] Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[5] See comments in Input Considerations Section.
[6] See Section 19 for package outline information.

*Specifications same as for AD503J.
**Specifications same as for AD503K.
Specifications subject to change without notice.

AD506J	AD506K	AD506L	AD506S
*	**	75,000 min (100,000 typ)	**
*	**	50,000 min	25,000 min
*	*	*	*
*	*	*	*
1000pF	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
3.5mV max (1.0mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.4mV typ)	1.5mV max (0.5mV typ)
*	**	10μV/°C max (5μV/°C typ)	50μV/°C max (20μV/°C typ)
**	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)
*	**	5pA max (2pA typ)	**
*	*	*	*
*	*	*	*
40μV (p-p)	*	*	*
8μV (rms)	*	6μV (rms)	*
80nV/√Hz	*	25nV/√Hz	*
±4V	*	*	*
*	*	*	*
*	**	**	**
*	*	*	*
*	*	*	±(5 to 22)V
7mA max (5mA typ)	*	*	*
*	*	*	-55°C to +125°C
*	*	*	*
AD506JH	AD506KH	AD506LH	AD506SH



Standard Offset Null Circuit

APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 and AD506 specify maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced in the AD503 and AD506 by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

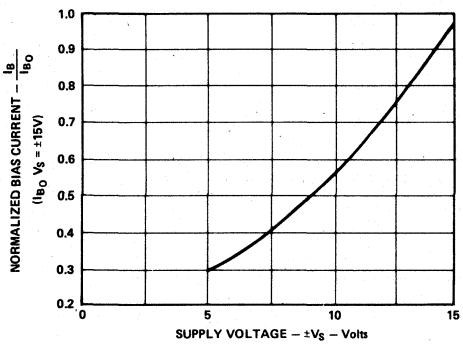


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD503K and AD506K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

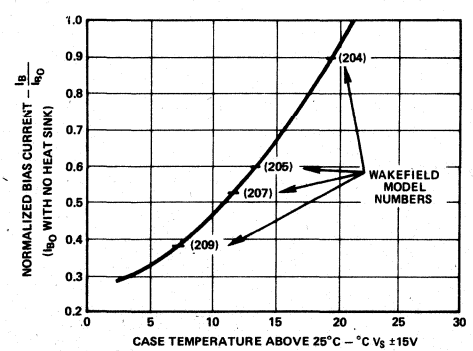


Figure 2. Normalized Bias Current vs. Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503/AD506K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

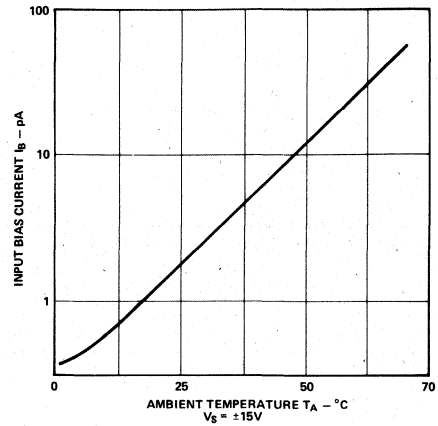


Figure 3. Input Bias Current vs. Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 volts and negative common mode inputs to $-V_S$ are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed $V_{CM} = V_S$.

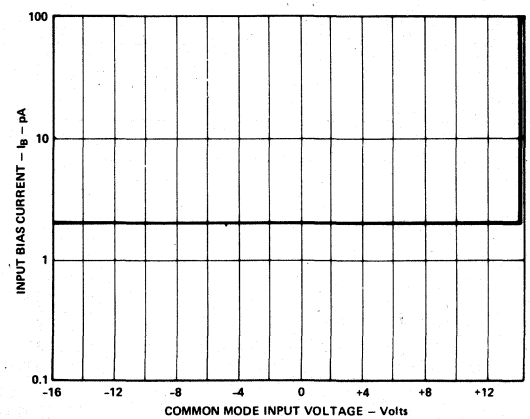


Figure 4. Input Bias Current vs. Common Mode Voltage

Like most other FET input op amps, the AD503 and AD506 display a degraded bias current specification when operated at moderate differential input voltages. The AD503 maintains its specified bias current up to a differential input voltage of ±3V typically, while the AD506's bias current performance is not significantly degraded for $V_{diff} \leqslant 4V$ typically. Above V_{diff} = ±3V in the AD503 and V_{diff} = ±4V in the AD506, the bias current will increase to approximately 400μA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase 100μA/V_{diff} (in volts), and other parameters may suffer degradation.

ANALOG DEVICES

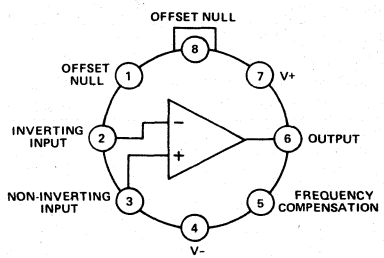
High Accuracy IC Operational Amplifier

AD504

4

FEATURES
Low V_{OS}: 500μV max (AD504M)
High Gain: 10^6 min (AD504L, M, S)
Low Drift: 0.5μV/°C max (AD504M)
Free of Popcorn Noise

AD504 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD504J, K, L, M and S IC operational amplifiers provide ultra-low drift and extremely high gain, comparable to that of modular amplifiers, for precision applications. A new double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than 10^6, offset voltage drift of less than 1μV/°C, small signal unity gain bandwidth of 300kHz, and slew rate of 0.12V/μs. Because of monolithic construction, the cost of the AD504 is significantly below that of modules, and becomes even lower with larger quantity requirements. The amplifier is externally compensated for unity gain with a single 470pF capacitor; no compensation is required for gains above 500. The inputs are fully protected, which permits differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits to ground and/or either supply voltage, and is capable of driving 1000pF of load capacitance. The AD504J, K, L and M are supplied in the hermetically sealed TO-99 package, and are specified for operation over the 0 to +70°C temperature range. The AD504S is specified over the -55°C to +125°C temperature range and is also supplied in the TO-99 package.

PRODUCT HIGHLIGHTS

1. Fully guaranteed and 100% tested 1μV/°C maximum voltage drift combined with voltage offset of 500μV (AD504L).
2. Fully protected input ($\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, and is of critical importance in this type of device whose overall performance is strongly dependent upon front-end stability.
3. Single capacitor compensation eliminates elaborate stabilizing networks while providing flexibility not possible with an internally compensated op amp. This feature allows bandwidth to be optimized by the user for his particular application.
4. High gain is maintained independent of offset nulling, power supply voltage and load resistance.
5. Bootstrapping of the critical input transistor quad produces CMRR and PSRR compatible with the tight 1μV/°C drift. CMRR and PSRR are both in the vicinity of 120dB.
6. Noise performance is closely monitored at Outgoing QC to ensure compatibility with the low error budgets afforded by the performance of all other parameters.
7. Every AD504 receives a stabilization bake for 24 hours at 150°C to ensure reliability and long term stability.
8. The 100 piece price of the AD504 is 1/3 to 1/2 less than that of modular low drift operational amplifiers, and is competitive with the price of less accurate IC op amps.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

PARAMETER	AD504J	AD504K	AD504L
OPEN LOOP GAIN			
V_{OS} = ±10V, $R_L \geq 2k\Omega$	250,000 min (4 x 10^6 typ)	500,000 min (4 x 10^6 typ)	10^6 min (8 x 10^6 typ)
$T_{min} \leq T_A \leq T_{max}$	125,000 min (10^6 typ)	250,000 min (10^6 typ)	500,000 min (10^6 typ)
OUTPUT CHARACTERISTICS			
Voltage at $R_L \geq 2k\Omega$, $T_{min} \leq T_A \leq T_{max}$	±10V min (±13V typ)	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal, C_c = 390pF	300kHz	*	*
Full Power Response, C_c = 390pF	1.5kHz	*	*
Slew Rate, Unity Gain, C_c = 390pF	0.12V/μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leq 10k$	2.5mV max (0.5mV typ)	1.5mV max (0.5mV typ)	0.5mV max (0.2mV typ)
vs Temp, $T_{min} \leq T_A \leq T_{max}$, V_{OS} nulled	5.0μV/°C max (0.5μV/°C typ)	3.0μV/°C max (0.5μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
$T_{min} \leq T_A \leq T_{max}$, V_{OS} unnulled†	10μV/°C max (1.5μV/°C typ)	5.0μV/°C max (1.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
vs Supply	25μV/V max	15μV/V max	10μV/V max
@ $T_{min} \leq T_A \leq T_{max}$	40μV/V	25μV/V max	15μV/V max
vs Time	20μV/mo	15μV/mo	10μV/mo
INPUT OFFSET CURRENT			
@ T_A = 25°C	40nA max	15nA max	10nA max
INPUT BIAS CURRENT			
Initial	200nA max	100nA max	80nA max
T_{min} to T_{max}	300nA max	150nA max	100nA max
vs Temp, T_{min} to T_{max}	300pA/°C	250pA/°C	200pA/°C
INPUT IMPEDANCE			
Differential	0.5MΩ	1.0MΩ	1.3MΩ
Common Mode	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.1 to 10Hz	1.0μV (p-p)	*	*
100Hz	10nV/√Hz(rms)	*	*
1kHz	8nV/√Hz(rms)	*	*
Current, 0.1 to 10Hz	50pA(p-p)	*	*
100Hz	0.6pA/√Hz(rms)	*	*
1kHz	0.5pA/√Hz(rms)	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, Max Safe	$\pm V_S$	*	*
Common Mode Rejection, V_{IN} = ±10V	94dB min (120dB typ)	100dB min (120dB typ)	110dB min (120dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
TEMPERATURE RANGE			
Operating, Rated Performance			
(T_{min} to T_{max})	0 to +70°C	*	*
Storage	-65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08B)	AD504JH	AD504KH	AD504LH

NOTES
*Specifications same as for AD504J.
[1] See Section 19 for package outline information.
Specifications subject to change without notice.

NOTE
Analog Devices 100% tests and guarantees all specified maximum and minimum limits. Certain parameters, because of the relative difficulty and cost of 100% testing, have been specified as "typical" numbers. At ADI, "typical" numbers are subjected to rigid statistical sampling and outgoing quality control procedures, resulting in "typicals" that are indicative of the performance that can be expected by the user.

AD504M	AD504S(AD504S/883)
10^6 min (8 x 10^6 typ)	10^6 min (8 x 10^6 typ)
500,000 min (10^6 typ)	250,000 min
*	*
*	*
*	*
*	*
*	*
*	*
*	*
0.5mV max (0.2mV typ)	0.5mV max
0.5μV/°C max (0.2μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
1.0μV/°C max (0.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
10μV/V max	10μV/V max
15μV/V max	20μV/V max
10μV/mo	10μV/mo
10nA max	10nA max
80nA max	80nA max
100nA max	200nA max
200pA/°C	200pA/°C
1.3MΩ	1.3MΩ
*	*
0.6μV (p-p) max	*
10nV/$\sqrt{Hz}$ max	*
9nV/$\sqrt{Hz}$ max	*
50pA p-p max	*
0.6pA/$\sqrt{Hz}$ max	*
0.3pA/$\sqrt{Hz}$ max	*
*	*
110dB min (120dB typ)	110dB min (120dB typ)
*	*
*	*
±3.0mA max (±1.5mA typ)	±3mA max (±1.5mA typ)
*	-55°C to +125°C
*	-65°C to +150°C
AD504MH	AD504SH

OFFSET VOLTAGE DRIFT AND NULLING

Most differential operational amplifiers have provisions for adjusting the initial offset voltage to zero with an external trim potentiometer. It is often not realized that there is a resulting increase in voltage drift which accompanies this initial offset adjustment. The increased voltage drift can often be safely ignored in conventional amplifiers, since it may be a small percentage of the specified voltage drift. However, the voltage drift of the AD504 is so small that this effect cannot be ignored.

To achieve low drift over temperature, it is necessary to maintain equal current densities in the input pair. Unless the initial offset nulling circuit is carefully arranged, the nulling circuits will themselves drift with temperature. The resulting change in the input transistor current *ratio* will produce an additional input offset voltage drift. This drift component can actually be larger than the unnulled drift.

Typically, IC op amps are nulled by using an external potentiometer to adjust the ratio of two resistances. These resistances are part of a network from which the input stage emitter currents are derived. Most commercially available op amps use diffused resistors in their internal nulling circuitry, which typically display large positive temperature coefficients of the order of 2000ppm/°C. As a result of the failure of the external potentiometer resistance to track the diffused resistors over temperature, the two resistance branches will drift relative to one another. This will cause a change in the emitter current ratio and induce an offset drift with temperature.

In the AD504, this problem is reduced an order of magnitude by the use of thin film resistors deposited on the monolithic amplifier chip. These resistors, which make up the critical bias network from which the input stage emitter current balance is determined, display typical temperature coefficients of less than 200ppm/°C, an order of magnitude improvement over diffused types. Thus, when the initial offset of the AD504 is trimmed using a low TC pot in combination with the thin film network, the drift induced by nulling even relatively large offsets is extremely small. This means that AD504 units of all three grades (J, K, L) will typically yield significantly better temperature performance in nulled applications than an all-diffused amplifier with comparable initial offset.

Since the intrinsic offset drift of the amplifier is improved by nulling, the direct measurement of any additional drift induced by differing temperature coefficients of resistors would be extremely difficult. However, the *induced* offset drift can be established by calculating the change in the emitter current ratio brought about by the differing TC's of resistances. From the change in this ratio, the offset voltage contribution at any temperature can be easily calculated.

A simple computer program was written to calculate induced offset drift as a function of initial offset voltage nulled. This calculation was made assuming zero TC of the amplifier resistors, and TC's of 200ppm/°C and 2000ppm/°C for the null pot. These results are very nearly equivalent to the case where the pot has zero temperature coefficient and the amplifier resistors drift. The results of these calculations are summarized graphically in Figure 1.

Figure 1 shows the variation of induced voltage drift with nulled offset voltage for:

a. AD504 op amp.
b. 725 typ op amp.

Note that as a result of nulling 1.4mV of offset, *the AD504 induces 30X less offset drift (only 0.05μV/°C) than the 725 type op amp* with its actual diffused resistor values and the recommended 100k pot to trim the offset. Actual induced drifts from this source for the AD504 may be even lower in the practical case when metal film resistors or pots are used for nulling since their TC's tend to closely *match* the negative TC's of the thin film resistors on the AD504 chip.

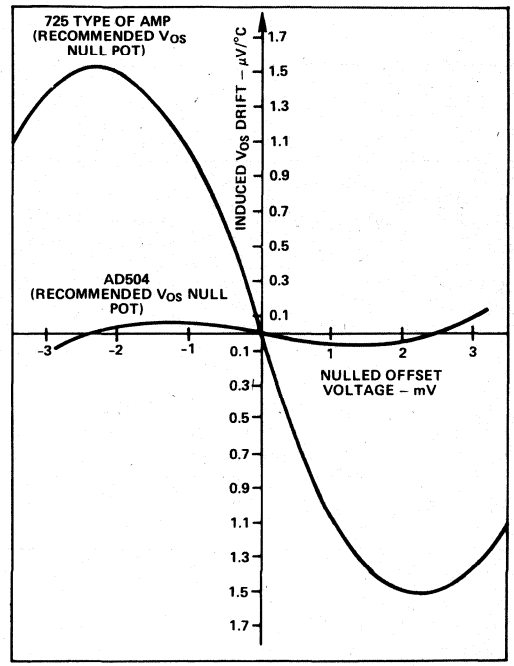


Figure 1. Induced Offset Drift vs. Nulled Offset Using Manufacturer's Recommended Adjustment Potentiometer

NULLING THE AD504

Since calculations show that superior drift performance can be realized with the AD504, special care should be taken to null it in the most advantageous manner. Using the actual values of resistors in the AD504, it is possible to calculate, under worst case conditions, that the total adjustment range of the AD504 is approximately 8mV. Since the amplifier may often be trimmed to within 1μV, this represents an adjustment of 1 part in 8000. This type of accuracy would require a pot with 0.0125% resolution and stability. Because of the problems of obtaining a pot of this stability, a slightly more sophisticated nulling operation is recommended for applications where offset drift is critical (see Figure 2a).

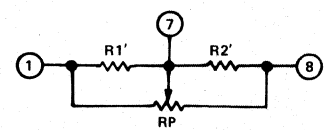


Figure 2a. High Resolution, High Stability Nulling Circuit

NULLING PROCEDURE

1. Null the offset to zero using a commercially available pot (suggest R_P = 10kΩ).
2. Measure pot halves R1 and R2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}, \quad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Insert R1′ and R2′ (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (R_P) to fine tune the trim.

For applications in which stringent nulling is not required, the user may choose a simplified nulling scheme as shown in Figure 2b. For best results the wiper of the potentiometer should be connected directly to pin 7 of the op amp. This is true for both nulling schemes.

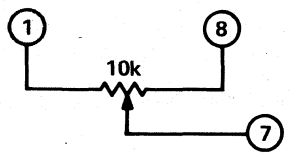


Figure 2b. Simplified Nulling Circuit

INPUT BIAS CURRENT

The input bias current vs. temperature characteristic is displayed in Figure 3.

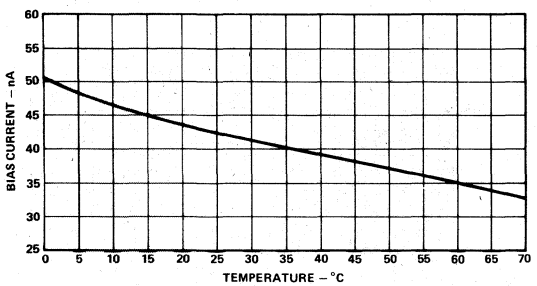


Figure 3. Input Bias Current vs. Temperature

GAIN PERFORMANCE

Most commercially available monolithic op amps have gain characteristics that vary considerably with:

1. Offset Nulling.
2. Load Resistance.
3. Supply Voltage.

Careful design allows the AD504 to maintain gain well in excess of 10^6, independent of nulling, load or supply voltage.

Nulling – The gain of a 741 op amp varies considerably with nulling (see Figure 4).

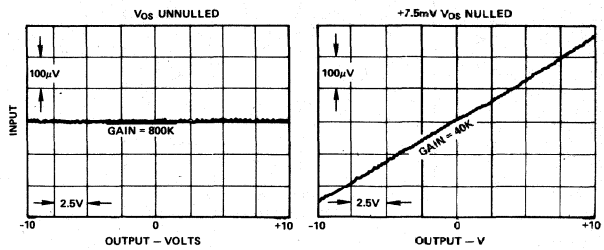


Figure 4. Gain Error Voltage Before and After Nulling a Typical 741 Op Amp

The gain of the AD504 is independent of nulling.

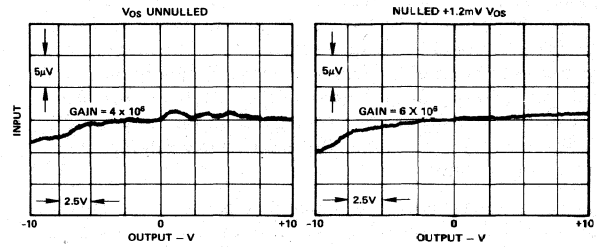


Figure 5. Gain Error Voltage Before and After Nulling the AD504

Load Resistance – The gain of the AD504 is flat with load resistance to 1kΩ loads and below.

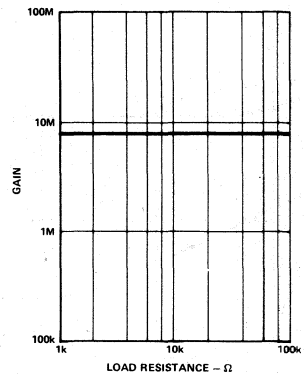


Figure 6. Gain vs. Load Resistance

Supply Voltage – The gain of the AD504 stays well above 1M down to V_S = ±5V.

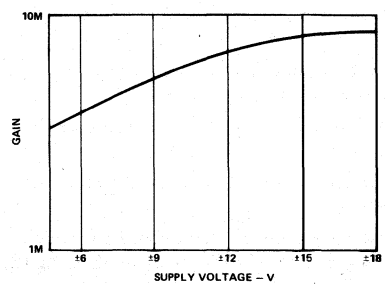


Figure 7. Gain vs. Supply Voltage

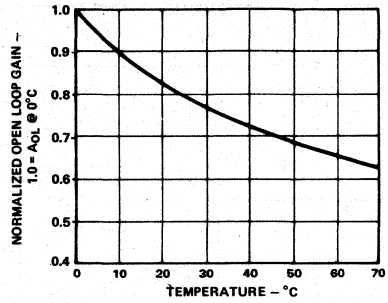


Figure 8. Normalized Open Loop Gain vs. Temperature

NOISE CHARACTERISTICS

An op amp with the precision of the AD504 must have correspondingly low noise levels if the user is to take advantage of its exceptional dc characteristics. Of primary importance in this type of amplifier is the absence of popcorn noise and minimum I/f or "flicker" noise in the 0.01Hz to 10Hz frequency band. Sample noise testing is done on every lot to guarantee that better than 90% of all devices will meet the noise specifications.

Separate voltage and current noise levels referred to the input are specified to enable the designer to calculate or optimize signal-to-noise ratio based on any desired source resistance. The spot noise figures are useful in determining total wideband noise over any desired bandwidth (see Figure 9).

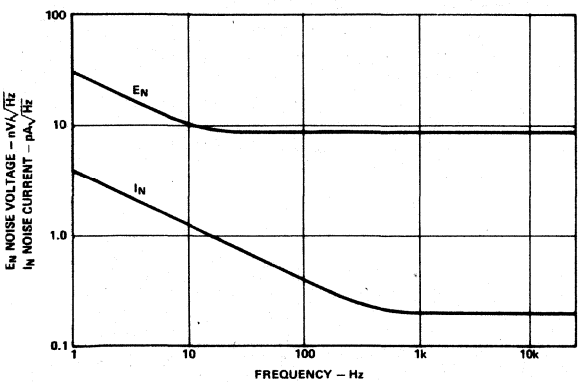


Figure 9. Spot Noise vs. Frequency

The key to success in using the AD504 in precision low noise applications is "attention to detail".

Here are a few reminders to help the user achieve optimum noise performance from the AD504.

1. Use metal film resistors in the source and feedback networks.
2. Use fixed resistors instead of potentiometers for nulling or gain setting.
3. Take advantage of the excellent common-mode noise rejection qualities of the AD504 by connecting the input differentially.
4. Limit the bandwidth of the system to the minimum possible consistent with the desired response time.
5. Use input guarding to reduce capacitive and leakage noise pickup.
6. Avoid ground loops and proximity to strong magnetic or electrostatic fields, etc.

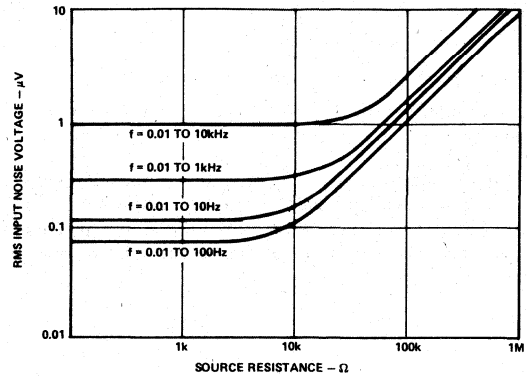


Figure 10. RMS Noise vs. Source Resistance

DYNAMIC PERFORMANCE

The dynamic performance of the AD504, although comparable to most general purpose op amps, is superior to most low drift op amps. Figure 11 shows the small signal frequency response for both open and closed loop gains for a variety of compensating values. Note that the circuit is completely stable for C_C = 390pF with a -3dB bandwidth of 300kHz; with C_C = 0, the -3dB bandwidth is 50kHz at a gain of 2000.

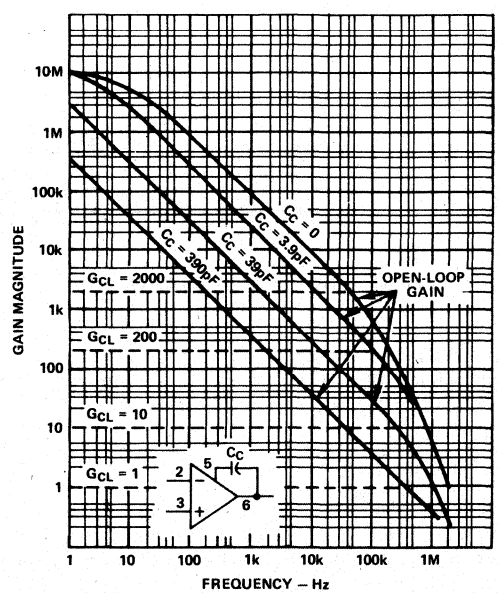


Figure 11. Small Signal Gain vs. Frequency

More important, at unity gain (390pF), full power bandwidth is (Figure 12) 2kHz which corresponds to a 0.12V/μs slew rate. At a gain of 10 (39pF), it increases to 20kHz, corresponding to 1.2V/μs, a considerable improvement over "725 type" amplifiers.

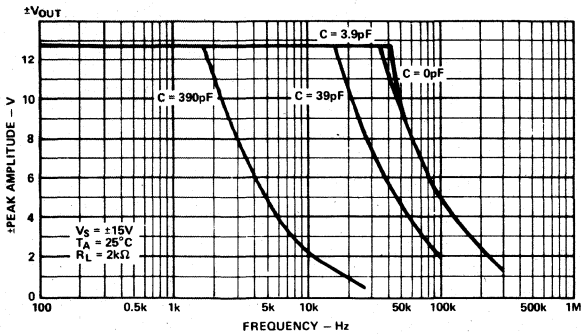


Figure 12. Output Voltage Swing vs. Frequency

Figure 13 shows the voltage follower step response for $V_S = \pm 15V$, $R_L = 2k\Omega$, $C_L = 200pF$ and $C_C = 390pF$.

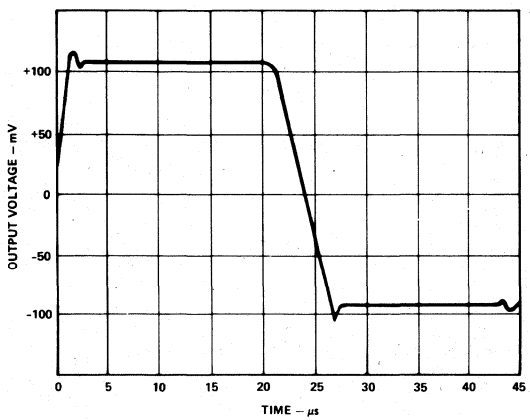


Figure 13. Voltage Follower Step Response

The common mode rejection of the AD504 is typically 120dB, and is shown as a function of frequency in Figure 14.

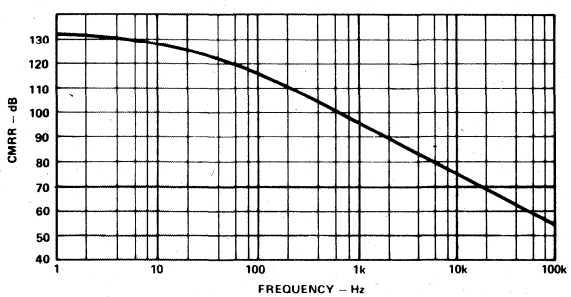


Figure 14. CMRR vs. Frequency

The power supply rejection ratio of the AD504 is shown in Figure 15.

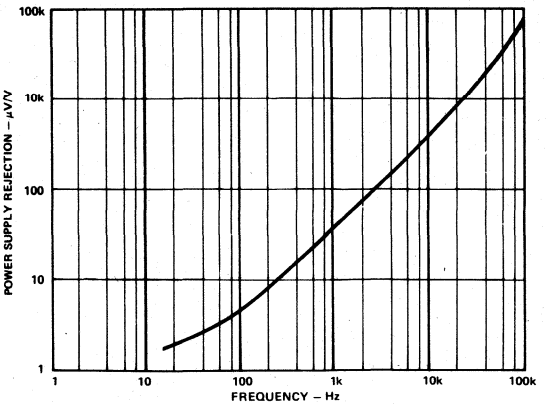


Figure 15. PSRR vs. Frequency

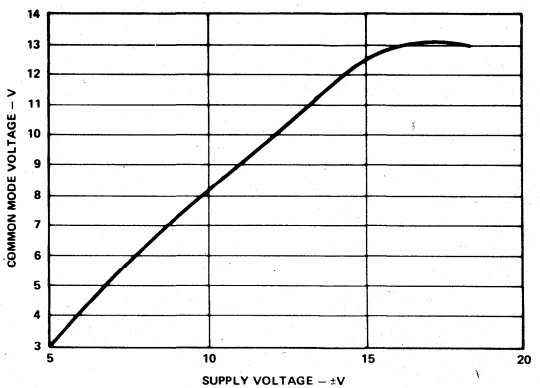


Figure 16. CMV Range vs. Supply Voltage

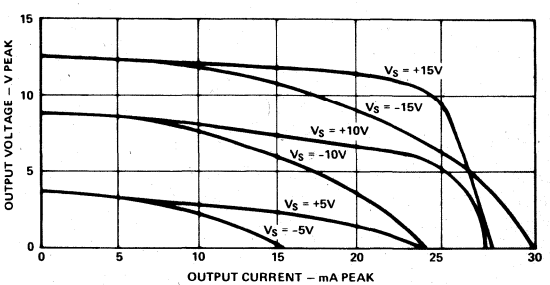


Figure 17. Output Characteristics

THERMAL PERFORMANCE

Temperature Gradients

Most modular and hybrid operational amplifiers are extremely sensitive to thermal gradients. The transient offset voltage response to thermal shock for a high performance modular op amp is shown in Figure 18.

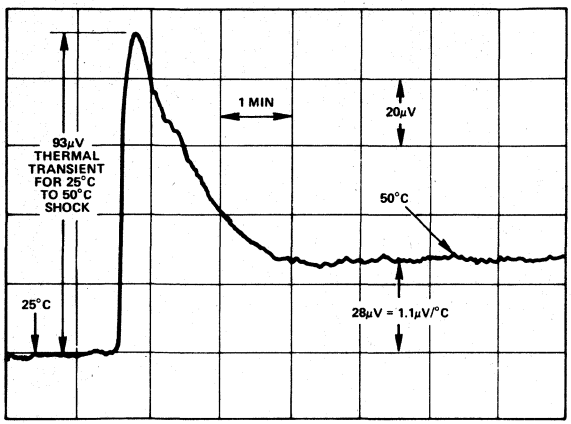


Figure 18. Response to Thermal Shock for High Performance Modular Op Amp

The graph shows the transient offset voltage resulting from a thermal shock when the amplifier's temperature is abruptly changed from 25°C to 50°C by dipping it into a hot silicon oil bath. Note the large overshoot (approximately 60μV) and long settling time (2.5 minutes). Also note the hysteresis of about 30μV.

Monolithic technology affords the AD504 significant improvements in this area. Thermal transients in the AD504 are small and over with quickly (see Figure 19).

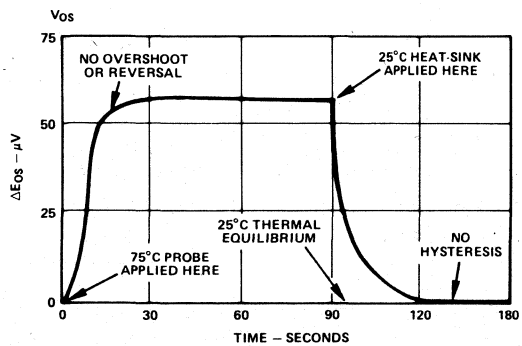


Figure 19. Response to Thermal Shock for AD504

In Figure 19, a 50°C step change in ambient temperature, applied to the can via a room temperature heat sink, then a 75°C thermal probe and back to the heat sink, results in settling to the final value within 30 seconds, for both increases and decreases in temperature. Note that the offset goes directly to its final value, with no spikes or hysteresis.

Warmup Drift

Modular and hybrid op amps have historically been plagued by excessive thermal time constants. Figure 20 shows the typical warmup drift of a high performance modular op amp.

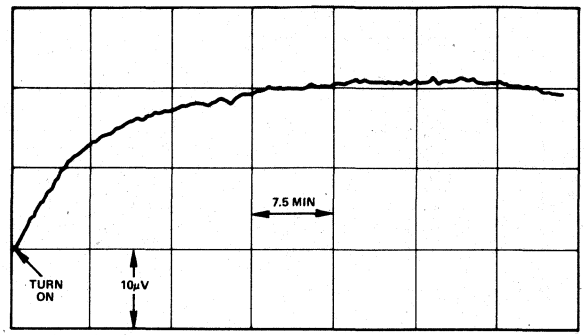


Figure 20. Warmup Voltage Drift for High Performance Modular Op Amp

Note that although warmup drift is low (20μV), it requires a long time to settle (>20 minutes).

Monolithic technology results in significant reduction of thermal time constants (see Figure 21).

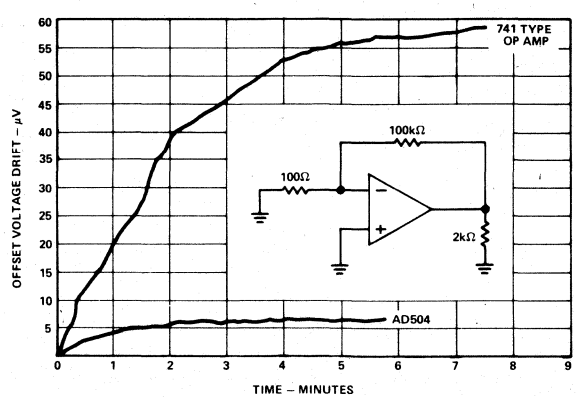


Figure 21. Warmup Voltage Drift for AD504 and 741 Type Op Amp

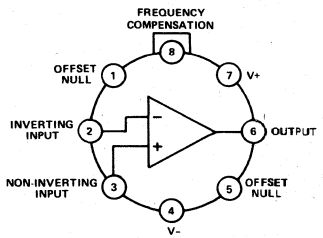
Note that warmup drift remains low (10μV), but that the thermal time constant decreases significantly to about 2 minutes. If a heat sink were used, total settling time would be completed within 30 seconds. Note that the 741 type op amp has a significantly longer warmup drift and thermal time constant.

IC, Wideband, Fast Slewing, General Purpose Operational Amplifier

AD507

FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive

AD507 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the extended temperature range, -55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

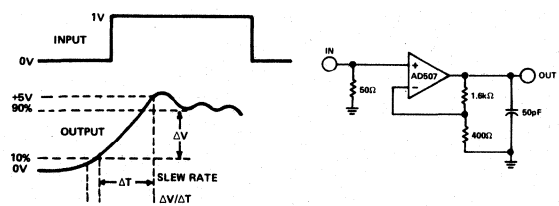
PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.

SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T min to T max	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	12nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Operating	−25°C to +85°C	*	−65°C to +150°C
Storage	−65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08A)	AD507JH	AD507KH	AD507SH

NOTES
*Specifications same as AD507J.
[1] See Section 19 for package outline information.
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V- 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

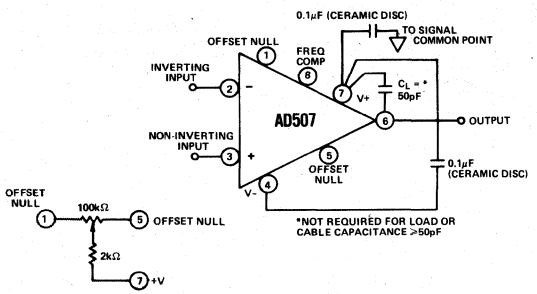


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

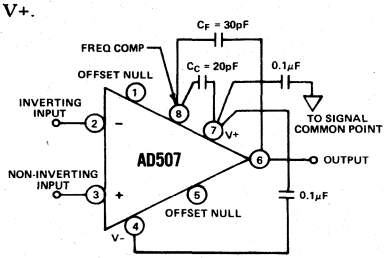


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

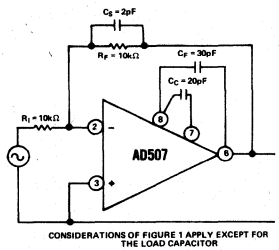
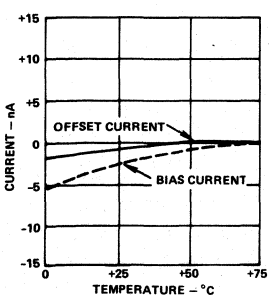
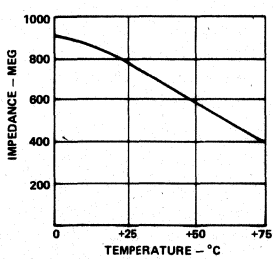


Figure 3. Fast Settling Time Configuration

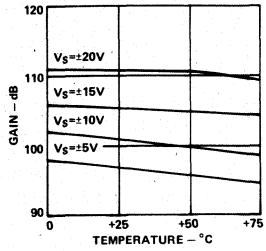
TYPICAL PERFORMANCE CURVES



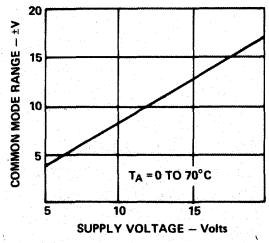
Input Bias Current and Offset Current vs Temperature



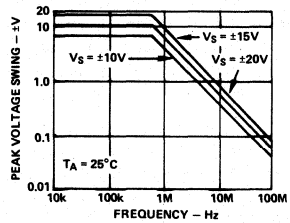
Input Impedance vs Temperature



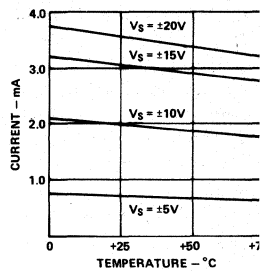
Open Loop Voltage Gain vs Temperature



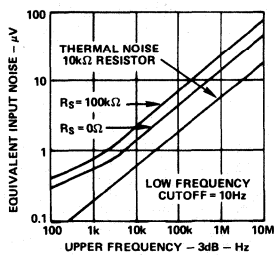
Common Mode Voltage Range vs Supply Voltage



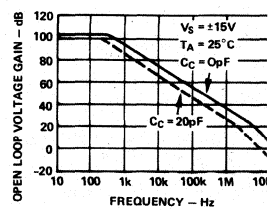
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

AD509

FEATURES

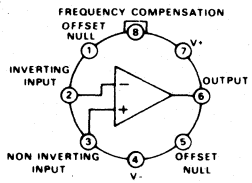
Fast Settling Time
- **0.1% in 500ns max**
- **0.01% in 2.5μs max**

High Slew Rate: 100V/μs min
Low I_{OS}: 25nA max
Guaranteed V_{OS} Drift: 30μV/°C max
High CMRR: 80dB min
Drives 500pF

APPLICATIONS

D/A and A/D Conversion
Wideband Amplifiers
Multiplexers
Pulse Amplifiers

AD509 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
2. The AD509 will drive capacitive loads of 500pF without deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
3. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.
4. The AD509K and AD509S are 100% tested for minimum slew rate and guaranteed to settle to 0.01% of its final value in less than 2.5μs.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

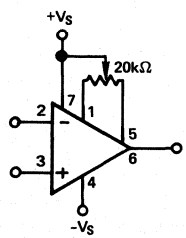
Model	AD509J Min	AD509J Typ	AD509J Max	AD509K Min	AD509K Typ	AD509K Max	AD509S Min	AD509S Typ	AD509S Max	Units
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**75,000**	15,000		**10,000**	15,000		**10,000**	15,000		V/V
T_{min} to T_{max}, R_L = 2kΩ	5,000			7,500			**7,500**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		V
FREQUENCY RESPONSE										
Unity Gain Small Signal		20			20			20		MHz
Full Power Response	1.2	1.6		1.5	2.0		1.5	2.0		MHz
Slew Rate, Unity Gain	80	120		80	120		100	120		V/µs
Settling Time										
to 0.1%		200			200			200	500	ms
to 0.01%		1.0			1.0			1.0	2.5	µs
INPUT OFFSET VOLTAGE										
Initial Offset		5	**10**		4	**8**		4	**8**	mV
Input Offset Voltage T_{min} to T_{max}			14			11			**11**	mV
Input Offset Voltage vs. Supply,										
T_{min} to T_{max}			**200**			**100**			**100**	µV/V
INPUT BIAS CURRENT										
Initial		125	**250**		100	**200**		100	**200**	nA
T_{min} to T_{max}			500			400			**400**	nA
INPUT OFFSET CURRENT										
Initial		20	50		10	25		10	25	nA
T_A = min to max			100			50			50	nA
INPUT IMPEDANCE										
Differential	40	100		50	100		50	100		MΩ
INPUT VOLTAGE RANGE										
Differential		±15			±15			±15		V
Common Mode		±10			±10			±10		V
Common Mode Rejection	**74**	90		**80**	90		**80**	90		dB
INPUT NOISE VOLTAGE										
f = 10Hz		100			100			100		nV/√Hz
f = 100Hz		30			30			30		nV/√Hz
f = 100kHz		19			19			19		nV/√Hz
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±20	±5		±20	±5		±20	V
Quiescent Current		4	**6**		4	**6**		4	**6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	−55		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE[1]										
TO-99 Style (H08A)		AD509JH			AD509KH			AD509SH		

NOTES

[1]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Simplified Nulling Circuit

APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

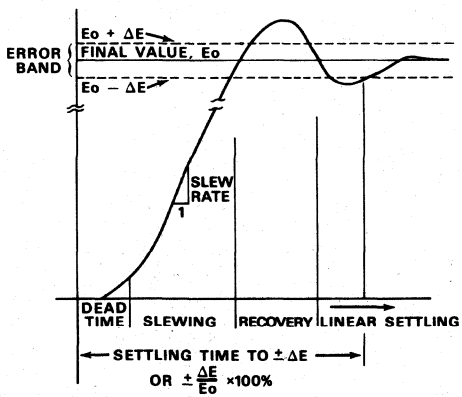


Figure 1. Settling Time

The AD509K and AD509S are guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs when tested as shown in Figure 2. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope display. The resultant waveform of ($E_O - E_{IN}$) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

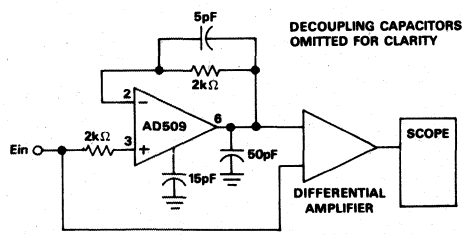


Figure 2. AD509 Settling Time Test Circuit

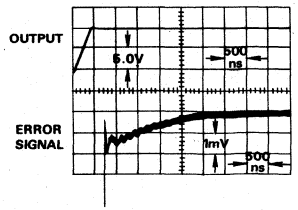


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

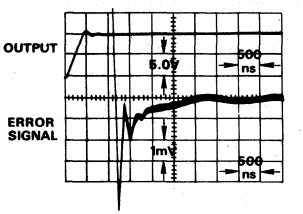


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are.....

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

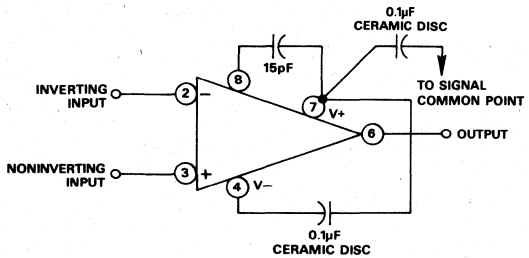


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

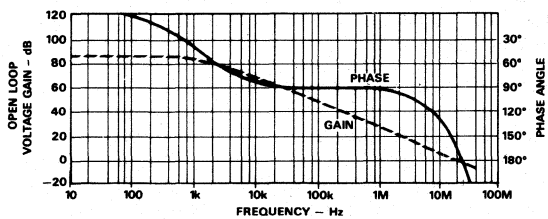


Figure 6. Open Loop Frequency and Phase Response

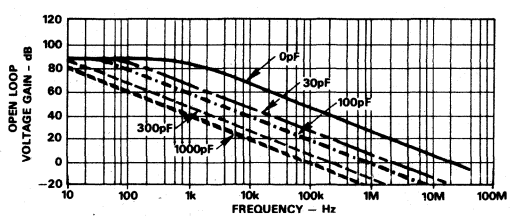


Figure 7. Open Loop Frequency Response for Various C_C's

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST CURRENT-OUTPUT D-TO-A CONVERTERS

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-to-voltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_s \text{ TOTAL} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to ±0.1% or ±0.01% of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

Figure 8 shows the AD509K connected as an output amplifier with the AD565K, high speed 12-bit IC digital-to-analog converter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.

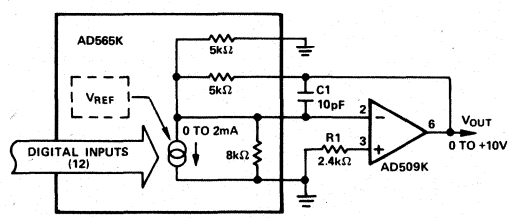


Figure 8. AD509 as an Output Amplifier for a Fast Current-Output D-to-A Converter

ANALOG DEVICES

Low Cost, Laser Trimmed, Precision IC Op Amp

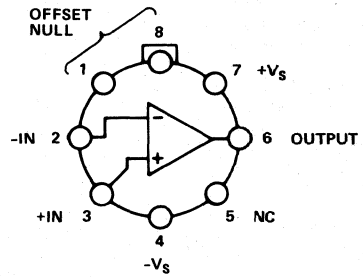
AD510

4

FEATURES

Low V_{OS}: 25μV max (AD510L), 100μV max (AD510J)
Low V_{OS} Drift: 0.5μV/°C max (AD510L)
Internally Compensated
High Open Loop Gain: 10^6 min
Low Noise: 1μV p-p 0.01 to 10Hz

AD510 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD510 is the first low cost high accuracy IC op amp available. Analog Devices' precise thermally-balanced layout combined with high-yield IC processing provides truly superlative op amp performance at the lowest possible cost. The device is internally compensated, thus eliminating the need for an additional external capacitor.

A truly precision device, the AD510 achieves laser trimmed offset voltages less than 25μV max and offset voltage drifts of 0.5μV/°C max (nulled). Bias currents and offset currents are available at less than 10nA and 2.5nA respectively, while open loop gain is maintained at over 1,000,000, even under loaded conditions. Designed along a thermal axis, the AD510 is unaffected by thermal gradients across the monolithic chip caused by current loading.

The AD510 has fully protected inputs, permitting differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits and drives 1000pF of load capacitance without oscillation.

The AD510 is specifically designed for applications requiring high precision at the lowest possible cost, such as bridge instruments, stable references, followers and analog computation. Packaged in a hermetically-sealed TO-99 metal can, the AD510 is available in three versions of performance (J, K and L) over the commercial temperature range, 0 to +70°C and one version (S) over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage drift is guaranteed and 100% tested on all models with a controlled temperature drift bath with the offset voltage nulled. Offset voltage on the AD510L is tested following a 3 minute warm-up.
2. The AD510 offers fully protected input (to $\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, a critical factor in high accuracy op amps where overall performance is strongly dependent on front-end stability.
3. Internal compensation eliminates the need for elaborate and costly stabilizing networks, often required by many high accuracy IC op amps.
4. A thermally balanced layout maintains high gain (1,000,000 min, K, L and S) independent of offset nulling, power supply voltage and output loading.
5. Bootstrapping of critical input transistors produces CMRR and PSRR of 110dB min and 100dB min, respectively.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD510JH	AD510KH	AD510LH	AD510SH
OPEN LOOP GAIN				
V_{OS} = ±10V, $R_L > 2k\Omega$	250,000 min	10^6 min	**	**
T_{min} to T_{max}	125,000 min	500,000 min	**	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	300kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leq 10k\Omega$	100μV max	50μV max	25μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.0μV/°C max	0.5μV/°C max	**
vs. Supply	25μV/V max	10μV/V max	**	**
T_{min} to T_{max}	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	5nA max	4nA max	2.5nA max	**
T_{min} to T_{max}	8nA max	6nA max	4nA max	10nA max
INPUT BIAS CURRENT				
Initial	25nA max	13nA max	10nA max	**
T_{min} to T_{max}	40nA max	20nA max	15nA max	30nA max
vs. Temp, T_{min} to T_{max}	±100pA/°C	±50pA/°C	±40pA/°C	**
INPUT IMPEDANCE				
Differential	4MΩ	6MΩ	**	**
Common Mode	100MΩ‖4pF	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	1μV p-p	*	*	*
f = 10Hz	$18nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$13nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$10nV/\sqrt{Hz}$	*	*	*
Current, f = 10Hz	$0.5pA/\sqrt{Hz}$	*	*	*
f = 100Hz	$0.3pA/\sqrt{Hz}$	*	*	*
f = 1kHz	$0.3pA/\sqrt{Hz}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTIONS:[1] TO-99 Style (H08B)	AD510JH	AD510KH	AD510LH	AD510SH

NOTES

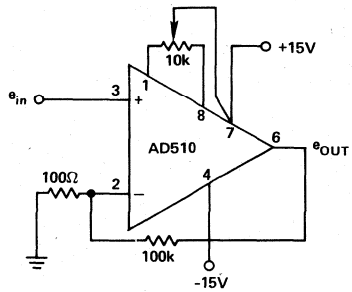
*Specifications same as AD510JH.

**Specifications same as AD510KH.

[1] See Section 19 for package outline information.

Specification subject to change without notice.

TYPICAL
NON-INVERTING AMPLIFIER CONFIGURATION



NULLING THE AD510

Nulling the AD510 can be achieved using the high resolution circuit of Figure 1.

1. Null the offset to zero using a commercially available pot (approximately 10kΩ).
2. Measure pot halves, R_1 and R_2.
3. Calculate . . . $R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}$ $R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$
4. Insert R_1' and R_2' (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (r_p) to fine tune the trim.

Nulling to within 1 microvolt can be achieved using this technique. For best results, the wiper of the potentiometer should be connected directly to pin 7 of the op amp.

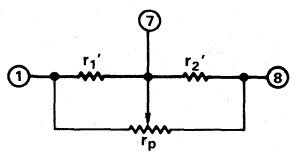


Figure 1. High Resolution, High Stability Nulling Circuit

THE AD510L IN A SIMPLE INSTRUMENTATION AMPLIFIER

The circuit of Figure 2 illustrates a simple instrumentation amplifier suitable for use with strain gauges, thermocouples and other transducers. It provides high input impedance to ground at each of the differential input terminals and excellent common mode rejection.

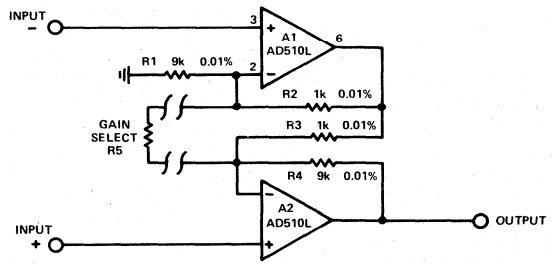


Figure 2. Instrumentation Amplifier

The configuration shown is designed for a gain of 10, however the gain can be varied upwards by adding a gain select resistor R_5. In operation, amplifier A_1 provides a gain of 10/9 for signals at the negative input terminal. This output feeds the inverting amplifier A_2, which has a gain of 9, resulting in an overall gain of 10. For signals at the positive input, the output of A_1 is at ground potential and the amplifier A_2 provides a gain of 10. Thus, the circuit has a gain of 10 for differential signals and 0 for common mode signals; the very high CMRR and open loop gain of the AD510L automatically produces common mode rejection of at least 25,000 at dc at a gain of 10 and over 1,000,000 at a gain of 1000. The common mode rejection, of course, depends upon the resistor ratios and their specified tolerance. Less accurate resistors can be used if the network is trimmed.

For gains of 10 the frequency response is down 3dB at 500kHz, for gains of 1000, 2kHz. Full output of ±10V can be attained up to 1800Hz.

The common mode rejection at 60Hz is limited by the finite gain bandwidth of A_1 causing a phase lag on the negative input signal. At 60Hz the CMRR measures 72dB at a gain of 1000 and 62dB at a gain of 10.

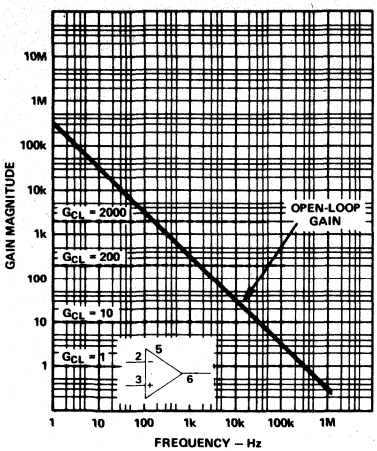


Figure 3. Small Signal Gain vs. Frequency

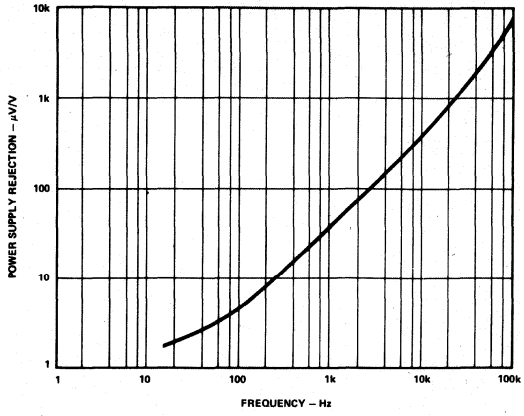


Figure 4. PSRR vs. Frequency

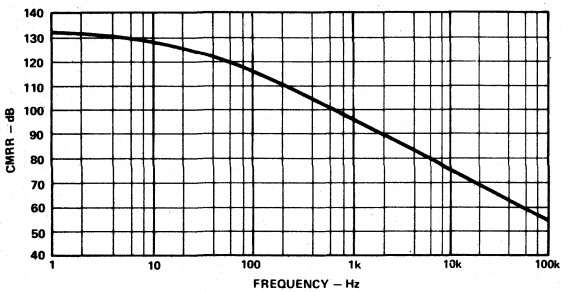


Figure 5. CMRR vs. Frequency

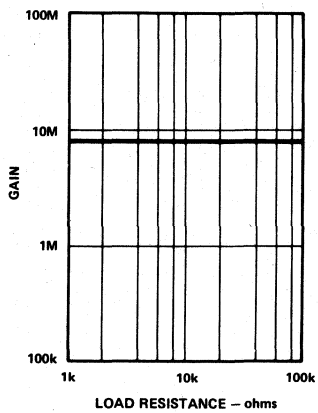


Figure 6. Gain vs. Load Resistance

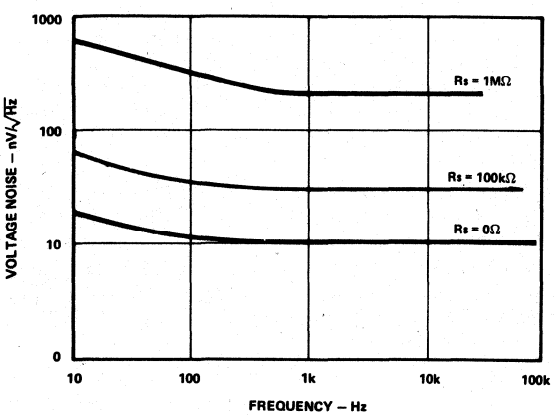


Figure 7. Voltage Noise vs. Frequency

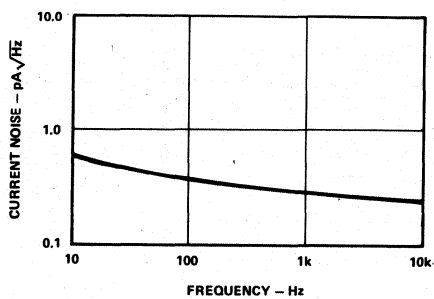


Figure 8. Current Noise vs. Frequency

ANALOG DEVICES

Precision, Low-Power FET-Input Electrometer Op Amp

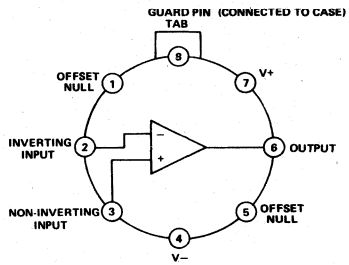
AD515

4

FEATURES

- **Ultra Low Bias Current:** 0.075pA max (AD515L)
  0.150pA max (AD515K)
  0.300pA max (AD515J)
- **Low Power:** 1.5mA max Quiescent Current
  (0.8mA typ)
- **Low Offset Voltage:** 1.0mV max (AD515 K & L)
- **Low Drift:** 15μV/°C max (AD515K)
- **Low Noise:** 4μV p-p, 0.1 to 10Hz
- **Low Cost**

AD515 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD515 series of FET-input operational amplifiers are second generation electrometer designs offering the lowest input bias currents available in any standard operational amplifier. The AD515 also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultra-low bias current circuits. All devices are internally compensated, free of latch-up, and short circuit protected.

The AD515 delivers a new level of versatility and precision to a wide variety of electrometer and very high impedance buffer measurement situations, including photo-current detection, vacuum ion-gauge measurement, long term precision integration, and low drift sample/hold applications. The device is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515 with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The 10^{15} ohm common mode input impedance, resulting from a solid bootstrap input stage, insures that the input bias current is essentially independent of common mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD515 is available in three versions of bias current and offset voltage, the "J", "K", and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The AD515 provides the lowest bias currents available in an integrated circuit amplifier.
   - The ultra low input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15 volt supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±5 volt supplies, input bias current can typically be brought below 50fA.
2. The input offset voltage on all grades is laser trimmed to a level typically less than 500μV.
   - The offset voltage drift is the lowest available in an FET electrometer amplifier.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per millivolt nulled).
3. The low quiescent current drain of 0.8mA typical and 1.5mA maximum, which is among the lowest available in operational amplifier designs of any type, keeps self-heating effects to a minimum and renders the AD515 suitable for a wide range of remote probe situations.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one Megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristic.

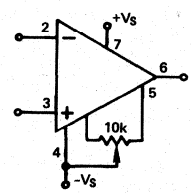
SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD515J Min	AD515J Typ	AD515J Max	AD515K Min	AD515K Typ	AD515K Max	AD515L Min	AD515L Typ	AD515L Max	Units
OPEN LOOP GAIN[1]										
V_O = ±10V, $R_L \geq 2k\Omega$	**20,000**			**40,000**			**25,000**			V/V
V_O = ±10V, $R_L \geq 10k\Omega$	**40,000**			**100,000**			**50,000**			V/V
T_{min} to T_{max}, R_L = 2kΩ	**15,000**			**40,000**			**25,000**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		V
Load Capacitance[2]		1000			1000			1000		pA
Short Circuit Current	**10**	25	**50**	**10**	25	**50**	**10**	25	**50**	mA
FREQUENCY RESPONSE										
Unity Gain Small Signal		350			350			350		MHz
Full Power Response	5	16		5	16			5		MHz
Slew Rate, Unity Gain	0.3	1.0		0.3	1.0		0.3	1.0		V/μs
Overload Recover, Inverting Unity Gain		16	100		16	100		16	100	μs
INPUT OFFSET VOLTAGE[3]										
Initial Offset		0.4	**3.0**		0.4	**1.0**		0.4	**1.0**	mV
Input Offset Voltage vs. Temperature			**50**			**15**			**25**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}		50	**400**			**100**			**200**	μV/V
INPUT BIAS CURRENT										
Either Input[4]			**300**			**150**			**75**	FA
INPUT IMPEDANCE										
Differential		10^{13}‖1.6			10^{13}‖1.6			10^{13}‖1.6		MΩ‖pA
Common Mode		10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8		MΩ‖pA
INPUT VOLTAGE RANGE										
Differential[5]	±20			±20			±20			V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**66**	94		**80**			**70**			dB
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		4.0			4.0			4.0		μV p-p
f = 10Hz		75			75			75		$nV/\sqrt{Hz}$
f = 100Hz		55			55			55		$nV/\sqrt{Hz}$
f = 1Hz		50			50			50		$nV/\sqrt{Hz}$
Current, 0.1Hz to 10Hz		0.003			0.003			0.003		pA (p-p)
10Hz to 10kHz		0.01			0.01			0.01		pA (rms)
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	V
Quiescent Current		0.8	**1.5**		0.8	**1.5**		0.8	**1.5**	mA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE[6]										
TO-99 Style (H08B)		AD515JH			AD515KH			AD515LH		

NOTES
[1]Open Loop Gain is specified with or without nulling of V_{OS}.
[2]A conservative design would not exceed 750pF of load capacitance.
[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.3mA indefinitely without damage. See next page.
[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Standard Offset Null Circuit

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515 can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultra-low input currents of the AD515. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pick-up and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515 is brought out separately to pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

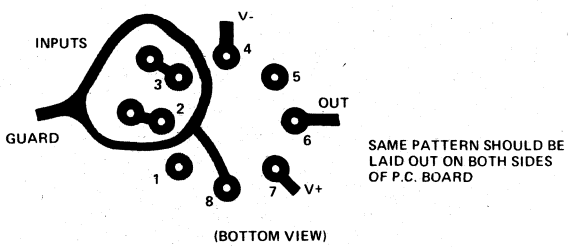


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515 can deliver. The best performance will be realized by using a teflon IC socket for the AD515; but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

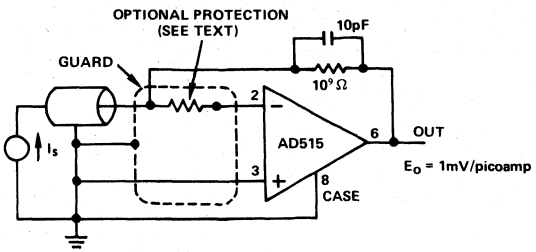


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

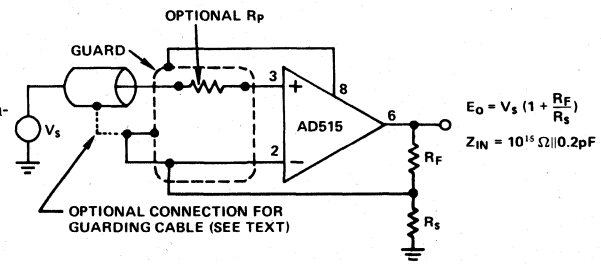


Figure 3. Very High Impedance Non-Inverting Amplifier

INPUT PROTECTION

The AD515 is guaranteed for a maximum safe input potential equal to the power supply potential. The unique bootstrapped input stage design also allows differential input voltages of up to ±20 volts (or within 10 volts of the sum of the supplies) while maintaining the full differential input resistance of $10^{13}\Omega$, as shown in Figure 10. This makes the AD515 suitable for low speed comparator situations employing a direct connection to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD515 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.5mA (for example, 200kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515 virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise, and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration-free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant will reduce the noise, but short rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other subjects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is normally about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will de-stabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Non-inverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may destabilize and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

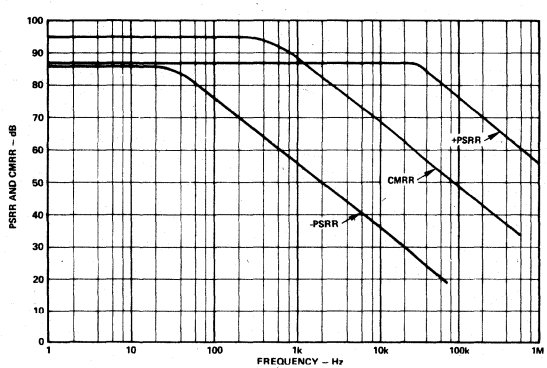


Figure 4. PSRR and CMRR Versus Frequency

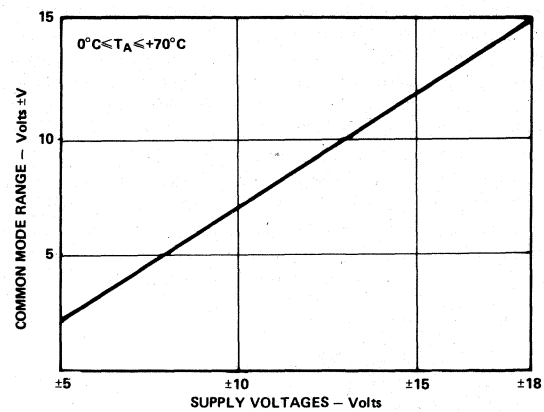


Figure 6. Input Common Mode Range Versus Supply Voltage

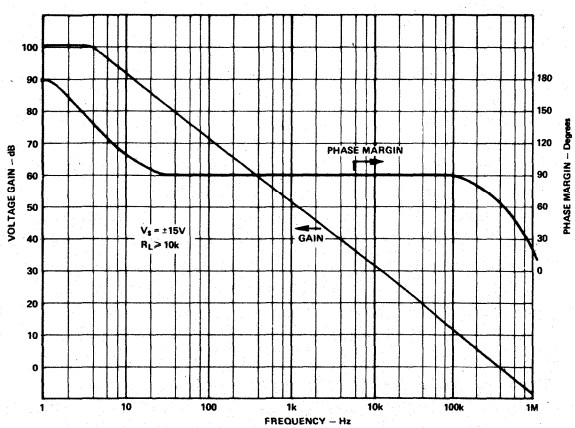


Figure 5. Open Loop Frequency Response

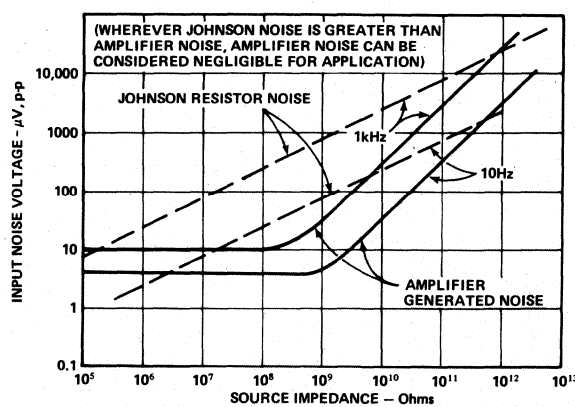


Figure 7. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515 offers the lowest input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515 and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515 has been reduced to a level much lower than that of any other electrometer-grade device, but additional performance improvement can be gained by lowering the supply voltages, to ±5 volts if possible. The effects of this are shown in Figure 8, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many dc performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load impedance to be at least 10kΩ.

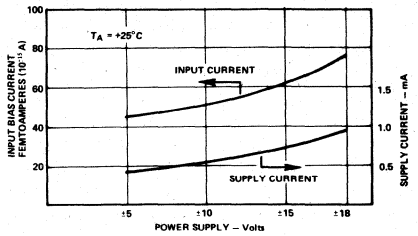


Figure 8. Input Bias Current and Supply Current Versus Supply Voltage

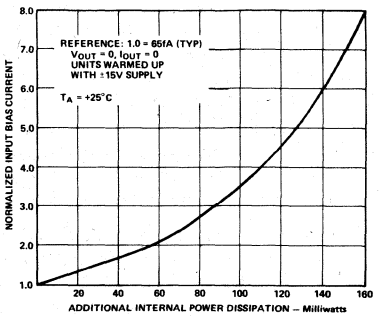


Figure 9. Input Bias Current Versus Additional Power Dissipation

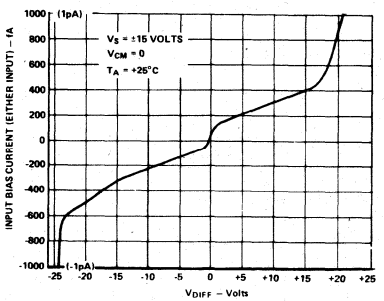


Figure 10. Input Bias Current Versus Differential Input Voltage

AD515 CIRCUIT APPLICATION NOTES

The AD515 is quite simple to apply to a wide variety of applications because of the pre-trimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High-megohm resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high-megohm resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515 is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515 are significant only above $10^{11}\Omega$.

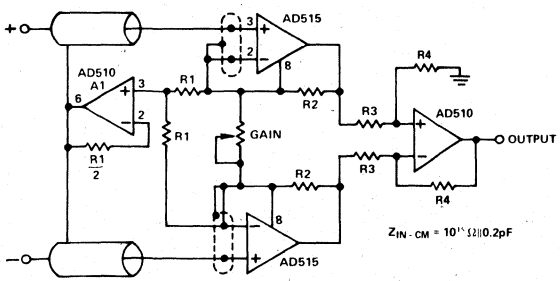


Figure 11. Very High Impedance Instrumentation Amplifier

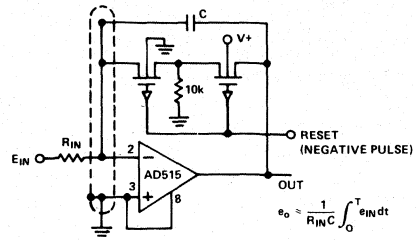


Figure 12. Low Drift Integrator and Low-Leakage Guarded Reset

LOW-LEVEL CURRENT TO VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515 makes the tradeoff easier.

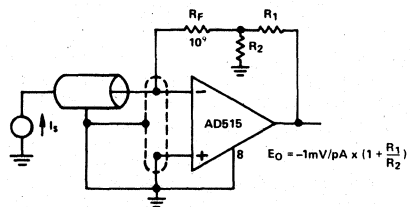


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the non-inverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD521 instrumentation amplifier converts the floating differential signal to a single-ended output.

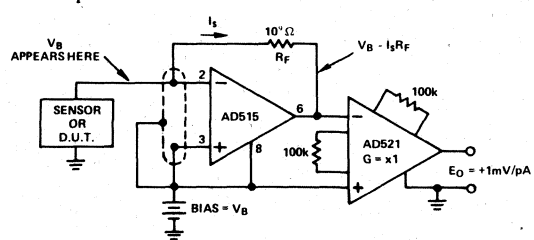


Figure 14. Current-to-Voltage Converters with Grounded Bias and Sensor

ANALOG DEVICES

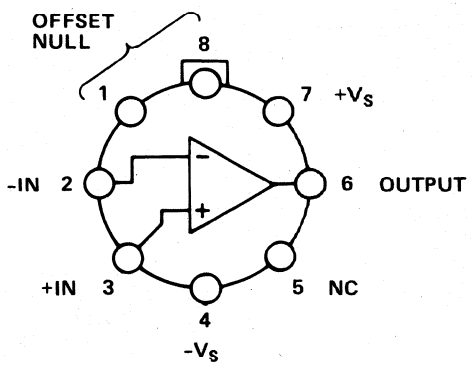
Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

Low Input Bias Current: 1nA max (AD517L)
Low Input Offset Current: 0.25nA max (AD517L)
Low V_{OS}: 50μV max (AD517L), 150μV max (AD517J)
Low V_{OS} Drift: 1.3μV/°C (AD517L)
Internal Compensation

AD517 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 50μV and offset voltage drifts less than 1.3μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

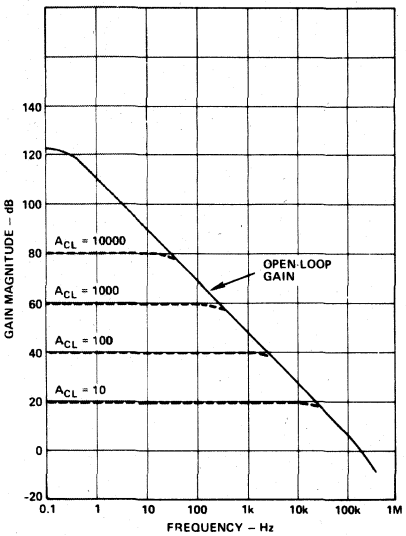
Model	AD517J			AD517K			AD517L			AD517S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**10^6**			**10^6**			**10^6**			**10^6**			V/V
T_{min} to T_{max}, R_L = 2kΩ	500,000			500,000			500,000			**250,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**			**±10**			**±10**			**±10**			V
Load Capacitance		1000			1000			1000			1000		pF
Output Current	10			10			10			10			mA
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		250			250			250			250		kHz
Full Power Response		1.5			1.5			1.5			1.5		kHz
Slew Rate, Unity Gain		0.10			0.10			0.10			0.10		V/μs
INPUT OFFSET VOLTAGE													
Initial Offset			**150**			**75**			**50**			**75**	μV
Input Offset vs. Temp.			3.0			**1.8**			**1.3**			**1.8**	μV/°C
Input Offset vs. Supply			**25**			**10**			**10**			**10**	μV/V
T_{min} to T_{max}			40			15			15			**20**	μV/V
INPUT BIAS CURRENT													
Initial			**5**			**2**			**1.0**			**2.0**	nA
T_{min} to T_{max}			**8**			3.5			1.5			**10**	nA
vs. Temp, T_{min} to T_{max}			±20			±10			±4			±10	pA/°C
INPUT OFFSET CURRENT													
Initial			**1.0**			**0.75**			**0.25**			**2.0**	nA
T_{min} to T_{max}			1.5			1.25			0.4			**10**	nA
INPUT IMPEDANCE													
Differential		15‖1.5			20‖1.5			20‖1.5			20‖1.5		MΩ‖pF
Common Mode		2.0×10^{11}			2.0×10^{11}			2.0×10^{11}			2.0×10^{11}		Ω
INPUT VOLTAGE RANGE													
Differential		±V_S			±V_S			±V_S			±V_S		V
Common Mode Rejection	**94**			**110**			**110**			**110**			dB
Common Mode Rejection													
T_{min} to T_{max}	94			110			100			**100**			dB
INPUT NOISE													
Voltage, 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		nV/√Hz
f = 100Hz		25			25			25			25		nV/√Hz
f = 1kHz		20			20			20			20		nV/√Hz
Current, f = 10kHz		0.05			0.05			0.05			0.05		pA/√Hz
f = 100Hz		0.03			0.03			0.03			0.03		pA/√Hz
f = 1kHz		0.03			0.03			0.03			0.03		pA/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**4**			**3**			**3**			**3**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	**0**		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[1]													
TO-99 Style (H08B)		AD517JH			AD517KH			AD517LH			AD517SH		

NOTES

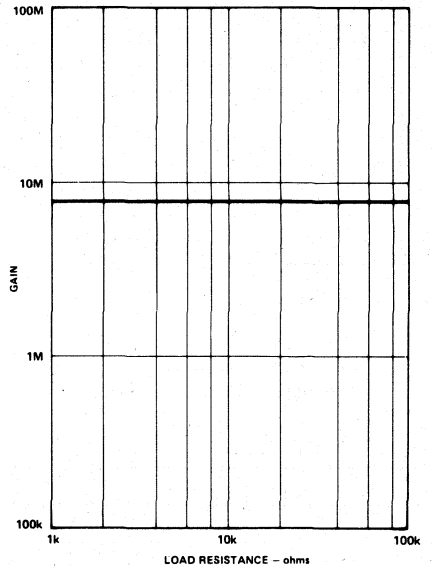
[1]See Section 19 for package outline information.

Specifications subject to change without notice.

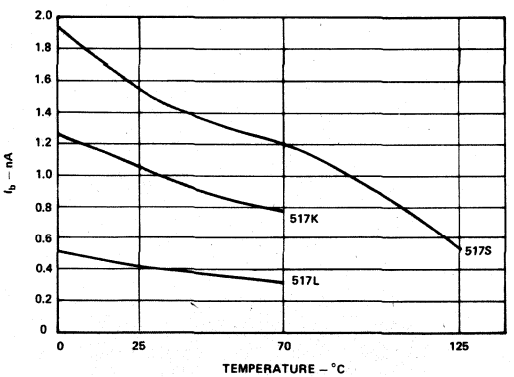
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



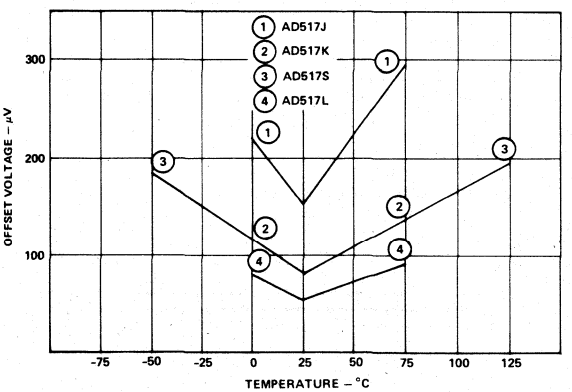
Small-Signal Gain vs. Frequency



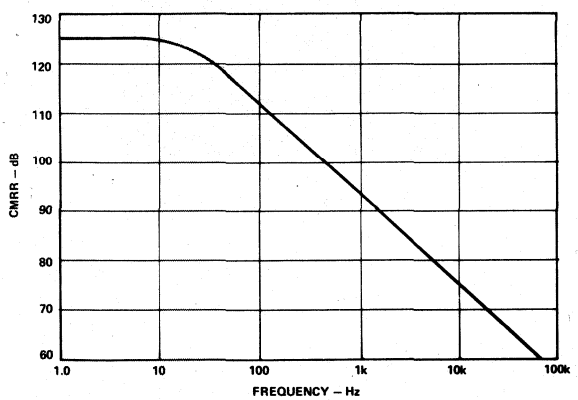
Open-Loop Gain vs. Load Resistance



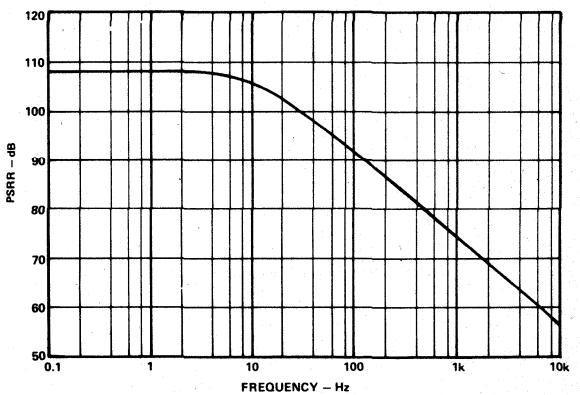
Input Bias Current vs. Temperature



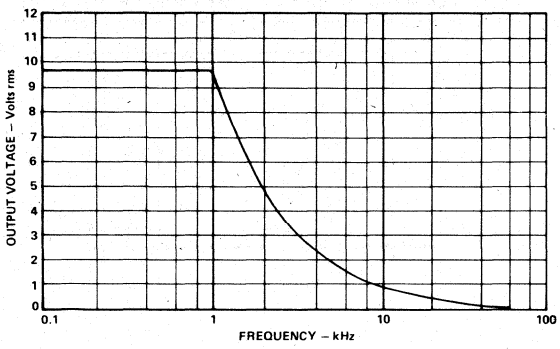
Untrimmed Offset Voltage vs. Temperature



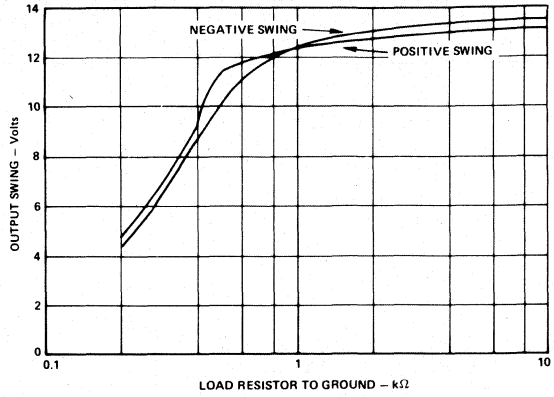
CMRR vs. Frequency



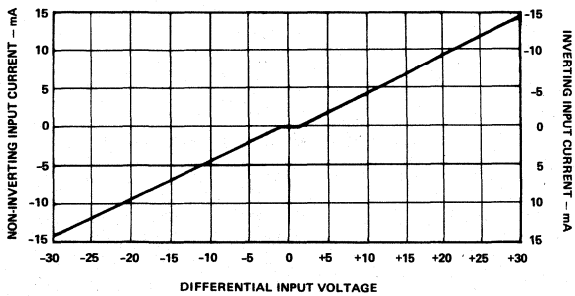
PSRR vs. Frequency



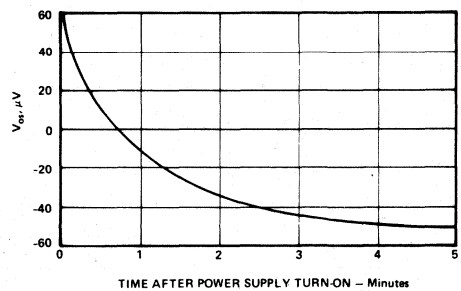
Maximum Undistorted Output vs. Frequency (Distortion ≤ 1%)



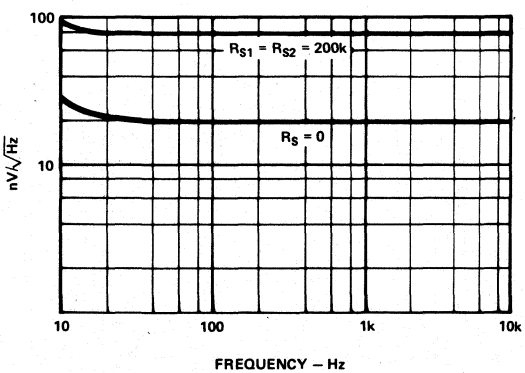
Output Voltage vs. Load Resistance



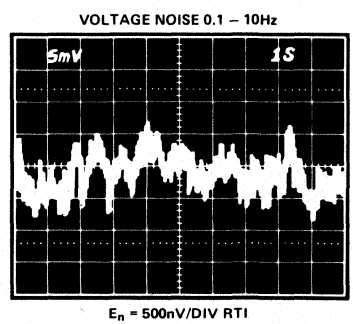
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

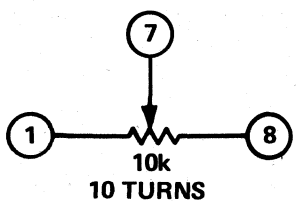
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

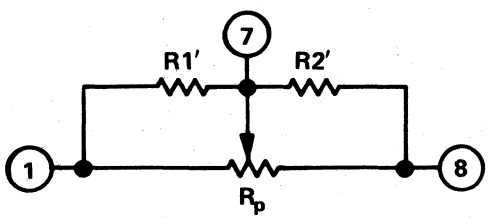
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega,}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

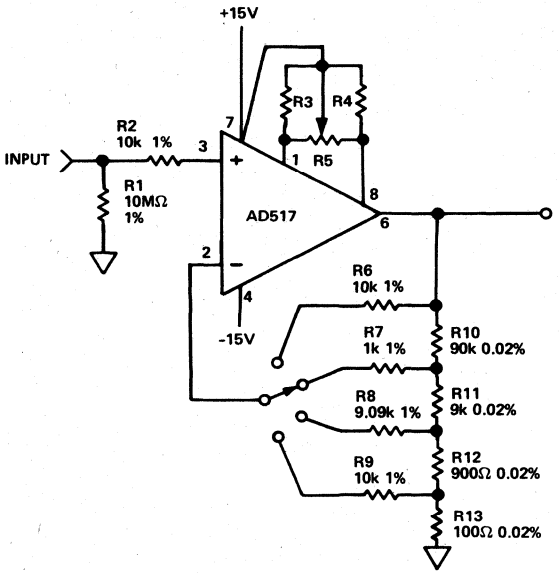


Figure 2. Stable Instrument Input Amplifier

Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

ANALOG DEVICES

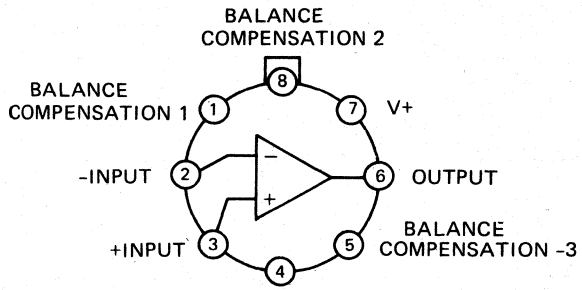
Low Cost, High Speed, IC Operational Amplifier

AD518

FEATURES

High Slew Rate: 70V/μs
Wide Bandwidth: 12MHz
60° Phase Margin (At Unity Gain Crossover)
Drives 300pF Load
Guaranteed Low Offset Drift:
15μV/°C Max (AD518K)
Pin Compatible With 118-Type Op Amp Series

AD518 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD518J, AD518K, and AD518S are high speed precision monolithic operational amplifiers designed for applications where slew rate and wide bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μs, and a typical bandwidth of 12MHz. In addition, in inverting applications external feedforward compensation may be added to increase the slew rate to over 100V/μs, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μs with a single external capacitor.

The AD518's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2mV, maximum offset drifts of 15μV/°C, and offset currents below 50nA max.

The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with D/A and A/D converters, as well as active filters, sample-and-hold circuits, and as a general purpose, fast, wideband amplifier. The AD518 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to +70°C temperature range; the AD518S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD518 offers the user high speed performance and flexibility previously unavailable at low cost . . . . . .
   - Internal compensation for unity gain applications
   - Capability to increase slew rate to over 100V/μs and double the bandwidth by an external feedforward technique
   - Capability to reduce settling time to under 1μs to 0.1% with a single external capacitor
   - Differential input capability
2. The phase margin of the AD518, uncompensated at the unity gain crossover frequency, is 60°, providing unconditional stability for all conditions. This conservative phase margin represents a clear improvement over that of the 118 series IC op amps currently available.
3. The static performance of the AD518 is consistent with its excellent dynamic performance, providing offset voltage drift under 15μV/°C, CMRR of 80dB, and offset current below 50nA.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD518J Min	AD518J Typ	AD518J Max	AD518K Min	AD518K Typ	AD518K Max	AD518S Min	AD518S Typ	AD518S Max	Units
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**25,000**	100,000		**50,000**	100,000		**50,000**	100,000		V/V
T_{min} to T_{max}, R_L = 2kΩ	20,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		V
Output Current		±10			±10			±10		mA
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain Small Signal		12			12			12		MHz
Slew Rate, Unity Gain	50	70		50	70		50	70		V/μs
Settling Time to 0.1%		800			800			800		ns
Phase Margin, Uncompensated at Unity Gain Crossover Frequency		60			60			60		Degrees
INPUT OFFSET VOLTAGE										
Initial Offset		4	**10**		2	**4**		2	**4**	mV
Input Offset Voltage or T_{min} to T_{max}			15			**6**			**6**	mV
Input Offset Voltage vs. Supply or T_{min} to T_{max}	**65**	80		**80**	90		**80**	90		dB
INPUT BIAS CURRENT										
Initial		120	**500**		120	**250**		120	**250**	nA
T_{min} to T_{max}			750			**400**			**400**	nA
INPUT OFFSET CURRENT										
Initial		30	**200**		6	**50**		6	**50**	nA
T_{min} to T_{max}			300			**100**			**100**	nA
INPUT IMPEDANCE	0.5	3.0		0.5	3.0		0.5	3.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential		±11.5			±11.5			±11.5		V
Common Mode		±V_S			±V_S			±V_S		V
Common Mode Rejection	**70**	100		**80**	100		**80**	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15	**±18**	V
Operating	±5		**±20**	±5		**±20**	±5		**±20**	V
Quiescent Current		5	**10**		5	**7**		5	**7**	μA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE[2]										
TO-99 Style (H08A)		AD518JH			AD518KH			AD518SH		
Plastic MINI DIP (N8A)		AD518JN			AD518KN					

NOTES

[1]The inputs are shunted with back-to-back diodes; if the differential input may exceed ± 1 volt, a resistor should be used to limit the input current to 10mA

[2]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

STABILITY & PHASE MARGIN

Perhaps one of the most meaningful ways to express the relative stability of a closed loop amplifier is in terms of phase margin. Phase margin is measured at that frequency where the open loop gain of the amplifier becomes unity or 0dB. It is the additional amount of phase shift that, if introduced in the loop, would make the loop unstable.

At very low frequencies the gain of most operational amplifiers is generally large. Moreover, the amplifier output signal is very nearly in phase with the differential input signal. This output is, therefore, nearly 180° out of phase with the feedback signal applied to the inverting input. At sufficiently high frequencies the gain of the amplifier begins to decrease as a function of frequency, with the resulting consequence of a lagging phase characteristic. That is, as the gain falls with increasing frequency, the phase of the output signal at a given frequency will lag the phase of the input signal. The phase shift depends most critically on the slope of the gain curve with respect to the logarithm of the frequency at the frequency where the phase is measured. If the gain changes more rapidly than 12dB/octave over a substantial frequency range, the minimum resulting phase shift may exceed 180°.

To insure amplifier stability, it is necessary that the phase shift near the unity gain frequency (12MHz in the AD518) is less than 180°. Moreover, it is generally required that the phase shift be substantially below the critical stability point to insure proper system performance. If the unity gain phase shift approaches 180°, the system will be on the verge of oscillation. As a result, there will be a large peak in the closed loop response near the unity loop gain frequency. This sharply peaked frequency response generally causes an undesirable small signal transient response with a poorly damped overshoot.

The term *phase margin* refers to the difference between 180° and the actual frequency-dependent phase shift at the system unity gain frequency. It is the margin between the actual system phase shift and the critical phase shift at which oscillation will occur. Not only does it indicate the relative immunity to oscillation, but it also gives some indication about the peaking and overshoot that can be expected.

The simple pole or frequency response of a single R-C network has a gain slope of 6dB/octave. This response has an associated phase shift which is asymptotic to −90°. Linear systems which are dominated by this characteristic in their open loop response are stable. They show no overshoot or ringing in their small signal transient response. Additional poles, either above or below the unity loop gain frequency, will add phase shift. As phase shift increases up to a lagging phase of about 120°, representing a 60° phase margin, little or no peaking will result. As the unity gain phase shift increases, peaking becomes more and more evident. For example, as the phase shift reaches 160° (20° of phase margin), between 9 and 10dB of peaking will occur.

The AD518 has been designed for a 60° phase margin at the unity gain crossover frequency, for absolute stability and absence of ringing and overshoot. (Note the transient response of the AD518 in Figure 1.) Note also in Figure 2 that the phase shift at 12MHz, the unity gain crossover frequency, is 120°, representing 60° of phase margin.

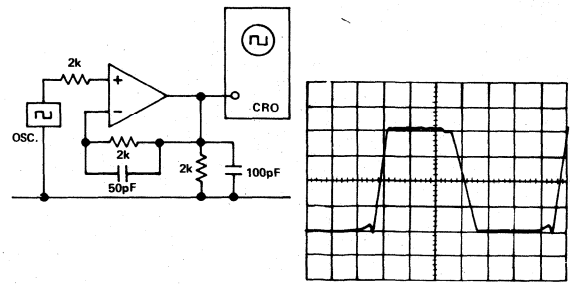


Figure 1. Transient Response of the AD518

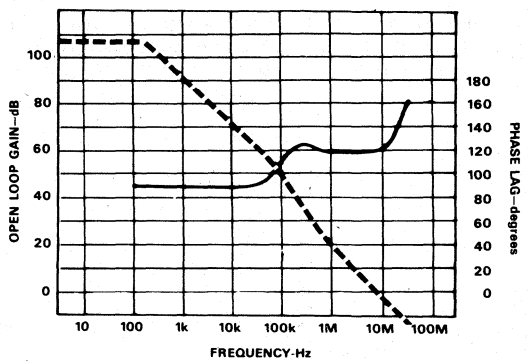


Figure 2. Amplitude and Phase Response of the AD518

THE FLEXIBILITY OF THE AD518

MINIMUM SETTLING TIME APPLICATIONS

For applications where a minimum settling time is desired, the settling time of the AD518 may be reduced significantly by employing the compensation scheme suggested in Figure 3.

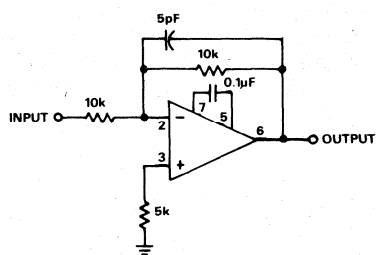


Figure 3. Minimum Settling Time Compensation

Using the 0.1μF capacitor from Pin 5 to V+ (Pin 7), the settling time to 0.1% is reduced from 2μs to 800ns.

HIGHER BANDWIDTH OR
HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD518 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 4.

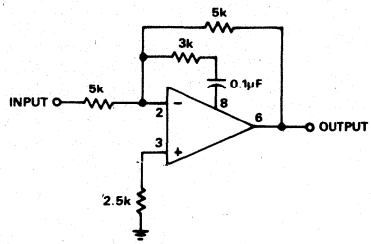


Figure 4. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD518 may be nearly doubled using the technique shown in Figure 5.

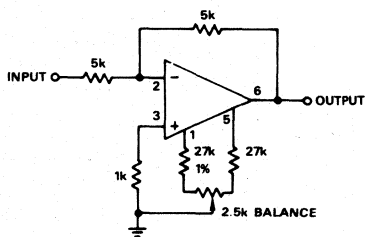


Figure 5. High Slew Rate Configuration

Note that the techniques of Figures 4 and 5 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/μs.

USING THE AD518

The connection scheme employed when using the AD518 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1μF bypass capacitors shown in Figure 6 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds, while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

When using the AD518, this decoupling configuration should be used in conjunction with the configuration of Figures 3, 4 and 5, depending on the specific application.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

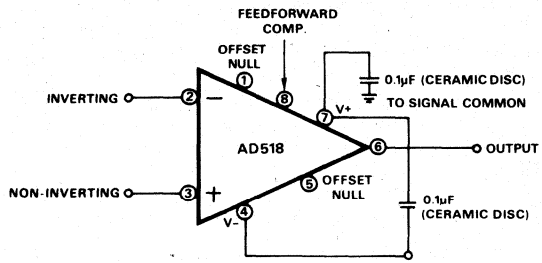
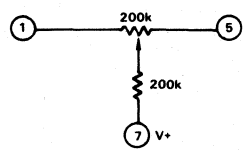


Figure 6. General Purpose Connection Diagram

NULLING THE AD518



OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

AD507	35MHz Gain Bandwidth Slew Rate of 25V/μs min Bias Current of 15nA max Offset Voltage Drift of 15μV/°C max
AD509	Settles to 0.01% in 1μs Settles to 0.1% in 200ns Slew Rate of 100V/μs min

ANALOG DEVICES

Precision Low Cost BIFET Op Amp

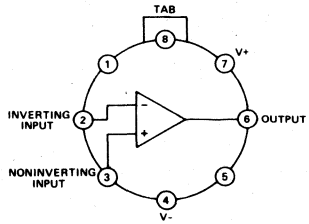
AD542

4

FEATURES

- Low Bias Current: 25pA max, warmed-up (AD542K,L), 50pA max (AD542J)
- Low Offset Voltage: 0.5mV max (AD542L), 1.0mV max (AD542K)
- Low Offset Voltage Drift: 5μV/°C max (AD542L), 10μV/°C max (AD542K) 20μV/°C max (AD542J)
- Low Quiescent Current: 1.5mA max
- Low Price

AD542 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD542 is a precision, monolithic FET-input operational amplifier fabricated with the most advanced BIFET and laser trimming technologies. The AD542 offers bias currents significantly lower than currently available BIFET devices: 25pA max, warmed-up for the AD542K and L, 50pA max for the AD542J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD542L and 1.0mV on the AD542K utilizing Analog's exclusive laser-wafer-trimming (LWT) process. When combined with the AD542's low offset voltage drift (5μV/°C max for "L", 10μV/°C max for "K"), these features offer the user IC performance truly superior to existing BIFET op amps – and at low, BIFET pricing.

The key to BI-FET technology is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. Analog Devices optimizes the BIFET process to produce bias currents lower than other popular BIFET op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1 – 10Hz), and low quiescent current.

The AD542 is recommended for any operational amplifier application requiring excellent dc performance at low and moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain—even under heavy loading—ensures better than "12-bit" linearity in high impedance buffer applications. Additionally, bandwidth and slew rate are much increased over presently available precision, bipolar op amps.

The AD542 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C extended operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved BIFET processing on the AD542 results in the lowest bias current available in a BIFET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD542 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD542L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (Offset voltage drift can increase an additional 3μV/°C per mV of offset nulled.)
5. Low voltage noise (2μV, p-p), and low offset voltage drift enhance the AD542's performance as a precision op amp.
6. The 1.5mA max quiescent current enables the device to be used in numerous portable applications where low battery drain is essential. This is achieved without sacrificing open loop gain or the ability to drive up to a 10mA load.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD542J			AD542K			AD542L			AD542S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN[1]													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			250,000			250,000			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[2]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage vs. Temp.			**20**			**10**			**5**			**15**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT													
Either Input[3]			**50**			**25**			**25**			**25**	pA
Offset Current		5			2			2			2		pA
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		70			70			70			70		$nV/\sqrt{Hz}$
f = 100Hz		45			45			45			45		$nV/\sqrt{Hz}$
f = 1kHz		30			30			30			30		$nV/\sqrt{Hz}$
f = 10kHz		25			25			25			25		$nV/\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**1.5**			**1.5**			**1.5**			**1.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD542JH			AD542KH			AD542LH			AD542SH			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[3]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

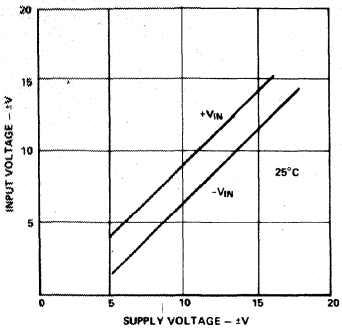


Figure 1. Input Voltage Range vs. Supply Voltage

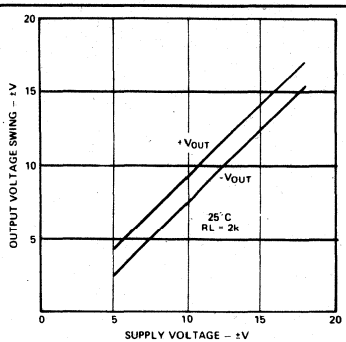


Figure 2. Output Voltage Swing vs. Supply Voltage

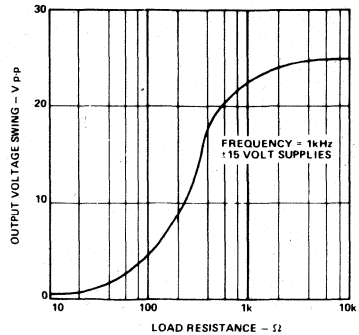


Figure 3. Output Voltage Swing vs. Resistive Load

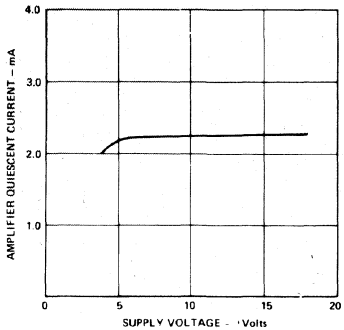


Figure 4. Quiescent Current vs. Supply Voltage

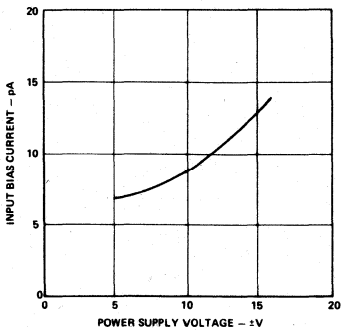


Figure 5. Input Bias Current vs. Supply Voltage

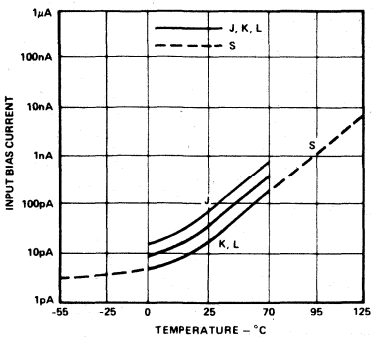


Figure 6. Input Bias Current vs. Temperature

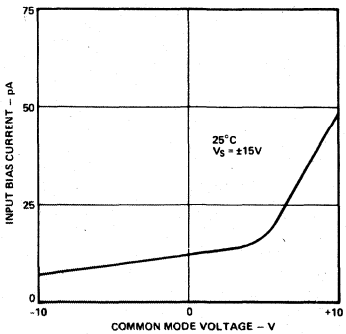


Figure 7. Input Bias Current vs. CMV

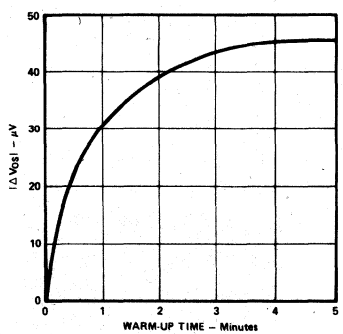


Figure 8. Input Offset Voltage Turn On Drift vs. Time

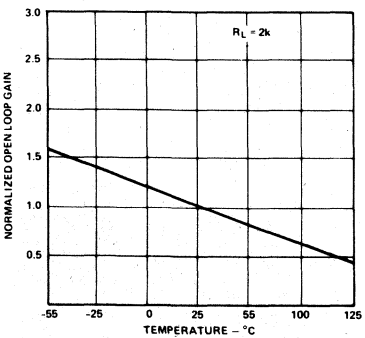


Figure 9. Open Loop Gain vs. Temperature

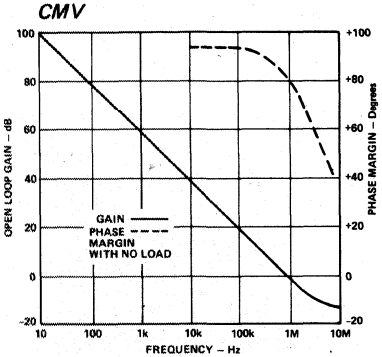


Figure 10. Open Loop Frequency Response

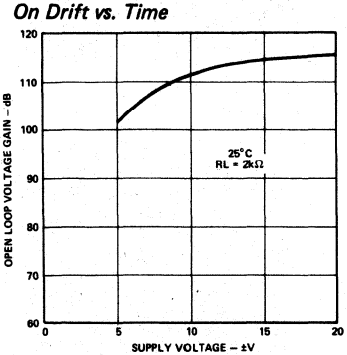


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

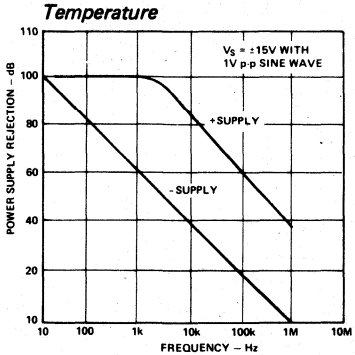


Figure 12. Power Supply Rejection vs. Frequency

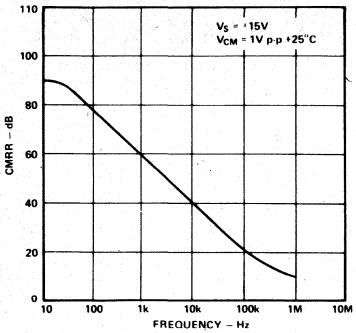


Figure 13. Common Mode Rejection vs. Frequency

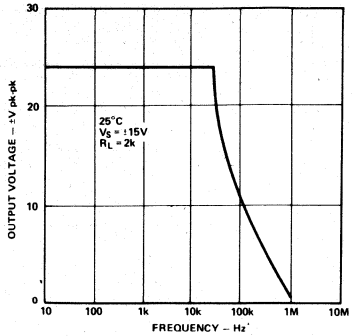


Figure 14. Large Signal Frequency Response

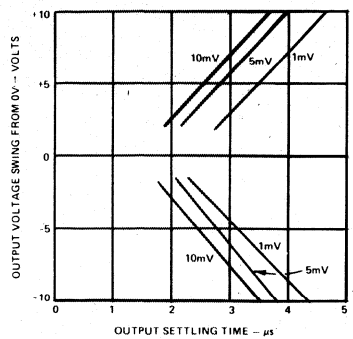


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

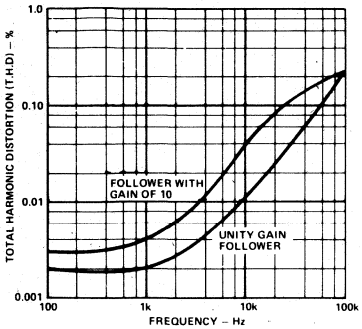


Figure 16. Total Harmonic Distortion vs. Frequency

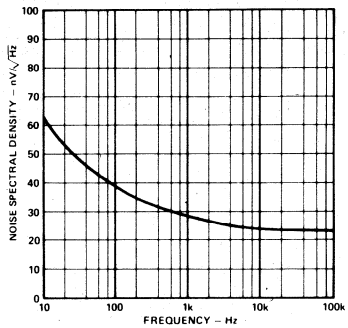


Figure 17. Input Noise Voltage Spectral Density

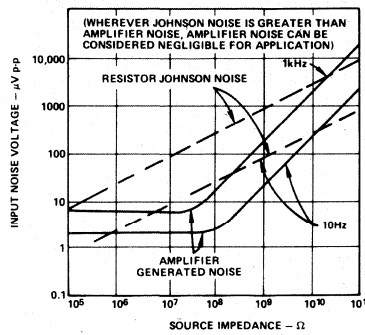
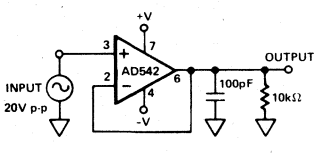
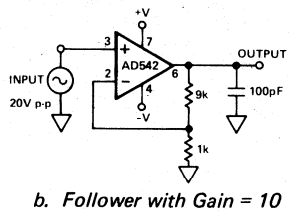


Figure 18. Total Noise vs. Source Resistance

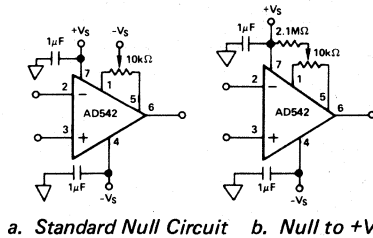


a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits



a. Standard Null Circuit b. Null to +VS

Figure 20. Offset Voltage Null Circuits

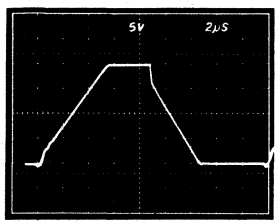


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

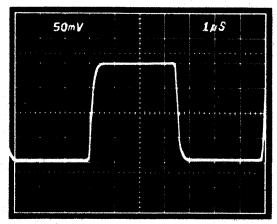


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

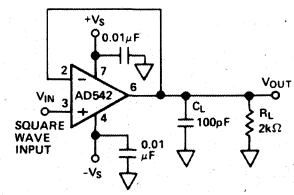


Figure 21c. Unity Gain Follower

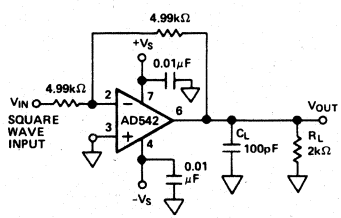


Figure 22a. Unity Gain Inverter

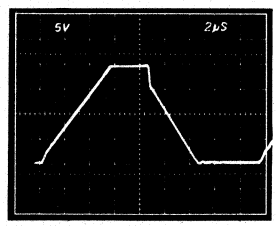


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

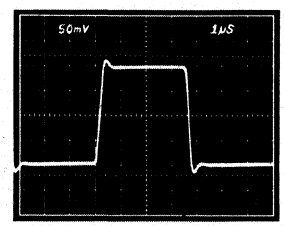


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

High Speed Implanted FET-Input Op Amp

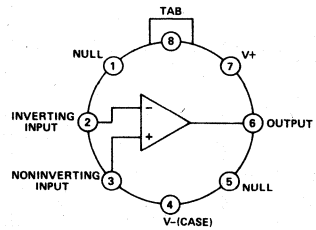
AD544

4

FEATURES

- Low Bias Current: 25pA max, warmed-up
- Low Offset Voltage: 500μV max
- Low Offset Voltage Drift: 5μV/°C max
- Low Input Voltage Noise: 2μV p-p
- Low Quiescent Current: 2.5mA max
- High Slew Rate: 13V/μs
- Fast Settling to ±0.01%: 3μs
- Low Total Harmonic Distortion: 0.0015% at 1kHz

AD544 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD544 is a high speed monolithic FET-input operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD544 offers bias currents significantly lower than currently available monolithic FET-input devices: 25pA max, warmed-up for the AD544K and L, 50pA max for the AD544J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD544L and 1.0mV on the AD544K utilizing Analog's laser-wafer-trimming (LWT) process. When combined with the AD544's low offset voltage drift (5μV/°C max for "L", 10μV/°C max for "K"), these features offer the user IC performance truly superior to existing FET-input op amps—and at low, monolithic pricing.

The key technology required for monolithic JFET-input op amps is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFET's on a monolithic bipolar chip. Analog Devices optimizes the process to produce bias currents lower than other popular FET-input op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1—10Hz), and low quiescent current.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low cost. The 2MHz bandwidth and low offset of the AD544 make it an excellent choice as an output amplifier for current output D/A Converters such as the AD7541, 12-Bit CMOS DAC. High common mode rejection (80dB, min on the "K" and "L" versions) and open-loop gain ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing on the AD544 results in the lowest bias current available in a high speed monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD544 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD544L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (In some devices, offset voltage drift can increase an additional 3μV/°C per mV of offset nulled.)
5. Low voltage noise (2μV, p-p), and low offset voltage drift (5μV/°C) enhance the AD544's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
7. Low harmonic distortion (0.0015%) makes the AD544 an ideal choice for audio applications.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD544J			AD544K			AD544L			AD544S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN[1]													
V_O = ±10V, $R_L \geq 2k\Omega$	**30,000**			**50,000**			**50,000**			**50,000**			V/V
T_{min} to T_{max}, R_L = 2kΩ	20,000			40,000			40,000			**20,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		2.0			2.0			2.0			2.0		MHz
Full Power Response		200			200			200			200		kHz
Slew Rate, Unity Gain	8.0	13.0		8.0	13.0		8.0	13.0		8.0	13.0		V/μs
Settling Time to 0.01%		3.0			3.0			3.0			3.0		μs
Total Harmonic Distortion		0.0025			0.0025			0.0025			0.0025		%
INPUT OFFSET VOLTAGE[2]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage vs. Temp. or T_{min} to T_{max}			**20**			**10**			**5**			**15**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[3]													
Either Input		10	**50**		10	25		10	25		10	25	pA
Offset Current		5			2			2			2		pA
INPUT IMPEDANCE													
Differential[4]		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**74**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		nV/√Hz
f = 100Hz		22			22			22			22		nV/√Hz
f = 1kHz		18			18			18			18		nV/√Hz
f = 10kHz		16			16			16			16		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		1.8	2.5		1.8	2.5		1.8	2.5		1.8	2.5	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD544JH			AD544KH			AD544LH			AD544SH			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

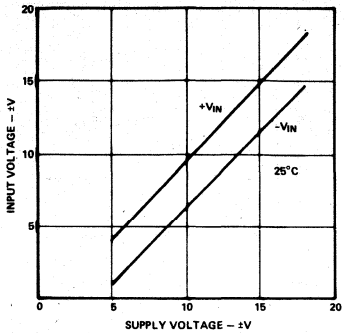


Figure 1. Input Voltage Range vs. Supply Voltage

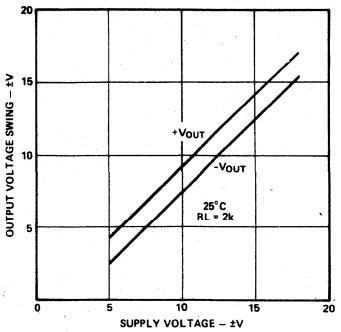


Figure 2. Output Voltage Swing vs. Supply Voltage

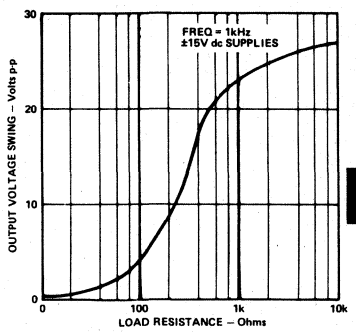


Figure 3. Output Voltage Swing vs. Resistive Load

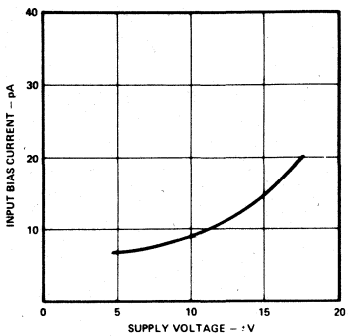


Figure 4. Input Bias Current vs. Supply Voltage

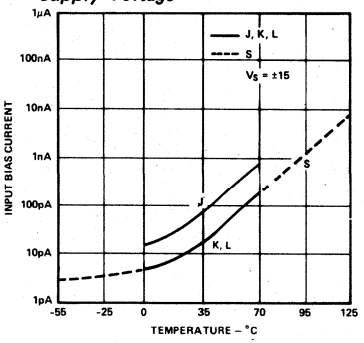


Figure 5. Input Bias Current vs. Temperature

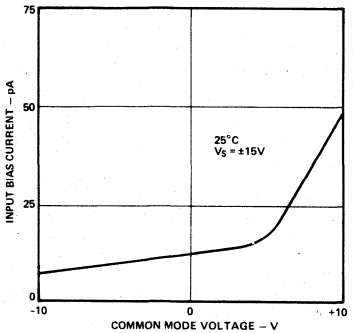


Figure 6. Input Bias Current vs. CMV

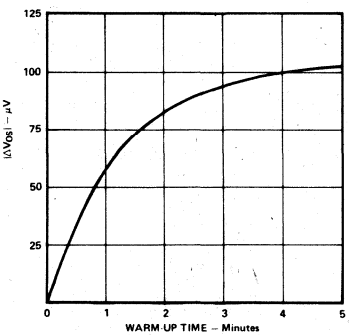


Figure 7. Change in Offset Voltage vs. Warm-Up Time

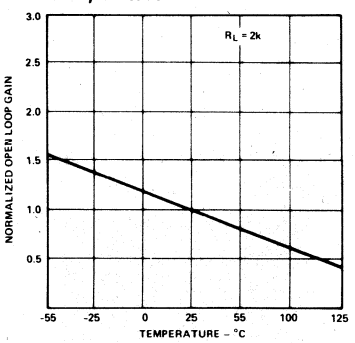


Figure 8. Open Loop Gain vs. Temperature

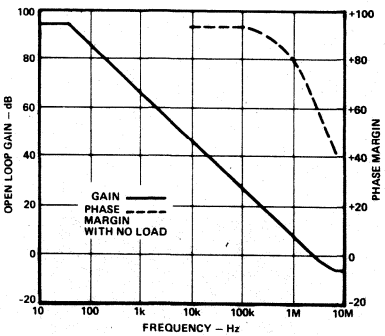


Figure 9. Open Loop Frequency Response

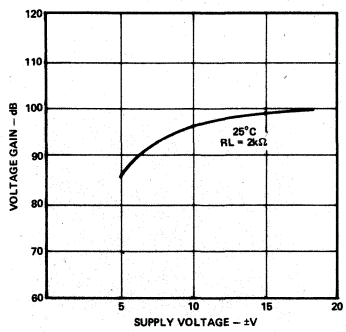


Figure 10. Open Loop vs. Voltage Gain vs. Supply Voltage

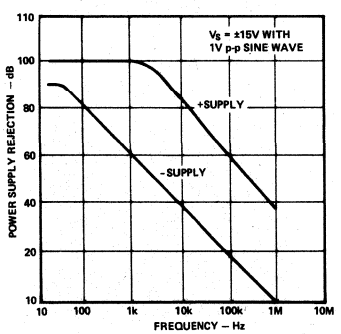


Figure 11. Power Supply Rejection vs. Frequency

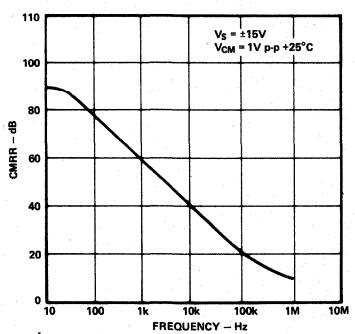


Figure 12. Common Mode Rejection Ratio vs. Frequency

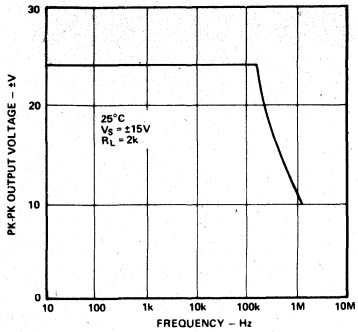


Figure 13. Large Signal Frequency Response

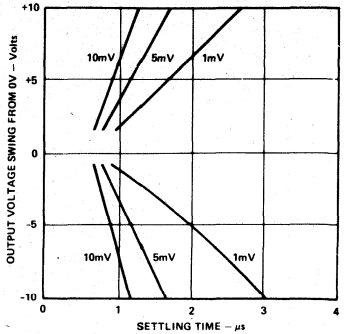


Figure 14. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

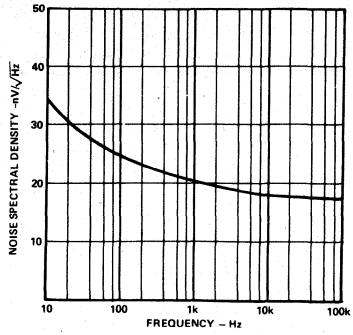


Figure 15. Noise Spectral Density

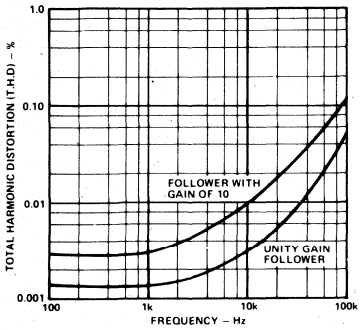


Figure 16. Total Harmonic Distortion vs. Frequency

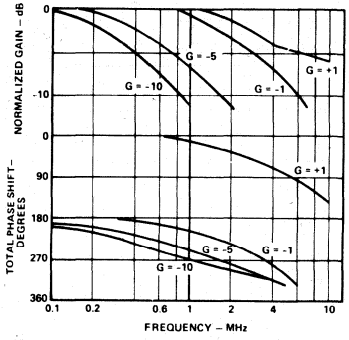


Figure 17. Closed Loop Gain & Phase vs. Frequency

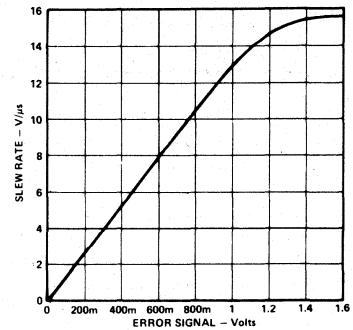
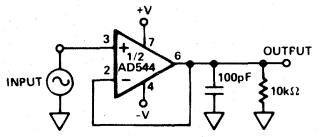
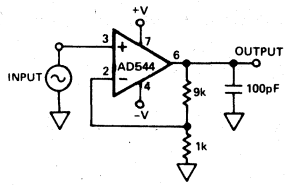


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

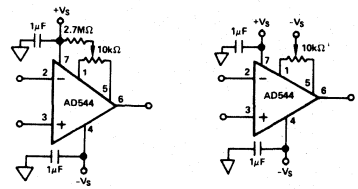


Figure 20. Offset Null Configuration

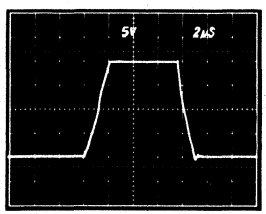


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

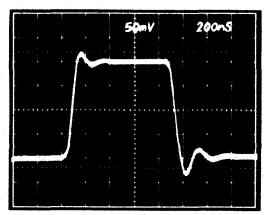


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

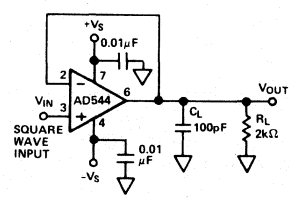


Figure 21c. Unity Gain Follower

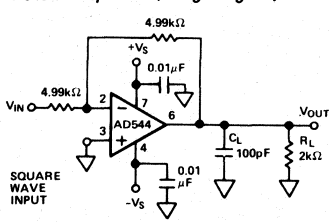


Figure 22a. Unity Gain Inverter

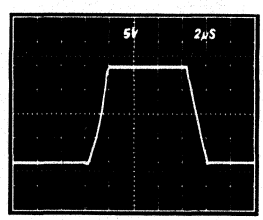


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

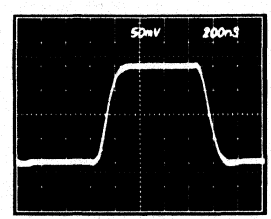


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

Precision, Low Drift FET-Input Op Amp

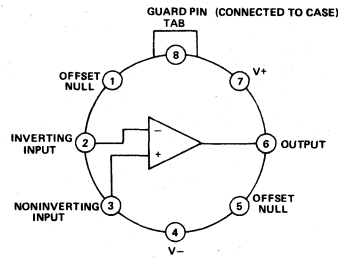
AD545

4

FEATURES

Low Offset Voltage: 0.5mV max (AD545L), 0.25mV max (AD545M)
Low Offset Voltage Drift: 5μV/°C max (AD545L), 3μV/°C max (AD545M)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545K, L, M)
Low Noise: 3μV p-p, 0.1 to 10Hz

AD545 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD545 is a precision FET-input operational amplifier with overall performance far superior to the general purpose IC FET-input op amp. The device is fabricated using a low leakage FET paired with a low power op amp. Bias current is specified as 2pA max for the AD545J and 1pA max for the AD545K, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545L, 0.25mV max for the AD545M. All devices also feature low voltage noise and power consumption. The AD545 is internally compensated, short circuit protected and free of latch-up.

The AD545 series offers a broad combination of performance features previously unavailable from a single device. For precision applications the AD545M specifies a 0.25mV max offset voltage, 3μV/°C max drift and 1pA max bias current. The AD545J, with a 1mV max offset voltage, 25μV/°C max drift and 2pA max bias current, is the best price performance choice.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/plon sensitive electrodes, photo-current detectors, biological microprobes, long term precision integrators and vacuum iongauge measurements. The versatility of the AD545 is further enhanced by its excellent low frequency noise (3μV p-p, 0.1 to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD545 is available in four versions of bias current and offset voltage, the "J", "K", "L", and "M". All are specified from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The offset voltage on the AD545 is laser trimmed to a level typically less than 250μV. Offset voltage drift is significantly lower than previously available FET-input devices (3μV/°C max for the AD545M). If additional external nulling is desired, the effect on drift is minimal (approximately 3μV/°C per millivolt, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient.
3. The low quiescent current drain of 0.8mA typical, and 1.5mA max, is among the lowest of any IC op amp and keeps self heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristics.

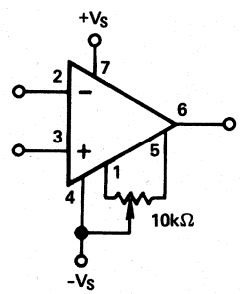
SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

MODEL	AD545J	AD545K	AD545L	AD545M
OPEN LOOP GAIN[1]				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000V/V min	40,000V/V min	40,000V/V min	40,000V/V min
$R_L \geq 10k\Omega$	40,000V/V min	50,000V/V min	50,000V/V min	50,000V/V min
T_A = min to max $R_L \geq 2k\Omega$	15,000V/V min	25,000V/V min	40,000V/V min	40,000V/V min
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*	*
Load Capacitance[2]	500pF	*	*	*
Short Circuit Current	10mA min (25mA typ)	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	700kHz	*	*	*
Full Power Response	5kHz min (16kHz typ)	*	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (1.0V/μs typ)	*	*	*
Overload Recovery Inverting Unity Gain	100μs max (16μs typ)	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	1.0mV max	0.5mV max	0.25mV max
vs. Temperature, T_A = min to max	25μV/°C max	15μV/°C max	5μV/°C max	3μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	200μV/V max	200μV/V max	200μV/V max
INPUT BIAS CURRENT				
Either Input[4]	2pA max	1pA max	1pA max	1pA max
INPUT IMPEDANCE				
Differential	$1.6pF \| 10^{13}\Omega$	*	*	*
Common Mode	$0.8pF \| 10^{15}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	3.0μV (p-p)	*	*	5μV (p-p) max
f = 10Hz	$55nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$45nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$35nV/\sqrt{Hz}$	*	*	*
Current, 0.1 to 10Hz	0.01pA (p-p)	*	*	*
10Hz to 10kHz	0.03pA rms	*	*	*
INPUT VOLTAGE RANGE				
Differential	±20V min	*	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	66dB min (80dB typ)	70dB min	76dB min	76dB min
Maximum Safe Input Voltages[5]	$\pm V_S$	*	*	*
POWER SUPPLY				
Rated Performance	±15V typ	*	*	*
Operating	*±5V min (±18V max)*	*	*	*
Quiescent Current	1.5mA max (0.8mA typ)	*	*	*
TEMPERATURE				
Operating, Rated Performance	0 to +70°C	*	*	*
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION[6]				
TO-99 Style (H08B)	AD545JH	AD545KH	AD545LH	AD545MH

*Specifications same as AD545J.

NOTES
[1] Open Loop Gain is specified with or without nulling of V_{OS}.
[2] A conservative design would not exceed 500pF of load capacitance.
[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
[5] If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage.
[6] See Section 19 for package outline information.

Specifications subject to change without notice.



Standard Offset Null Circuit

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves the additional function of reducing the effective capacitance to the input line. The case of the AD545 is brought out separately to pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or one of the amplifier's power supplies to reduce noise.
3. Printed circuit board layout and construction is critical in achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545 but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

APPLICATION NOTES

The AD545 offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545 and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated (it doubles every 10°C); we recommend restricting the load impedance to be at least 10kΩ.

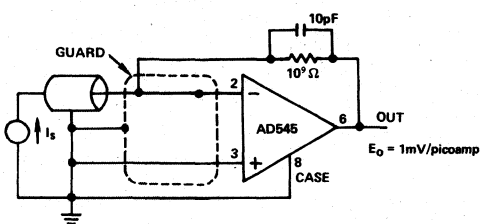


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

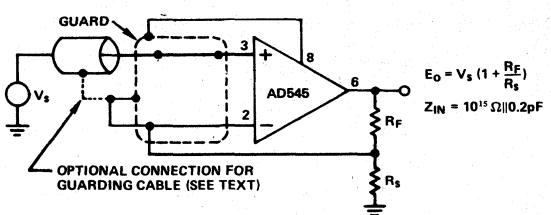


Figure 2. Very High Impedance Non-Inverting Amplifier

Typical Performance Curves

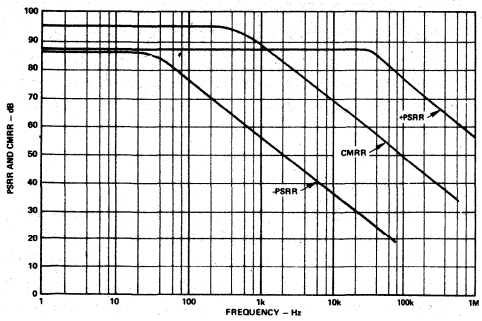


Figure 3. PSRR and CMRR Versus Frequency

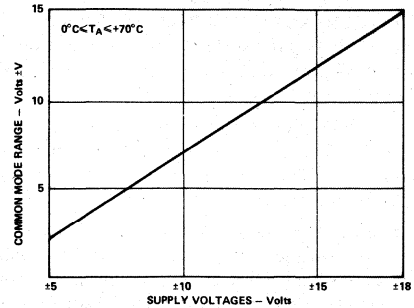


Figure 4. Input Common Mode Range Versus Supply Voltage

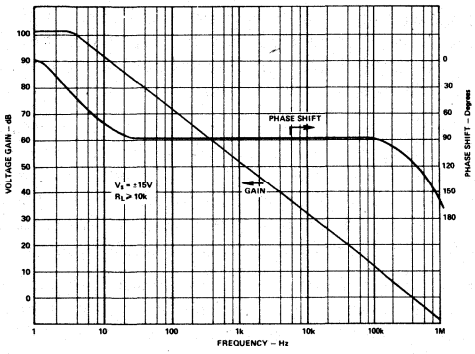


Figure 5. Open Loop Frequency Response

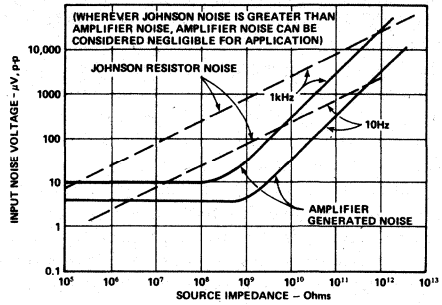


Figure 6. Total Input Noise Voltage Versus Source Impedance and Bandwidth

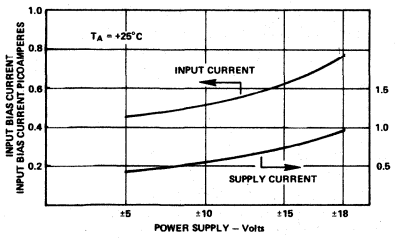


Figure 7. Input Bias Current and Supply Current Versus Supply Voltage

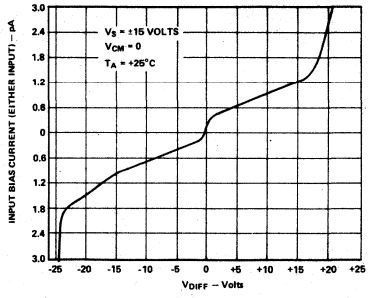


Figure 8. Input Bias Current Versus Differential Input Voltage

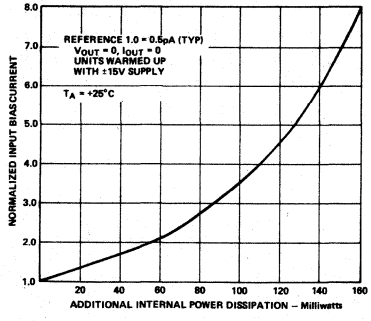


Figure 9. Input Bias Current Versus Addition Power Dissipation

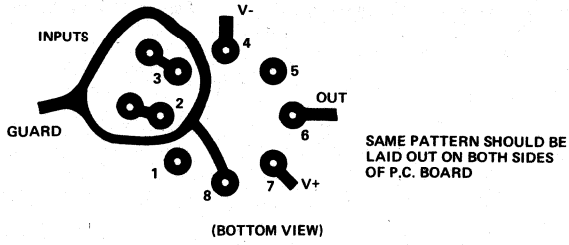


Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package

ANALOG DEVICES

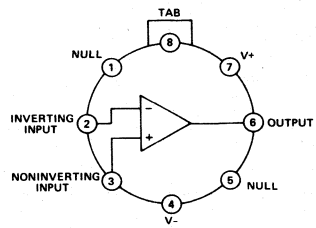
Ultra Low Drift BIFET Operational Amplifier

AD547

4

FEATURES
Ultra Low Drift (1μV/°C–AD547L)
Low Offset Voltage (0.25mV–AD547L)
Low Input Bias Currents (25pA–AD547L, K)
Low Quiescent Current (1.5mA)
Low Noise (2μV p-p)
High Open Loop Gain (110dB–AD547K, L, S)

AD547 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD547 is a monolithic, FET input operational amplifier combining the very low input bias current advantages of a BIFET op amp with offset and drift performance previously available only from high quality bipolar amplifiers.

The exclusive Analog Devices laser wafer trim process trims both the input offset voltage and offset voltage drift to levels far lower than any competing BIFET amplifier (1mV, 5μV/°C–AD547JH, 0.25mV, 1μV/°C–AD547LH).

In addition to superior low drift performance, the AD547 offers the lowest guaranteed input bias currents of any BIFET amplifier with 50pA max for the J grade and 25pA max for the L grade. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our BIFET amplifiers are specified under actual operating conditions.

The AD547 is especially designed for use in applications, such as instrumentation signal conditioning and analog computation, that require a high degree of precision at low cost.

The AD547 is offered in three commercial versions, J, K and L are specified from 0 to +70°C and the S is specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-99 cans.

PRODUCT HIGHLIGHTS

1. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and reduce offset voltage to only 0.25mV max on the AD547L.
2. Analog Devices BIFET processing provides 25pA max (10pA typical) bias currents specified after 5 minutes of warm-up.
3. Low voltage noise, high open loop gain and outstanding offset performance make the AD547 a true precision BIFET amplifier.
4. The low quiescent supply current, typically 1.1mA, enables the AD547 to bring a new level of precision to applications where low power consumption is essential.
5. A further benefit on the AD547's low power consumption and low offset voltage drift is a minimal warm-up drift after power is applied (typically 7μV shift for the AD547L).

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD547J			AD547K			AD547L			AD547S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN[1]													
V_O = ±10V, $R_L \geq 2k\Omega$	100,000			250,000			250,000			250,000			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			250,000			250,000			100,000			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	±10	±12		±10	±12		±10	±12		±10	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	±12	±13		±12	±13		±12	±13		±12	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[2]													
Initial Offset			1.0			0.5			0.25			0.5	mV
Input Offset Voltage vs. Temp.[3]			5			2			1.0			5.0	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			100			100			100	μV/V
INPUT BIAS CURRENT													
Either Input[4]		10	50		10	25		10	25		10	25	pA
Offset Current		5			2			2			2		pA
INPUT IMPEDANCE													
Differential[5]		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential		±20			±20			±20			±20		V
Common Mode	±10	±12		±10	±12		±10	±12		±10	±12		V
Common Mode Rejection	76			80			80			80			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2				4			4			4	μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		1.1	1.5		1.1	1.5		1.1	1.5		1.1	1.5	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[6]													
TO-99 Style (H08B)	AD547JH			AD547KH			AD547LH			AD547SH			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of nulled offset.

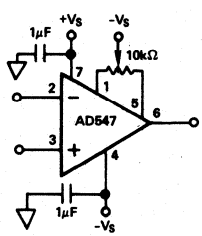
[4]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceed ±10V from ground.

[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Standard Null Circuit

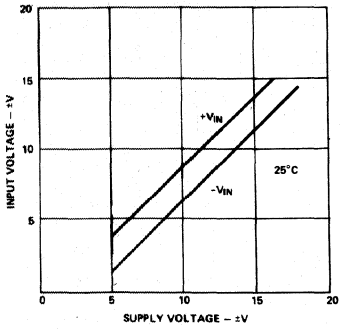


Figure 1. Input Voltage Range vs. Supply Voltage

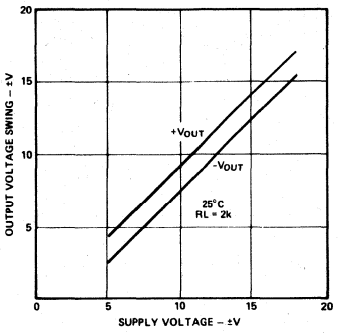


Figure 2. Output Voltage Swing vs. Supply Voltage

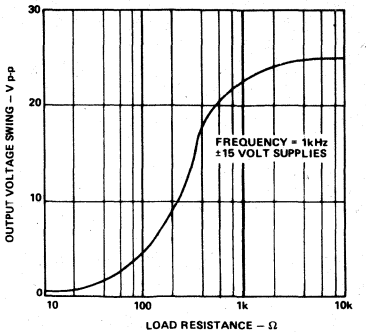


Figure 3. Output Voltage Swing vs. Resistive Load

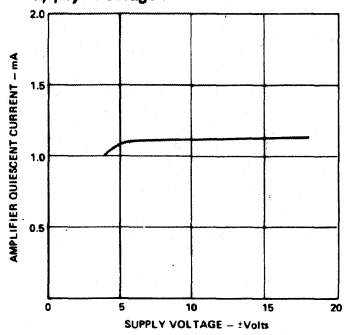


Figure 4. Quiescent Current vs. Supply Voltage

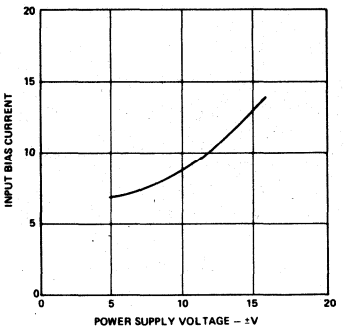


Figure 5. Input Bias Current vs. Supply Voltage

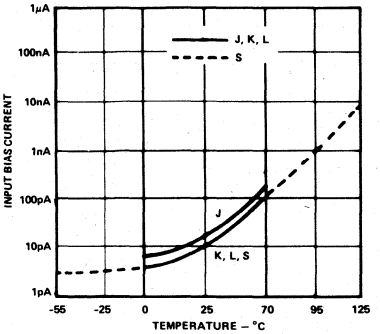


Figure 6. Input Bias Current vs. Temperature

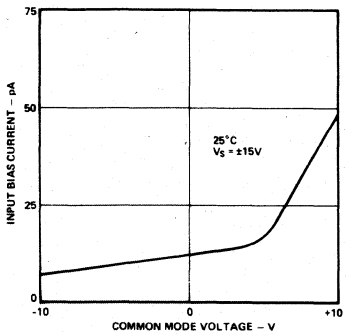


Figure 7. Input Bias Current vs. CMV

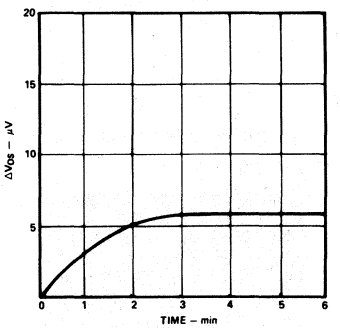


Figure 8. Input Offset Voltage Turn On Drift vs. Time

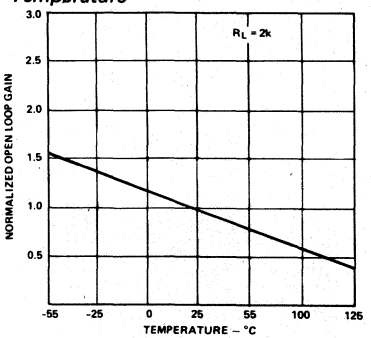


Figure 9. Open Loop Gain vs. Temperature

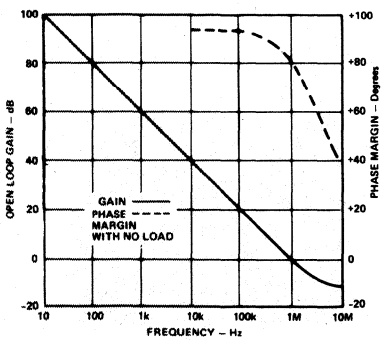


Figure. 10 Open Loop Frequency Response

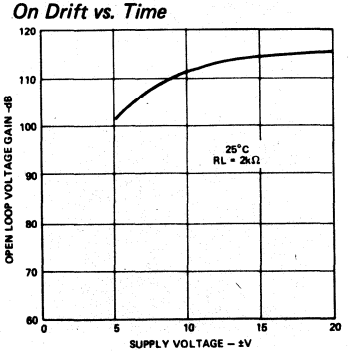


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

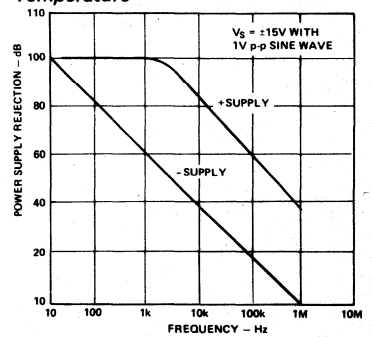


Figure 12. Power Supply Rejection vs. Frequency

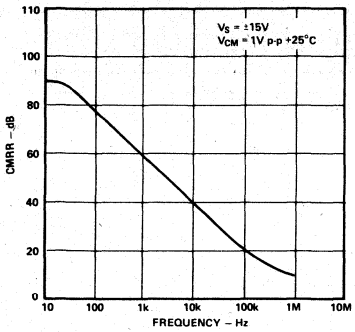


Figure 13. Common Mode Rejection vs. Frequency

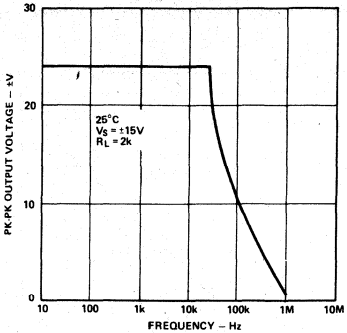


Figure 14. Large Signal Frequency Response

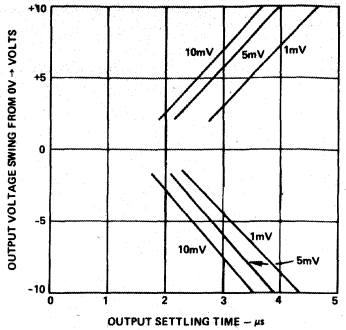


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 20)

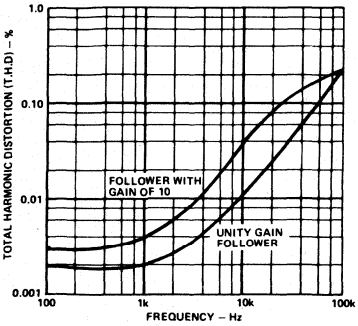


Figure 16. Total Harmonic Distortion vs. Frequency

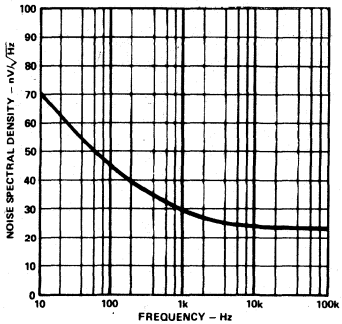


Figure 17. Input Noise Voltage Spectral Density

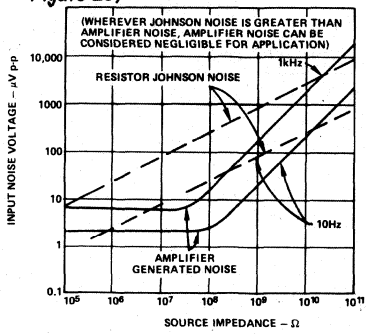
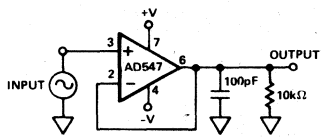
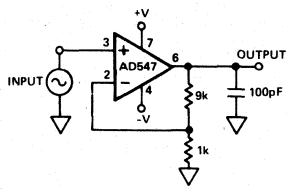


Figure 18. Total Input Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

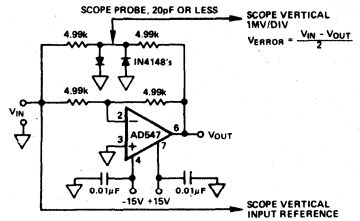


Figure 20. Settling Time Test Circuit

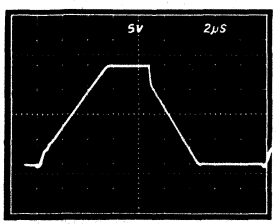


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

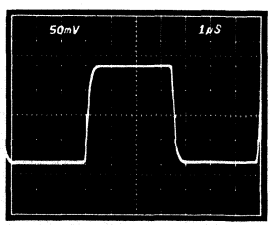


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

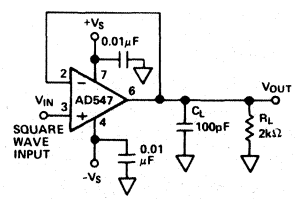


Figure 21c. Unity Gain Follower

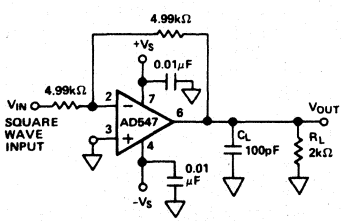


Figure 22a. Unity Gain Inverter

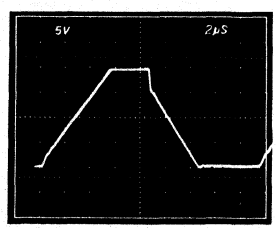


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

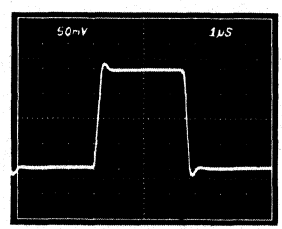


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

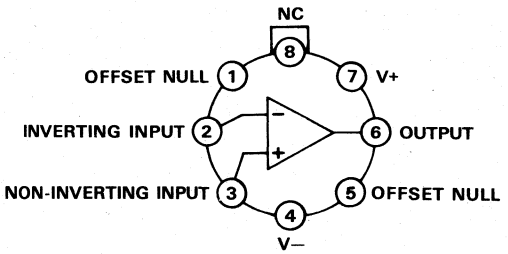
Low Cost Implanted FET-Input Op Amp

AD611

4

FEATURES
Low Offset Voltage: 0.5mV max (AD611K)
Low Offset Voltage Drift: 10μV/°C max (AD611K)
Low Bias Current: 50pA max (AD611K)
High Slew Rate: 8V/μs min
Low Supply Current: 2.5mA max
Fast Settling Time: 3μs

AD611 FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN 4 CONNECTED TO CASE

TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD611 is a precision monolithic BIFET operational amplifier designed and manufactured to offer offset voltages of 0.5mV max and offset voltage drifts of 10μV/°C max, yet is priced in the same range as lower performance devices. Analog Devices precision BIFET fabrication technology and proprietary laser wafer drift trimming process are combined with years of experience in manufacturing precision analog integrated circuits to insure consistently high performance at low cost. The offset voltage specifications mentioned above, coupled with the lowest input bias current of any general purpose BIFET amplifier, 100pA max guaranteed after five minutes of operation, make the AD611 the most precise BIFET amplifier in its price range.

In addition to the excellent dc specifications, the design of the AD611 is optimized to deliver 13V/μs slew rate, 2MHz unity gain bandwidth and a 0.01% settling time of 3μs. This combination of performance makes the AD611 ideal for any FET application where excellent performance at low cost is required. Its wide bandwidth, low offset voltage and fast settling time make this device ideal as an output amplifier for current output D/A converters of all types. 80dB of CMRR and 94dB of open loop gain ensure "12-bit" performance in high speed buffer circuits. The devices' excellent low frequency noise performance and low supply current requirements will benefit any general purpose BIFET application.

The AD611 is available in two grades rated over the 0 to +70°C temperature range; the general purpose AD611J and the high precision AD611K. Both grades are available in hermetically sealed TO-99 packages. The AD611 is pinned out in standard operational amplifier configuration to facilitate low cost upgrading of existing designs using older, less accurate amplifiers.

PRODUCT HIGHLIGHTS

1. The AD611 is laser wafer drift trimmed to offer offset voltages of 0.5mV max and offset voltage drifts of 10μV/°C.
2. Analog Devices BIFET processing results in maximum input bias currents of 50pA, guaranteed after 5 minutes of operation.
3. The high slew rate (8V/μs min.) and fast settling time (3μs to 0.01%) make the AD611 ideal for use in D/A, A/D, sample-hold circuits and precision high speed integrators.
4. Monolithic construction, along with advanced processing and manufacturing technologies result in extremely high performance at very low cost.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise noted)

Model	AD611J Min	AD611J Typ	AD611J Max	AD611K Min	AD611K Typ	AD611K Max	Units
OPEN LOOP GAIN[1]							
V_{OUT} = ±10V $R_L \geq 2k\Omega$	**30,000**	80,000		**50,000**	80,000		V/V
T_A = min to max $R_L \geq 2k\Omega$	20,000	50,000		**40,000**	50,000		V/V
FREQUENCY RESPONSE							
Unity Gain, Small Signal		2			2		MHz
Full Power Response		200			200		kHz
Slew Rate, Unity Gain	8	13		8	13		V/μs
Total Harmonic Distortion f = 1kHz		0.0025			0.0025		%
INPUT OFFSET VOLTAGE[2]		0.25	**2.0**		0.25	**0.5**	mV
vs. Temperature		5	20		5	**10**	μV/°C
vs. Supply		50	**200**		50	**100**	μV/V
T_A = min to max		70	200		70	100	μV/V
INPUT BIAS CURRENT							
Either Input[3]		25	**100**		10	**50**	pA
Input Offset Current		10	**50**		5	**25**	pA
INPUT IMPEDANCE							
Differential		$10^{12}\Omega \| 6pF$			$10^{12}\Omega \| 6pF$		
Common Mode		$10^{12}\Omega \| 3pF$			$10^{12}\Omega \| 3pF$		
INPUT VOLTAGE RANGE							
Differential[4]		±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		V
Common-Mode Rejection, V_{IN} = ±10V	**74**			**80**			dB
POWER SUPPLY							
Operating Range	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current		1.8	2.5		1.8	2.5	mA
VOLTAGE NOISE							
0.1 – 10Hz		2.0			2.0		μV p-p
10Hz		35			35		$nV/\sqrt{Hz}$
100Hz		22			22		$nV/\sqrt{Hz}$
1kHz		18			18		$nV/\sqrt{Hz}$
10kHz		16			16		$nV\sqrt{Hz}$
TEMPERATURE RANGE							
Operating, Rated Performance	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	°C
PACKAGE OPTIONS[5]		AD611JH			AD611KH		
TO-99							

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

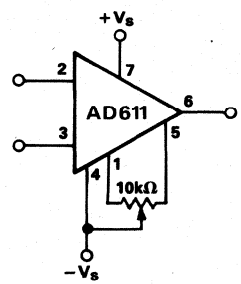
[3]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Standard Offset Null Circuit

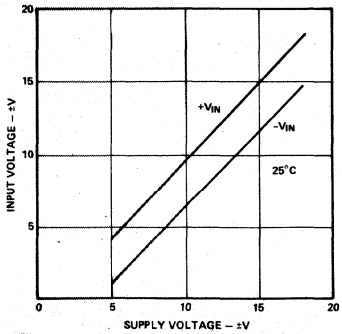


Figure 1. Input Voltage Range vs. Supply Voltage

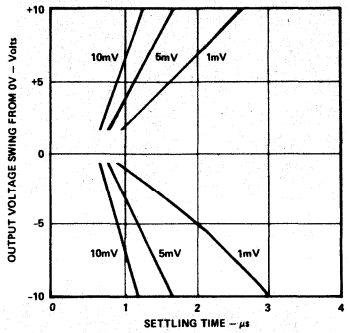


Figure 2. Output Settling Time vs. Output Swing and Error (Circuit of Figure 15a)

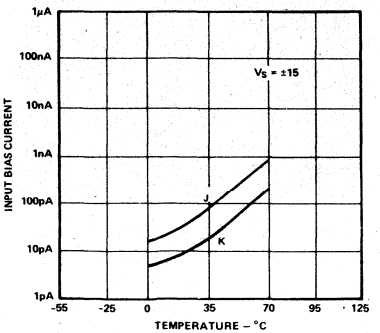


Figure 3. Input Bias Current vs. Temperature

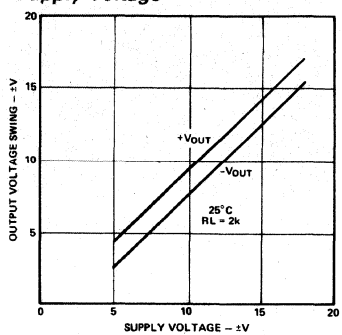


Figure 4. Output Voltage Swing vs. Supply Voltage

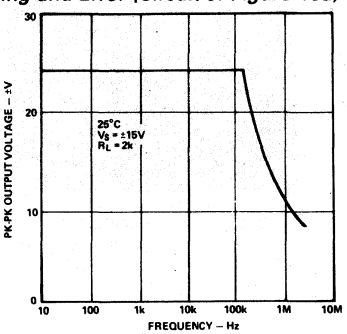


Figure 5. Large Signal Frequency Response

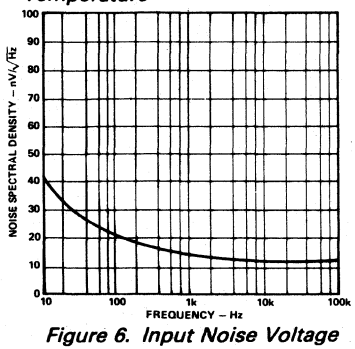


Figure 6. Input Noise Voltage Spectral Density

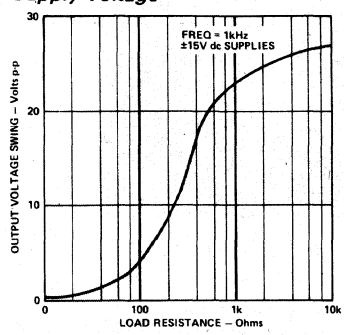


Figure 7. Output Voltage Swing vs. Resistive Load

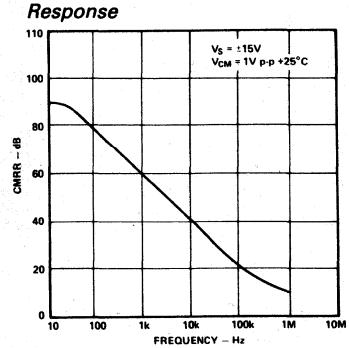


Figure 8. Common-Mode Rejection vs. Frequency

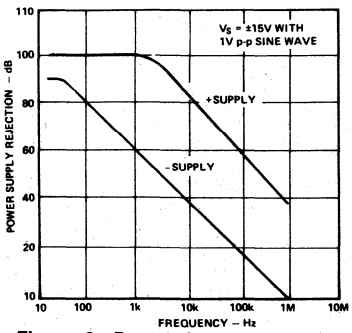


Figure 9. Power Supply Rejection vs. Frequency

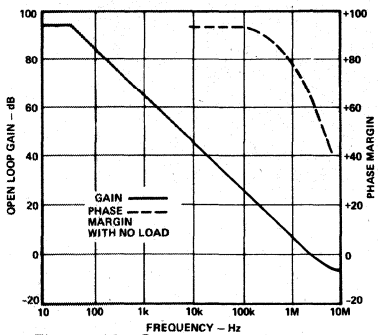


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

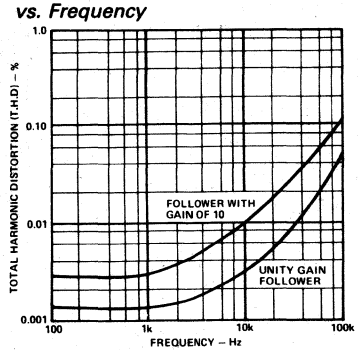


Figure 11. Total Harmonic Distortion vs. Frequency

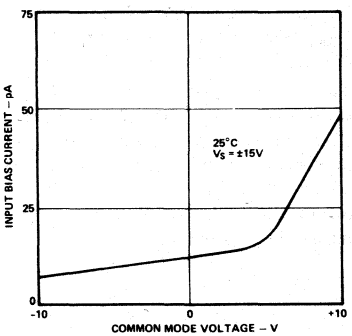


Figure 12. Input Bias Current vs. CMV

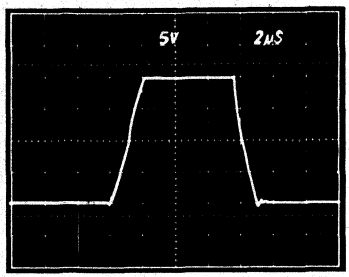


Figure 13a. Unity Gain Follower Pulse Response (Large Signal)

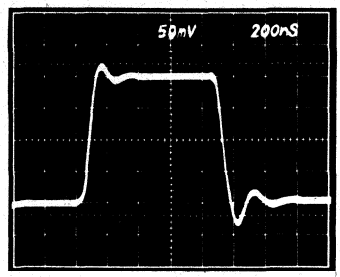


Figure 13b. Unity Gain Follower Pulse Response (Small Signal)

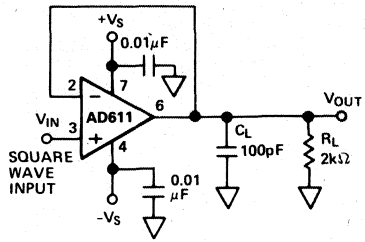


Figure 13c. Unity Gain Follower

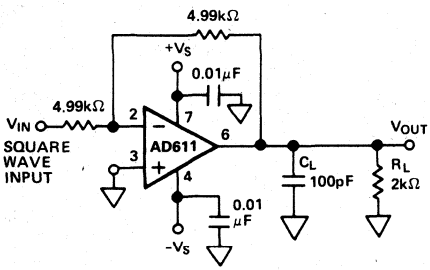


Figure 14a. Unity Gain Inverter

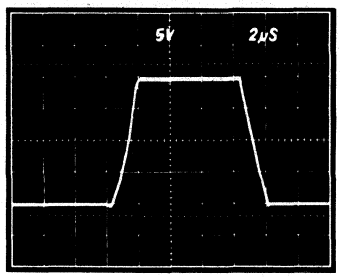


Figure 14b. Unity Gain Inverter Pulse Response (Large Signal)

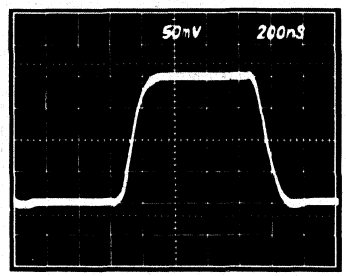


Figure 14c. Unity Gain Inverter Pulse Response (Small Signal)

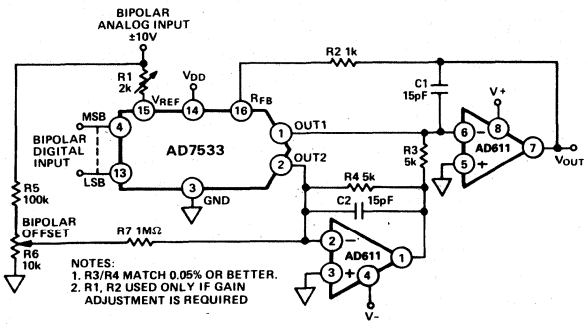


Figure 15a. AD611 Used as DAC Output Amplifiers

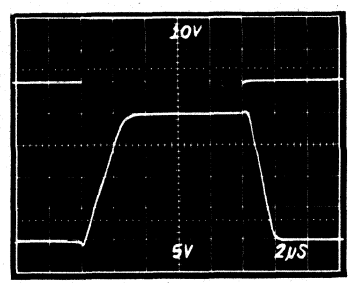


Figure 15b. Large Signal Response

Figure 15a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. The photos exhibit the response to a step input at V_{REF}. Figure 15b is the large signal response and Figure 15c is the small signal response.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The AD611 with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many CMOS DACs are not required when using the AD611.

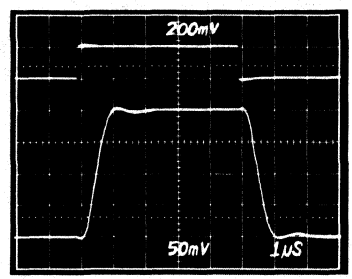


Figure 15c. Small Signal Response

ANALOG DEVICES

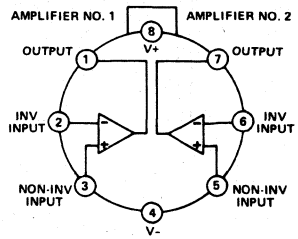
Precision Low Cost Dual BIFET Op Amp

AD642

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Current
Crosstalk-124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Open Loop Gain
Low Quiescent Current: 2.8mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pin Out

AD642 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic BI-FET operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max matched to 25pA for the AD642K and L; 75pA max, matched to 35pA for the AD642J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV and matched to 0.25mV for the AD642L, 1.0mV and matched to 0.5mV for the AD642K, utilizing Analog's laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to produce matched bias currents which have lower initial bias currents than other popular BIFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and combined with superior IC processing guarantees offset voltage tracking over the temperature range.

The AD642 is recommended for applications in which excellent ac and dc performance is required. The matched amplifiers provide a low cost solution for true instrumentation amplifiers, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters such as the AD7541.

The AD642 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C extented operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD642 has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max and matched side to side to 0.25mV (AD642L), thus eliminating the need for external nulling.
4. Low voltage noise (2μV, p-p), and high open loop gain enhance the AD642's performance as a precision op amp.
5. The standard dual amplifier pin out allows the AD642 to replace lower performance duals without redesign.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD642J			AD642K			AD642L			AD642S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	**100,000**			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			**3.5**			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	75		10	35		10	35		10	35	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**3.5**			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±15	±5		±15	±5		±15	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD642JH			AD642KH			AD642LH			AD642SH			

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

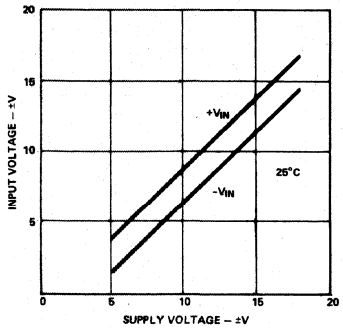


Figure 1. Input Voltage Range vs. Supply Voltage

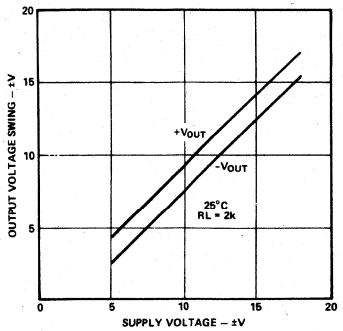


Figure 2. Output Voltage Swing vs. Supply Voltage

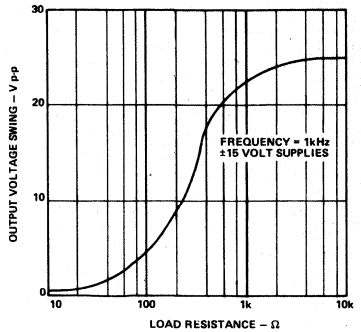


Figure 3. Output Voltage Swing vs. Resistive Load

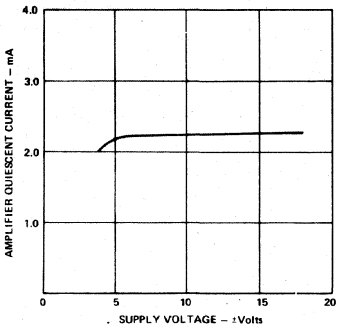


Figure 4. Quiescent Current vs. Supply Voltage

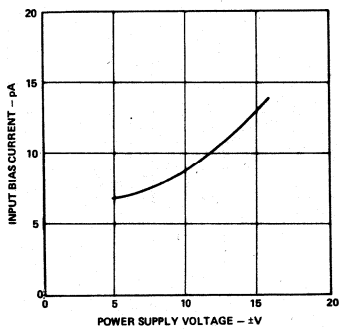


Figure 5. Input Bias Current vs. Supply Voltage

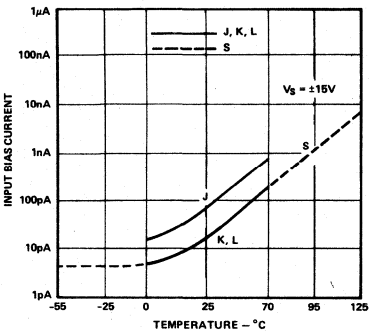


Figure 6. Input Bias Current vs. Temperature

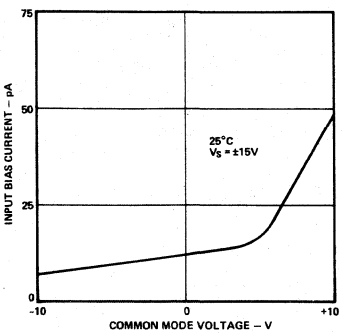


Figure 7. Input Bias Current vs. CMV

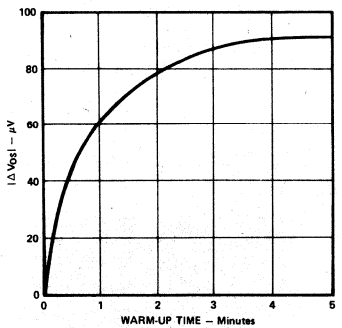


Figure 8. Input Offset Voltage Turn On Drift vs. Time

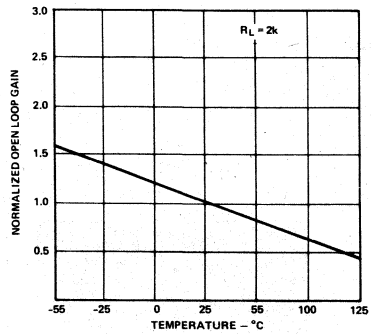


Figure 9. Open Loop Gain vs. Temperature

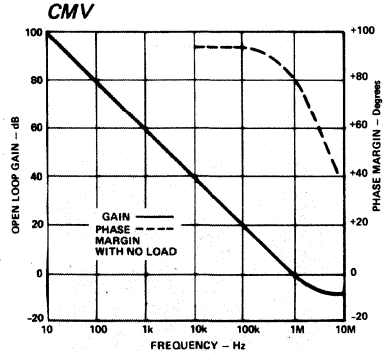


Figure 10. Open Loop Frequency Response

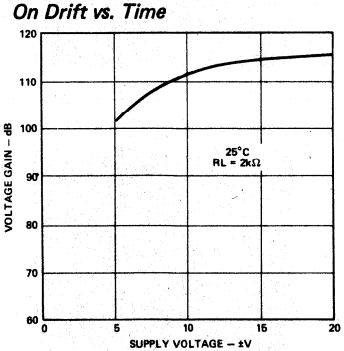


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

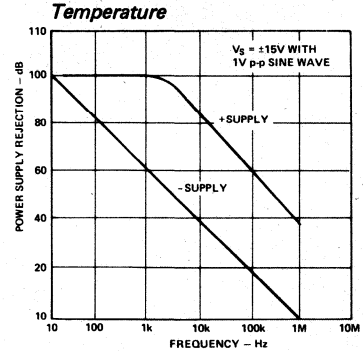


Figure 12. Power Supply Rejection vs. Frequency

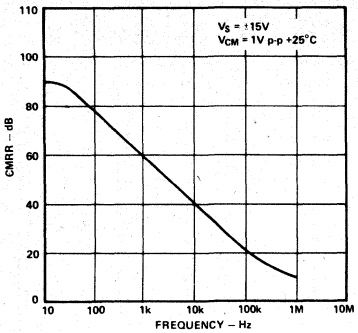


Figure 13. Common Mode Rejection vs. Frequency

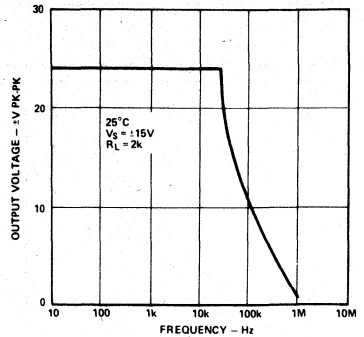


Figure 14. Large Signal Frequency Response

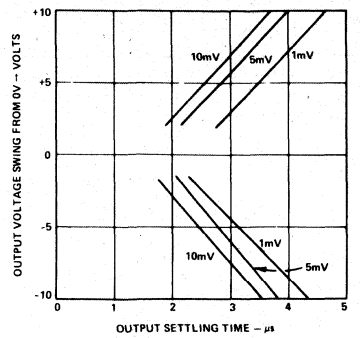


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

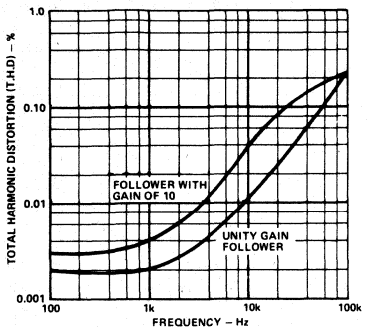


Figure 16. Total Harmonic Distortion vs. Frequency

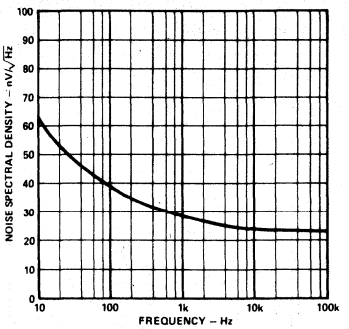


Figure 17. Input Noise Voltage Spectral Density

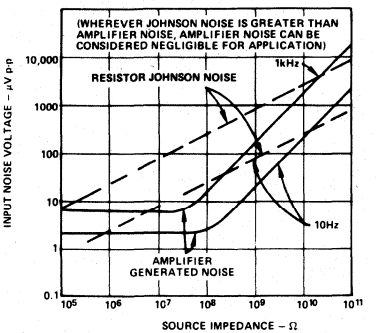
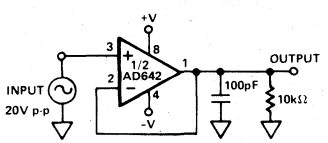
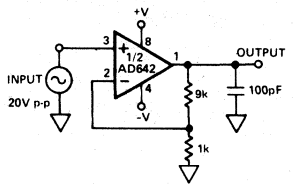


Figure 18. Total Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

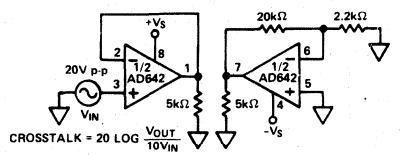


Figure 20. Crosstalk Test Circuit

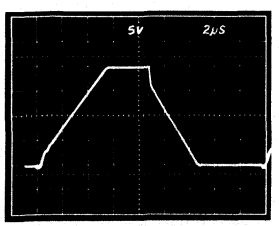


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

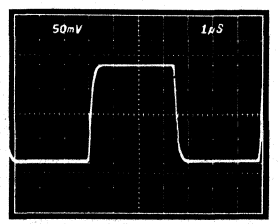


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

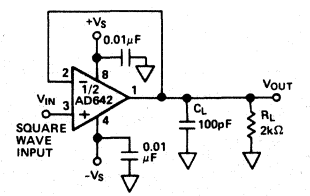


Figure 21c. Unity Gain Follower

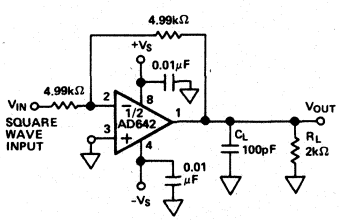


Figure 22a. Unity Gain Inverter

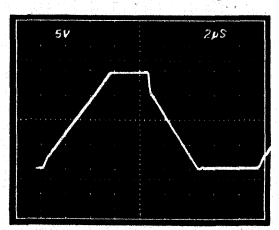


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

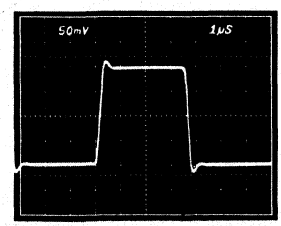


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

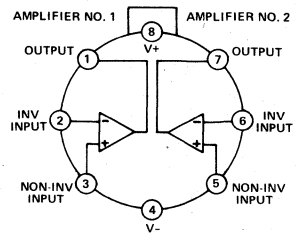
Dual High Speed Implanted BIFET Op Amp

AD644

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Currents
Crosstalk -124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Slew Rate: 13V/μs
Low Quiescent Current: 4.5mA max
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0015% at 1kHz
Standard Dual Amplifier Pin Out

AD644 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD644 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD644 offers matched bias currents that are significantly lower than currently available monolithic dual BIFET operational amplifiers: 35pA max, matched to 25pA for the AD644K and L, 75pA max matched to 35pA for the AD644J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV, and matched to 0.25mV for the AD644L, 1.0mV and matched to 0.5mV for the AD644K, utilizing Analog Devices' laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This process optimizes the ability to produce matched amplifiers which have lower initial bias currents than other popular BIFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and superior IC processing guarantees offset voltage tracking over the temperature range.

The AD644 is recommended for applications in which both excellent ac and dc performance is required. The matched amplifiers provide a low cost solution to true wideband instrumentation amplifiers, low dc drift active filters and output amplifiers for four quadrant multiplying D/A converters such as the AD7541, 12-bit CMOS DAC.

The AD644 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD644 has tight side to side matching specifications to ensure high performance without matching individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD644 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max matched side to side to 0.25mV (AD644L), thus eliminating the need for external nulling.
4. Improved bipolar and JFET processing on the AD644 result in the lowest matched bias current available in a high speed monolithic FET op amp.
5. Low voltage noise (2μV p-p) and high open loop gain enhance the AD644's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and dual high speed integrators.
7. Low harmonic distortion (0.0015%) and low crosstalk (-124dB) make the AD644 an ideal choice for stereo audio applications.
8. The standard dual amplifier pin out allows the AD644 to replace lower performance duals without redesign.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD644J			AD644K			AD644L			AD644S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	30,000			50,000			50,000			50,000			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	20,000			40,000			40,000			20,000			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	±10	±12		±10	±12		±10	±12		±10	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	±12	±13		±12	±13		±12	±13		±12	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		2.0			2.0			2.0			2.0		MHz
Full Power Response		200			200			200			200		kHz
Slew Rate, Unity Gain	8.0	13.0		8.0	13.0		8.0	13.0		8.0	13.0		V/μs
Total Harmonic Distortion		0.0015			0.0015			0.0015			0.0015		%
INPUT OFFSET VOLTAGE[1]													
Initial Offset			2.0			1.0			0.5			1.0	mV
Input Offset Voltage T_{min} to T_{max}			3.5			2.0			1.0			3.5	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			100			100			100	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	75		10	35		10	35		10	35	pA
Offset Current		10			5			5			5		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			1.0			0.5			0.25			0.5	mV
Input Offset Voltage T_{min} to T_{max}			3.5			2.0			1.0			3.5	mV
Input Bias Current			35			25			25			35	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	±10	±12		±10	±12		±10	±12		±10	±12		V
Common Mode Rejection	76			80			80			80			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		$nV/\sqrt{Hz}$
f = 100Hz		22			22			22			22		$nV/\sqrt{Hz}$
f = 1kHz		18			18			18			18		$nV/\sqrt{Hz}$
f = 10kHz		16			16			16			16		$nV/\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		3.5	4.5		3.5	4.5		3.5	4.5		3.5	4.5	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD644JH			AD644KH			AD644LH			AD644SH			

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

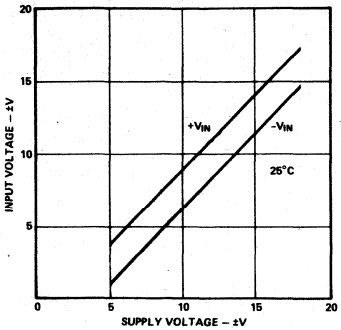


Figure 1. Input Voltage Range vs. Supply Voltage

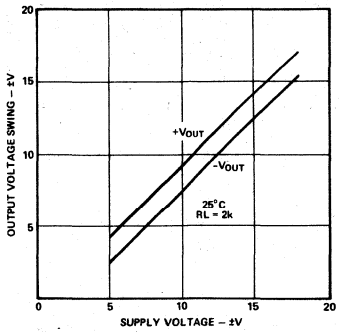


Figure 2. Output Voltage Swing vs. Supply Voltage

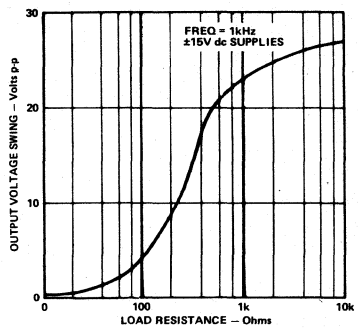


Figure 3. Output Voltage Swing vs. Resistive Load

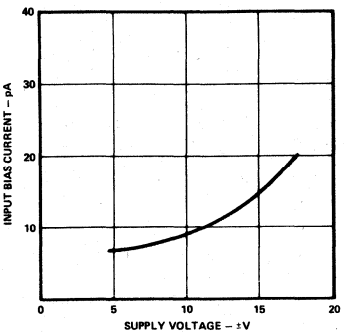


Figure 4. Input Bias Current vs. Supply Voltage

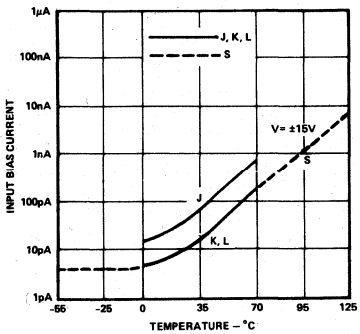


Figure 5. Input Bias Current vs. Temperature

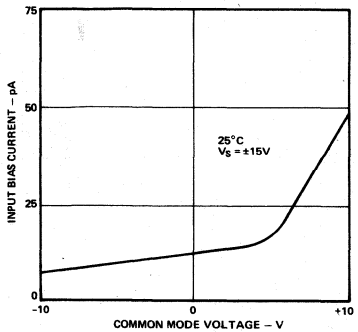


Figure 6. Input Bias Current vs. CMV

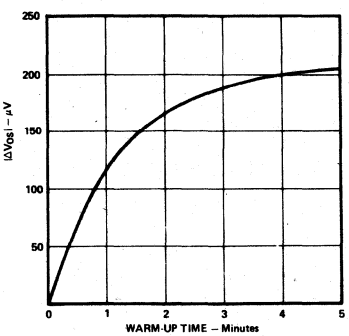


Figure 7. Change in Offset Voltage vs. Warm-Up Time

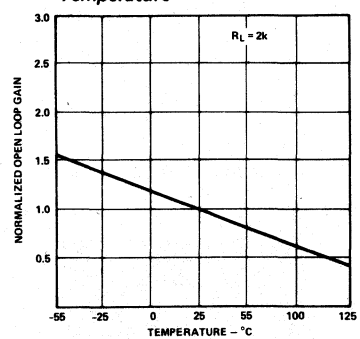


Figure 8. Open Loop Gain vs. Temperature

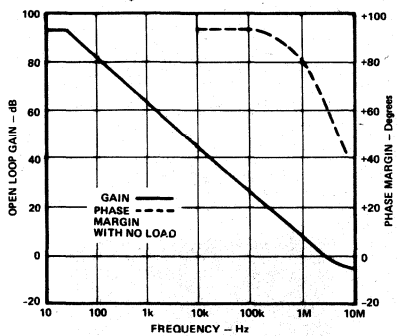


Figure 9. Open Loop Frequency Response

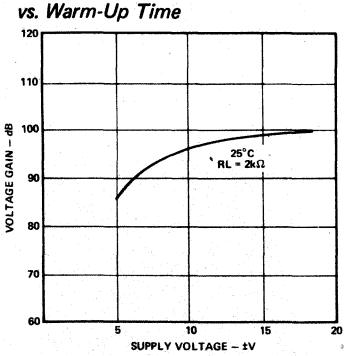


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

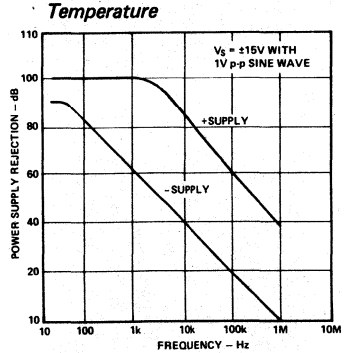


Figure 11. Power Supply Rejection vs. Frequency

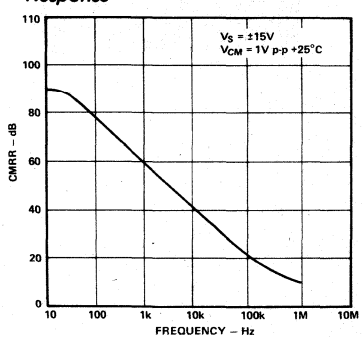


Figure 12. Common Mode Rejection Ratio vs. Frequency

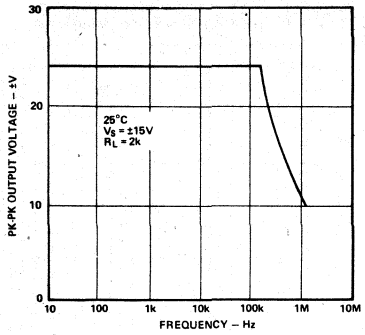


Figure 13. Large Signal Frequency Response

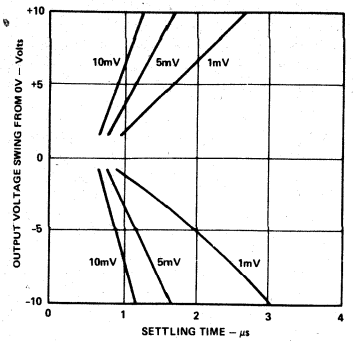


Figure 14. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

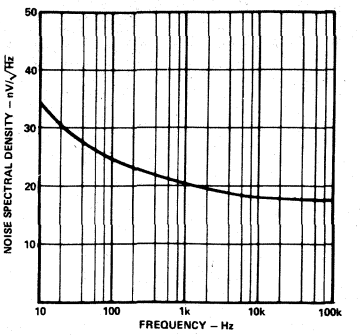


Figure 15. Noise Spectral Density

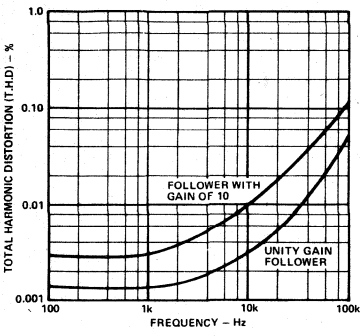


Figure 16. Total Harmonic Distortion vs. Frequency

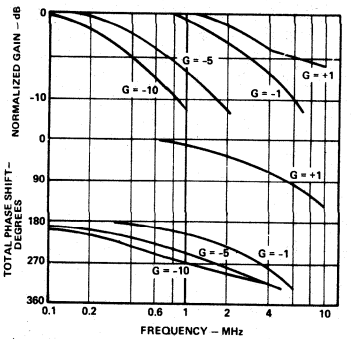


Figure 17. Closed Loop Gain & Phase vs. Frequency

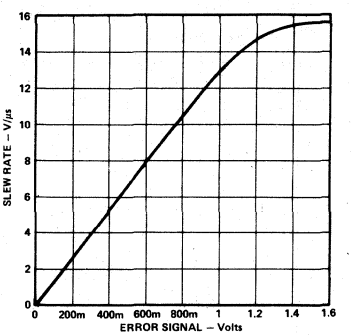
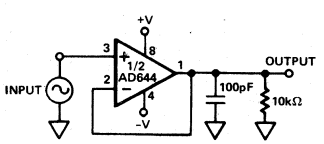
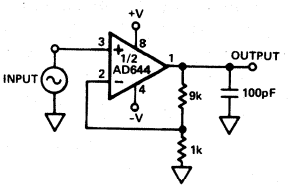


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

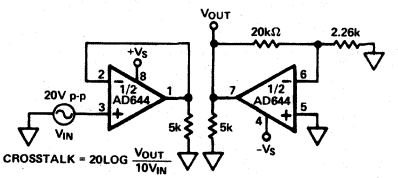


Figure 20. Crosstalk Test Circuit

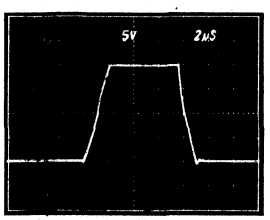


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

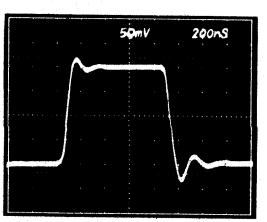


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

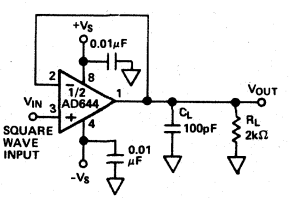


Figure 21c. Unity Gain Follower

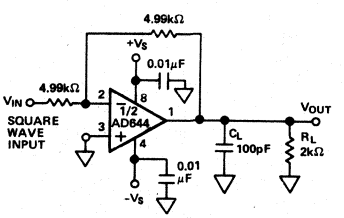


Figure 22a. Unity Gain Inverter

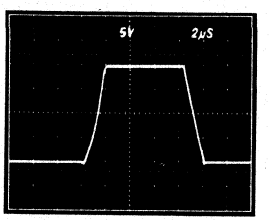


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

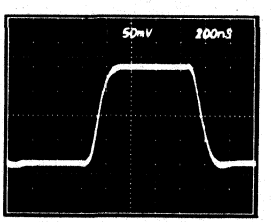


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

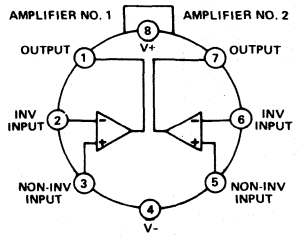
Ultra-Low Drift Dual BIFET Op Amp

AD647

FEATURES

- Low Offset Voltage Drift
- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Current
- Crosstalk -124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 250μV max
- Low Input Voltage Noise: 2μV p-p
- High Open Loop Gain: 108dB
- Low Quiescent Current: 2.8mA max
- Low Total Harmonic Distortion
- Standard Dual Amplifier Pin Out

AD647 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD647 is an ultra low drift dual JFET amplifier that combines high performance and convenience in a single package.

The AD647 uses the most advanced ion-implantation and laser wafer drift trimming technologies to achieve the highest performance currently available in a dual JFET. Ion-implantation permits the fabrication of matched JFETs on a monolithic bipolar chip. Laser wafer drift trimming trims both the initial offset voltage and its drift with temperature to provide offsets as low as 100μV (250μV max) and drifts of 2.5μV/°C max.

In addition to outstanding individual amplifier performance, the AD647 offers guaranteed and tested matching performance on critical parameters such as offset voltage, offset voltage drift and bias currents.

This high level of performance makes the AD647 especially well suited for high precision instrumentation amplifier applications that previously would have required the costly selection and matching of space wasting single amplifiers.

The AD647 also offers high levels of performance for Digital to Analog Converter output amplifiers, and filtering applications.

The AD647 is offered in four performance grades, three commercial (the J, K, and L) and one extended (the S). All are supplied in hermetically sealed 8-pin TO-99 packages.

PRODUCT HIGHLIGHTS

1. The AD647 is guaranteed and tested to tight matching specifications to ensure high performance and to eliminate the selection and matching of single devices.
2. Laser wafer drift trimming reduces offset voltage and offset voltage drifts to 250μV and 2.5μV/°C max.
3. Voltage noise is guaranteed at 4μV p-p max (0.1 to 10Hz) on K, L and S grades.
4. Bias current (35pA K, L, S; 75pA J) is specified after five minutes of operation.
5. Total supply current is a low 2.8mA max.
6. High open loop gain ensures high linearity in precision instrumentation amplifier applications.
7. The standard dual amplifier pin out permits the direct substitution of the AD647 for lower performance devices.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD647J			AD647K			AD647L			AD647S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			250,000			250,000			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage vs. Temp.			**10**			**5**			**2.5**			**5.0**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	75		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**10**			**5**			**2.5**			**10.0**	μV/°C
Input Bias Current			**35**			**25**			**25**			**25**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2				**4**			**4**			**4**	μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD647JH			AD647KH			AD647LH			AD647SH			

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

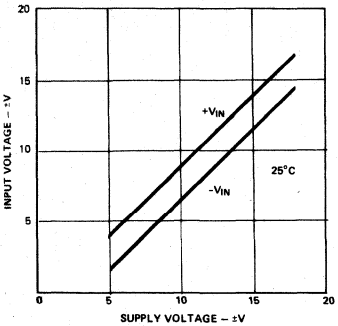


Figure 1. Input Voltage Range vs. Supply Voltage

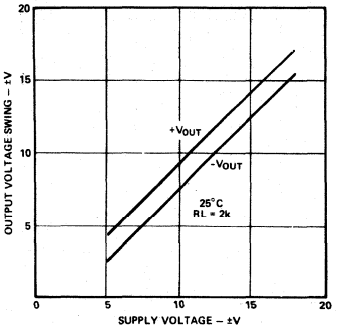


Figure 2. Output Voltage Swing vs. Supply Voltage

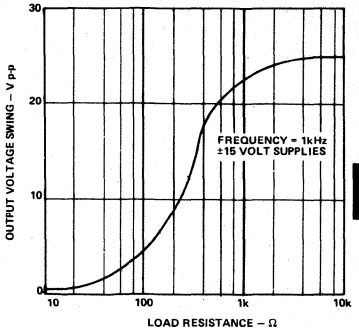


Figure 3. Output Voltage Swing vs. Resistive Load

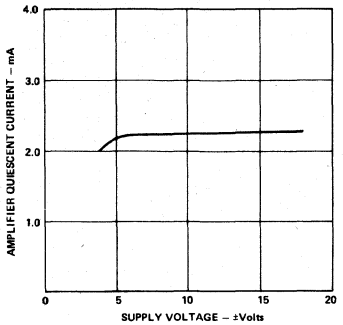


Figure 4. Quiescent Current vs. Supply Voltage

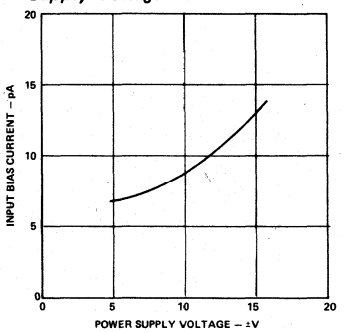


Figure 5. Input Bias Current vs. Supply Voltage

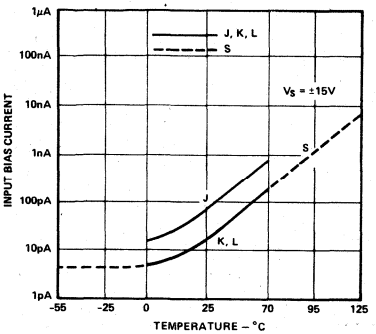


Figure 6. Input Bias Current vs. Temperature

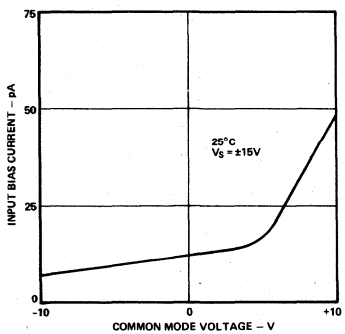


Figure 7. Input Bias Current vs. CMV

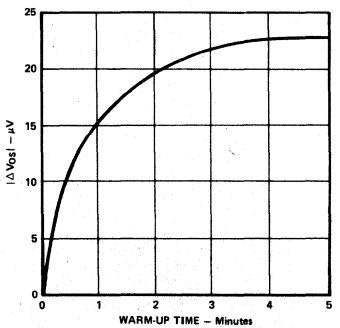


Figure 8. Input Offset Voltage Turn On Drift vs. Time

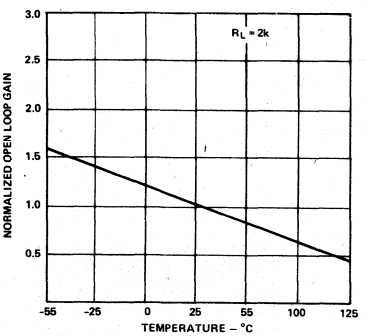


Figure 9. Open Loop Gain vs. Temperature

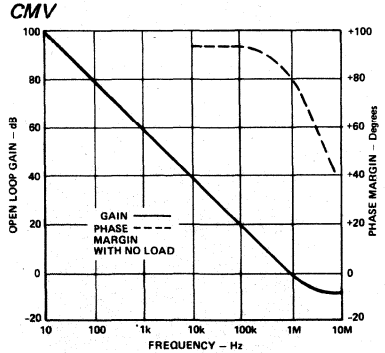


Figure 10. Open Loop Frequency Response

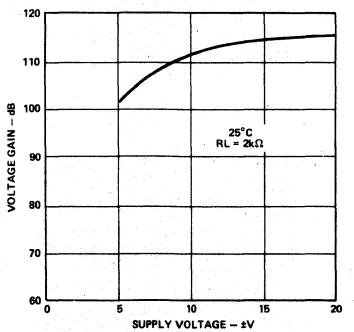


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

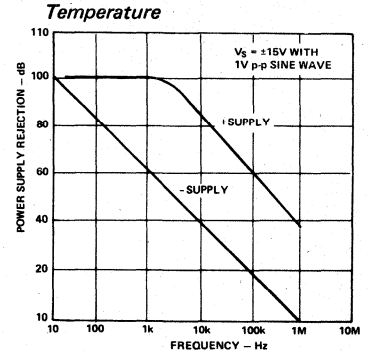


Figure 12. Power Supply Rejection vs. Frequency

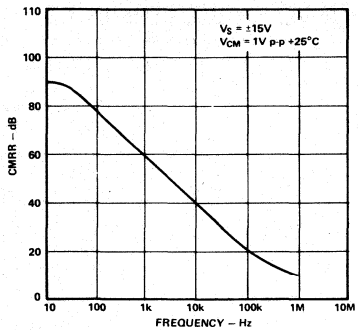


Figure 13. Common Mode Rejection vs. Frequency

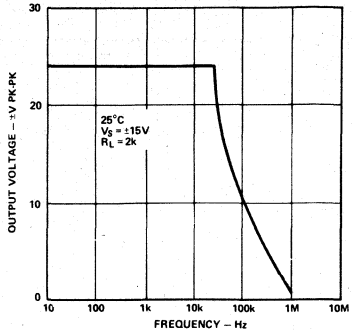


Figure 14. Large Signal Frequency Response

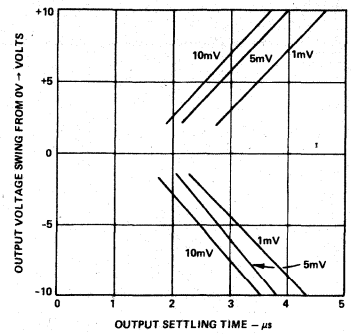


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

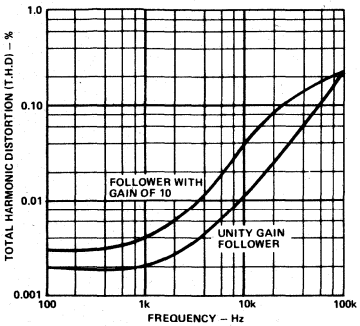


Figure 16. Total Harmonic Distortion vs. Frequency

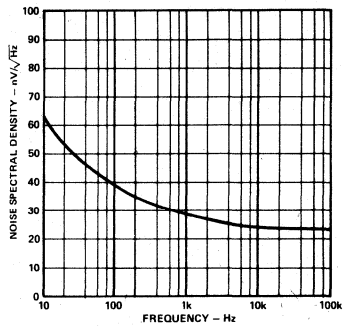


Figure 17. Input Noise Voltage Spectral Density

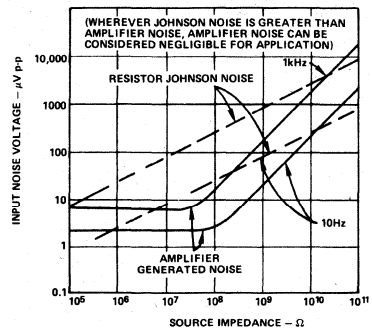
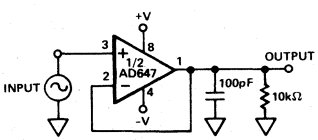
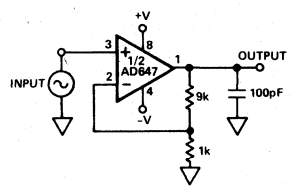


Figure 18. Total rms Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

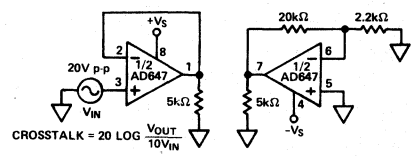


Figure 20. Crosstalk Test Circuit

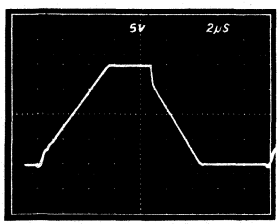


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

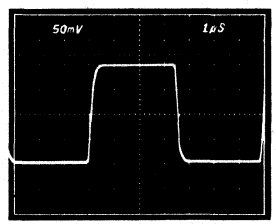


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

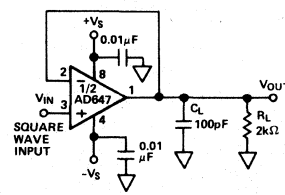


Figure 21c. Unity Gain Follower

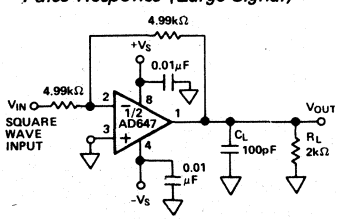


Figure 22a. Unity Gain Inverter

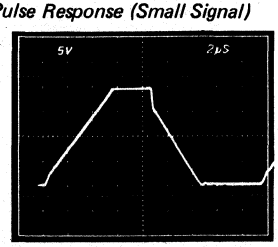


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

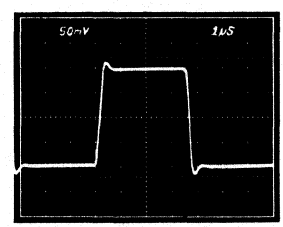


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

Low Cost High Accuracy IC Op Amps

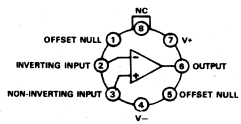
AD741 SERIES

FEATURES

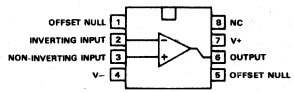
Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1kΩ load (J, S)
  T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

AD741 SERIES FUNCTIONAL DIAGRAMS



TO-99
TOP VIEW



8-PIN MINI DIP
TOP VIEW

GENERAL DESCRIPTION

The Analog Devices AD741 series are high performance monolithic operational amplifiers. All the devices feature full short circuit protection and internal compensation.

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the standard AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection. For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

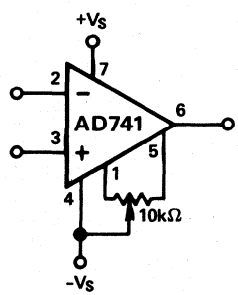
SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

Model	AD741C Min	AD741C Typ	AD741C Max	AD741 Min	AD741 Typ	AD741 Max	AD741J Min	AD741J Typ	AD741J Max	Units
OPEN LOOP GAIN										
R_L = 1kΩ, V_O = ±10V							50,000	200,000		V/V
R_L = 2kΩ, V_O = ±10V	20,000	200,000		50,000	200,000					V/V
T_A = min to max R_L = 2kΩ	15,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1kΩ, T_A = min to max							±10	±13		V
Voltage @ R_L = 2kΩ, T_A = min to max	±10	±13		±10	±13					V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time $C_L \leq$ 10V p-p		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq$ 10kΩ, Adj. to Zero		1.0	6.0		1.0	5.0		1.0	3.0	mV
T_A = min to max		1.0	7.5		1.0	6.0			4.0	mV
Average vs. Temperature (Untrimmed)									20	μV/°C
vs. Supply, T_A = min to max								30	100	μV/V
INPUT OFFSET CURRENT										
Initial		20	200		20	200		5	50	nA
T_A = min to max		40	300		85	500			100	nA
Average vs. Temperature								0.1		nA/°C
INPUT BIAS CURRENT										
Initial		80	500		80	500		40	200	nA
T_A = min to max		120	800		300	1,500			400	nA
Average vs. Temperature								0.6		nA/°C
INPUT IMPEDANCE DIFFERENTIAL	0.3	2.0		0.3	2.0			1.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe									±30	V
Common Mode, max Safe	±12	±13		±12	±13			±15		V
Common Mode Rejection,										
$R_S \leq$ 10kΩ, T_A = min to max, V_{IN} = ±12V	70	90		70	90		80	90		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating							±5		±18	V
Power Supply Rejection Ratio		30	150		30	150				μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.2	3.3	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min					60	100				mW
T_A = max					45	75				mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	−55		+125	0		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C

NOTES

[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.



Standard Nulling Offset Circuit

Model	AD741K Min	AD741K Typ	AD741K Max	AD741L Min	AD741L Typ	AD741L Max	AD741S Min	AD741S Typ	AD741S Max	Units
OPEN LOOP GAIN										
R_L = 1kΩ, V_O = ±10V							50,000	200,000		V/V
R_L = 2kΩ, V_O = ±10V	50,000	200,000		50,000	200,000					V/V
T_A = min to max R_L = 2kΩ	25,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1kΩ, T_A = min to max										V
Voltage @ R_L = 2kΩ, T_A = min to max	±10	±13		±10	±13		±10	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Respone (Unity Gain)										
Rise Time		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq$ 10kΩ, Adj. to Zero		0.5	2.0		0.2	0.5		1.0	2	mV
T_A = min to max			3.0			1.0			4	mV
Average vs. Temperature (Untrimmed)		6.0	15.0		2.0	5.0		6.0	15.0	μV/°C
vs. Supply, T_A = min to max		5	15.0		5	15.0		30	100	μV/V
INPUT OFFSET CURRENT										
Initial		2	10		2	5		2	10	nA
T_A = min to max			15			10			25	nA
Average vs. Temperature		0.02	0.2		0.02	0.1		0.1	0.25	nA/°C
INPUT BIAS CURRENT										
Initial		30	75		30	50		30	75	nA
T_A = min to max			120			100			250	nA
Average vs. Temperature		0.6	1.5		0.6	1.0		0.6	2.0	nA/°C
INPUT IMPEDANCE DIFFERENTIAL		2			2			2		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe		±30			±30			±30		V
Common Mode max Safe		±15			±15			±15		V
Common Mode Rejection,										
$R_S \leq$ 10kΩ, T_A = min to max										
V_{IN} = ±12V	90	100		90	100		90	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±22	±5		±22	±5		±22	V
Power Supply Rejection Ratio										μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.0	2.8	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min								60	100	mW
T_A = max								75	115	mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	0		+70	-55		+125	°C
Storage	-65		+150	-65		+150	-65		+150	°C

NOTES

[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Temperature Range	Package[1]	Initial Off-Set Voltage
AD741CN	0 to +70°C	MINI-DIP (N8A)	6.0mV
AD741CH	0 to +70°C	TO-99	6.0mV
AD741JN	0 to +70°C	MINI-DIP (N8A)	3.0mV
AD741JH	0 to +70°C	TO-99	3.0mV
AD741KN	0 to +70°C	MINI-DIP (N8A)	2.0mV
AD741KH	0 to +70°C	TO-99	2.0mV
AD741LN	0 to +70°C	MINI-DIP (N8A)	0.5mV
AD741LH	0 to +70°C	TO-99	0.5mV
AD741H	-55°C to +125°C	TO-99	5.0mV
AD741SH	-55°C to +125°C	TO-99	2.0mV

NOTE

[1] See Section 19 for package outline information.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	AD741, J, K, L, S	AD741C
Supply Voltage	±22V	±18V
Internal Power Dissipation	500mW[1]	500mW
Differential Input Voltage	±30V	±30V
Input Voltage	±15V	±15V
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (soldering, 60 seconds)	300°C	300°C
Output Short Circuit Duration	Indefinite[2]	Indefinite

NOTES

[1] Rating applies for case temperature to +125°C. Derate TO-99 linearity at 6.5mW/°C for ambient temperatures above +70°C.

[2] Rating applies for shorts to ground or either supply at case temperatures to +125°C or ambient temperatures to +75°C.

Typical Performance Curves

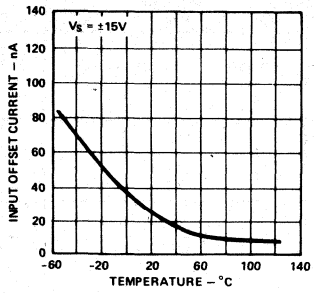


Figure 1. Offset Current vs. Temperature

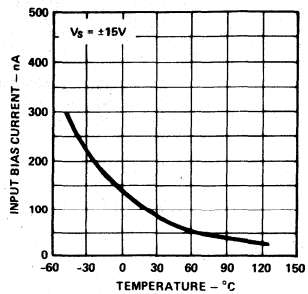


Figure 2. Bias Current vs. Temperature

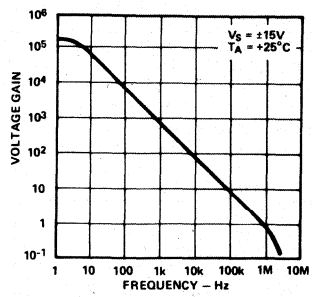


Figure 3. Open Loop Gain vs. Frequency

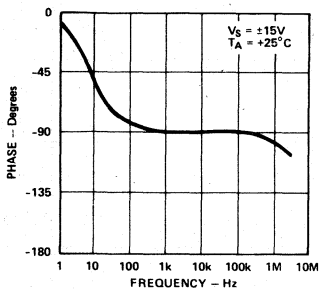


Figure 4. Open Loop Phase Response vs. Frequency

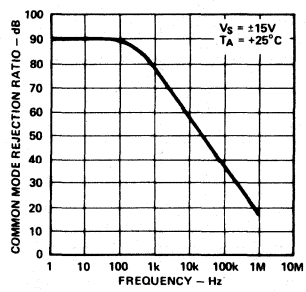


Figure 5. Common Mode Rejection vs. Frequency

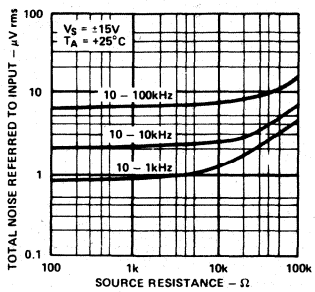


Figure 6. Broad Band Noise vs. Source Resistance

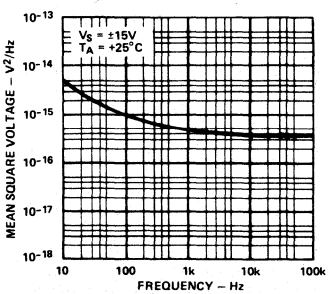


Figure 7. Input Noise Voltage vs. Frequency

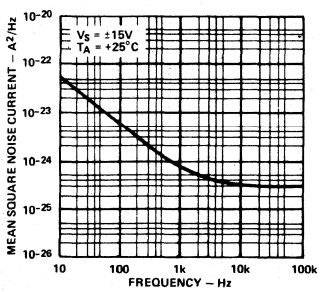


Figure 8. Input Noise Current vs. Frequency

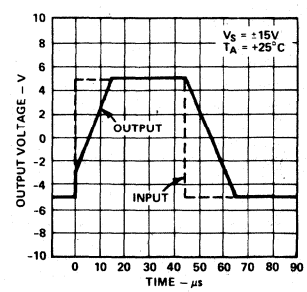


Figure 9. Voltage Follower Large Signal Pulse Response

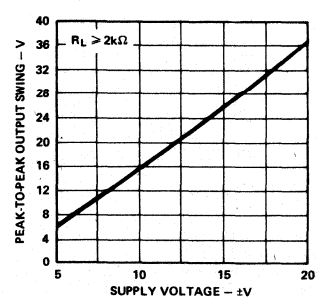


Figure 10. Output Voltage Swing vs. Supply Voltage

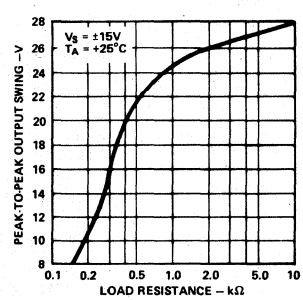


Figure 11. Output Voltage Swing vs. Load Resistance

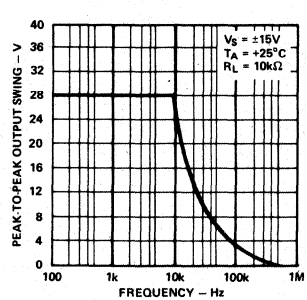


Figure 12. Output Voltage Swing vs. Frequency

Fast-Settling, Wideband, FET-Input Op Amp

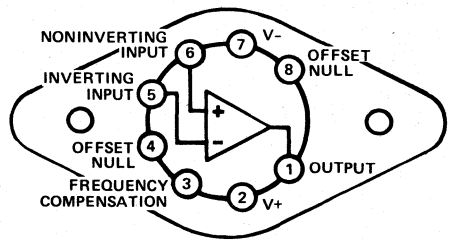
AD3554

4

FEATURES

Very High Slew Rate: 1000V/μs
Fast Settling: 150ns max to ±0.05%
Gain Bandwidth Product: 1.7GHz typical
High Output Current: 100mA min @ V_{OUT} = 10V
Full Differential Input

AD3554 FUNCTIONAL BLOCK DIAGRAM



TO-3 STYLE
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD3554 is a FET-input, hybrid operational amplifier that features an excellent combination of high slew rate, fast settling time and large gain-bandwidth product. The AD3554 has a full differential input with matched input FETs for low offset voltage.

The AD3554 can supply ±100mA at 10 volts. The slew rate is 1000V/μs minimum; 1200V/μs is typical. Settling time to ±0.05% of final value is only 150ns when configured as an inverting amplifier. The user can optimize the combination of bandwidth, slew rate, and settling time for a particular application by selecting the external compensation capacitor.

The AD3554 is recommended for any operational amplifier application where speed and bandwidth are important considerations. The high slew rate and fast settling time make the AD3554 an excellent choice for use in fast D/A converters, fast current amplifiers, integrators, waveform generators and multiplexer buffers.

The AD3554 is available in three versions: the "A" and "B" are specified over the -25°C to +85°C temperature range and "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed TO-3 style metal can.

The AD3554 is a pin-compatible replacement for 3554 devices from other manufacturers.

PRODUCT HIGHLIGHTS

1. The high slew rate (1000V/μs min) and fast settling time to 0.01% (250ns max) make the AD3554 ideal for D/A, A/D, sample-hold, and video instrumentation circuits.
2. Laser trimming techniques reduce initial offset voltage to as low as 1mV max (AD3554B), thus eliminating the need for external nulling in many applications.
3. Very high gain-bandwidth product (1.7GHz typical at A = 1000) makes the AD3554 an ideal choice for high frequency amplifier applications.
4. FET inputs result in a low bias current (50pA max, 10pA typ) in a high gain-bandwidth product operational amplifier.
5. Full differential input makes the AD3554 ideal for all standard operational amplifier applications such as high speed integrators, differentiators, and high gain amplifiers.
6. The 100mA at 10V output makes the AD3554 suitable for many applications that require high output power, such as cable drivers. The capacitance of coaxial cable (e.g., 29pF/foot for RG-58) does not load the AD3554 when the coaxial cable or transmission line is terminated in its characteristic impedance.

SPECIFICATIONS (typical @ T_{CASE} = +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD3554AM	AD3554BM	AD3554SM
OPEN LOOP GAIN			
No Load	106dB (100dB min)	*	*
R_L = 100Ω	96dB (90dB min)	*	*
OUTPUT CHARACTERISTICS			
Voltage @ I_O = ±100mA	±11V (±10V min)	*	*
Output Resistance, Open Loop @ f = 10MHz	20Ω		
Current @ V_O = ±10V	±125mA (±100mA min)	*	*
FREQUENCY RESPONSE			
Bandwidth (0dB, Small Signal, C_F = 0)[1]	90MHz (70MHz min)	*	*
Gain-Bandwidth Product, C_F = 0			
G = 10V/V	225MHz (150MHz min)	*	*
G = 100V/V	725MHz (425MHz min)	*	*
G = 1000V/V	1700MHz (1000MHz min)	*	*
Full Power Bandwidth, C_F = 0, V_O = 20V p-p,			
R_L = 100Ω	19MHz (16MHz min)	*	*
Slew Rate, C_F = 0, V_O = 20V p-p,			
R_L = 100Ω	1200V/μs (1000V/μs min)	*	*
Settling Time, A = −1, to ±1%	60ns	*	*
to ±0.1%	120ns	*	*
to ±0.05%	140ns (150ns max)	*	*
to ±0.01%	200ns (250ns max)	*	*
INPUT OFFSET VOLTAGE			
Initial Offset	0.5mV (2.0mV max)	0.2mV (1.0mV max)	**
vs. Temperature	20μV/°C (50μV/°C max)	8μV/°C (15μV/°C max)	12μV/°C (25μV/°C max)
vs. Supply, T_A = min to max	80μV/V (300μV/V max)	*	*
INPUT BIAS CURRENT			
Either Input[2]	10pA (50pA max)	*	*
Initial Difference	2pA (10pA max)	*	*
vs. Supply Voltage	1pA/V	*	*
INPUT IMPEDANCE			
Differential	10^{11}Ω‖2pF	*	*
Common Mode	10^{11}Ω‖2pF	*	*
INPUT VOLTAGE RANGE			
Max Safe Input Voltage, Diff	±(|V_{CC}|−8)	*	*
Common Mode	±(|V_{CC}|−4)	*	*
Common Mode Rejection, V_{CM} = +7V, −10V	78dB (60dB min)	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(7 to 18)V	*	*
Quiescent Current	28mA (45mA max)	*	*
INPUT NOISE[1]			
Voltage, f_o = 1Hz	125nV/√Hz (450nV/√Hz max)	*	*
f_o = 10Hz	50nV/√Hz (160nV/√Hz max)	*	*
f_o = 100Hz	25nV/√Hz (90nV/√Hz max)	*	*
f_o = 1kHz	15nV/√Hz (50nV/√Hz max)	*	*
f_o = 10kHz	10nV/√Hz (35nV/√Hz max)	*	*
f_o = 100kHz	8nV/√Hz (25nV/√Hz max)	*	*
f_o = 1MHz	7nV/√Hz (25nV/√Hz max)	*	*
f_B = 0.3Hz to 10Hz	2μV p-p (7μV p-p max)	*	*
f_B = 10Hz to 1MHz	8μV rms (25μV rms max)	*	*
Current, f_B = 3Hz to 10Hz	45fA p-p	*	*
f_B = 10Hz to 1MHz	2pA rms	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	−25°C to +85°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*
PACKAGE[3] — TO-3 Style (H08C)	AD3554AM	AD3554BM	AD3554SM

NOTES

[1] These parameters are untested and not guaranteed. This specification is established to a 90% confidence level.

[2] Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures, the current doubles every 10°C.

[3] See Section 19 for package outline information.

*Specifications same as AD3554AM.

**Specifications same as AD3554BM.

Specifications subject to change without notice.

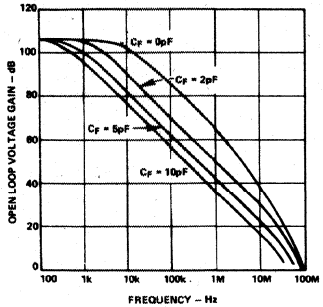


Figure 1. Open Loop Frequency Response (Voltage Gain)

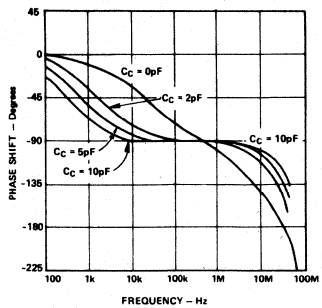


Figure 2. Open Loop Frequency Response (Phase Shift)

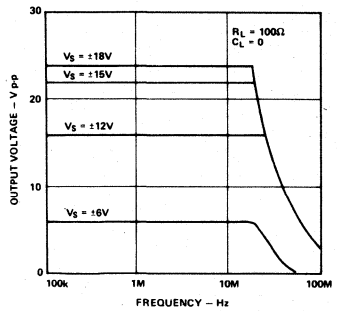


Figure 3. Output Voltage vs. Frequency

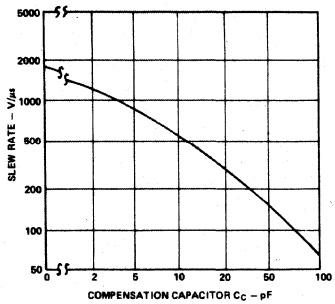


Figure 4. Slew Rate vs. Compensation

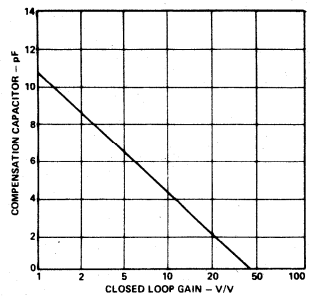


Figure 5. Recommended Compensation Capacitor vs. Closed Loop Gain

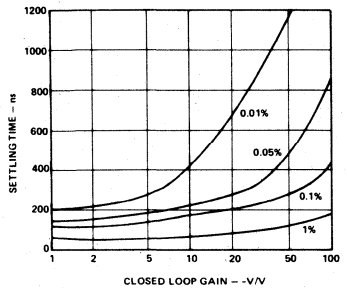


Figure 6. Settling Time vs. Closed Loop Gain (Circuit of Figure 18A)

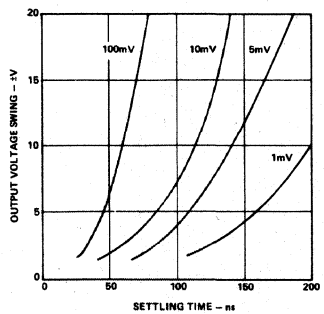


Figure 7. Settling Time vs. Output Voltage Change (Circuit of Figure 18A)

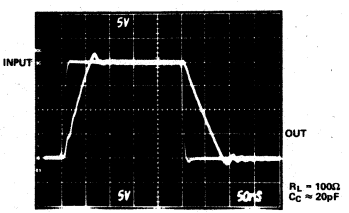


Figure 8. Voltage Follower Large Signal Response

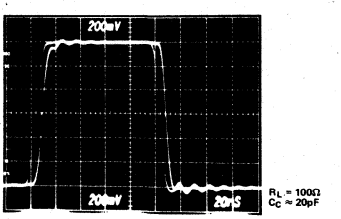


Figure 9. Voltage Follower Small Signal Response

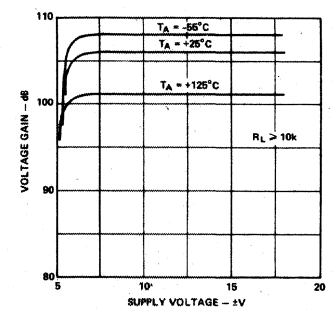


Figure 10. Open Loop Gain vs. Supply Voltage

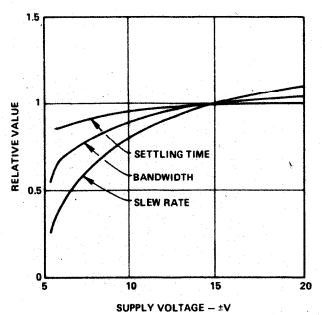


Figure 11. Dynamic Characteristics vs. Supply Voltage

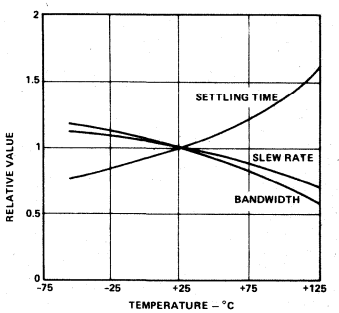


Figure 12. Dynamic Characteristics vs. Temperature

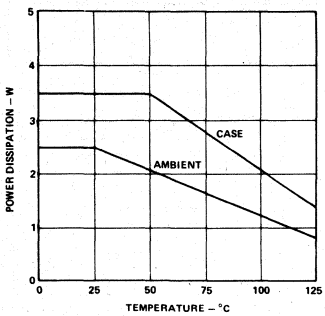


Figure 13. Power Dissipation vs. Temperature

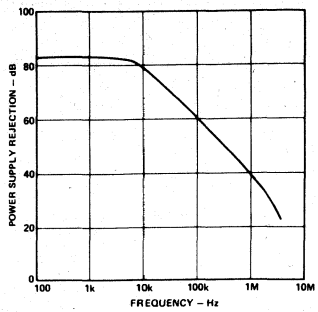


Figure 14. PSRR vs. Frequency

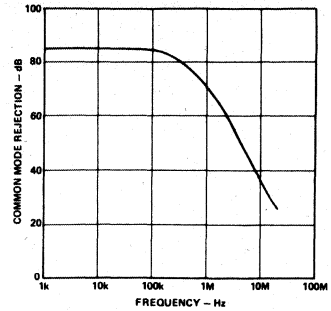


Figure 15. CMRR vs. Frequency

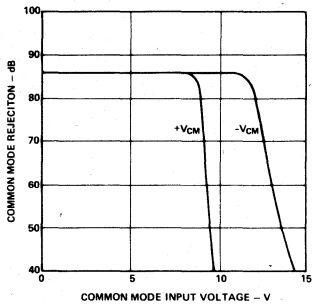


Figure 16. Common Mode Rejection vs. Input Voltage

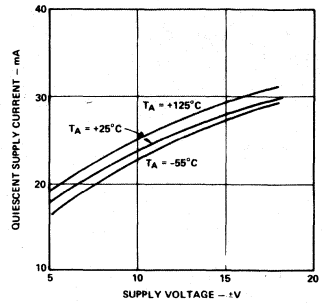


Figure 17. Quiescent Supply Current vs. Supply Voltage

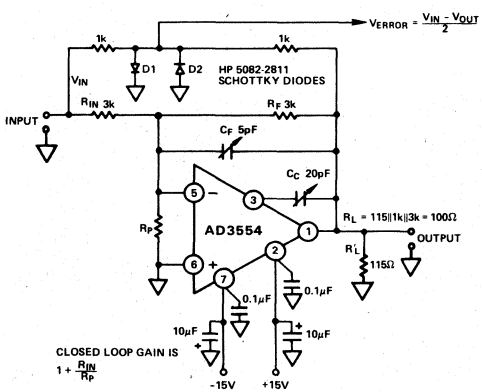


Figure 18A. Settling Time Test Circuit Schematic

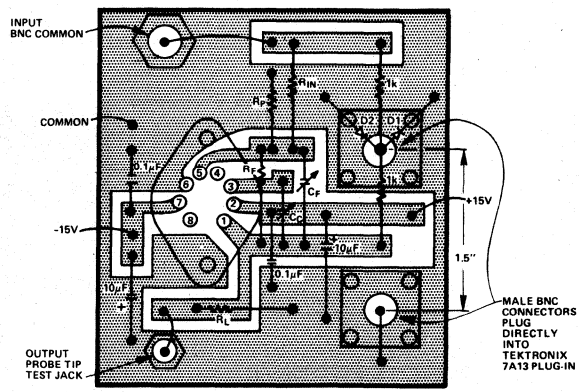


Figure 18B. Settling Time Test Circuit Layout

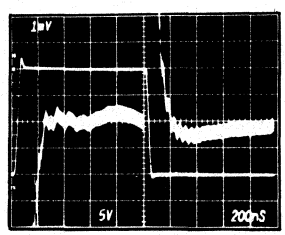


Figure 18C. Unity Gain Inverter Settling Time

LAYOUT CONSIDERATIONS

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling and stray capacitance.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical, particularly to the inverting input, which is especially sensitive to stray capacitances.

Low value resistors should be used to assure that the time constants formed with the circuit capacitances will not limit the amplifier performance. Resistor values less than 5.6kΩ are recommended.

Each power supply lead should be bypassed to ground as close as possible to the amplifier pins. A 10μF electrolytic or tantalum capacitor in parallel with a 0.01μF ceramic capacitor is recommended.

GROUNDING

Grounding the case will add a slight capacitance to each pin. Therefore, we recommend leaving the case ungrounded.

In inverting applications we recommend grounding the non-inverting input rather than connecting it to a bias current compensating resistor. FET input amplifiers do not require compensating resistors because of their low input bias currents.

GUARDING

In high input impedance applications the input terminals may be surrounded by a conductive path to divert leakage currents. This guard ring should be connected to a low impedance point at the input signal potential.

In high frequency applications guarding may not be desirable as it increases the risk of oscillation due to increased printed circuit board capacitance.

COMPENSATION

The user can optimize the bandwidth, slew rate, or settling time by selecting the external frequency compensation capacitor. No compensation capacitor is required for closed loop gains above 50 and when the load capacitance is less than 100pF. When driving capacitive loads greater than 470pF, in low closed loop gain configurations, connect a 1000pF capacitor between pin 8 and the positive supply. The performance may be improved by connecting a small resistor in series with the output and a small capacitor from pin 1 to 5. See Typical Circuits.

The flat high frequency response of the AD3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin.

The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed loop gain.

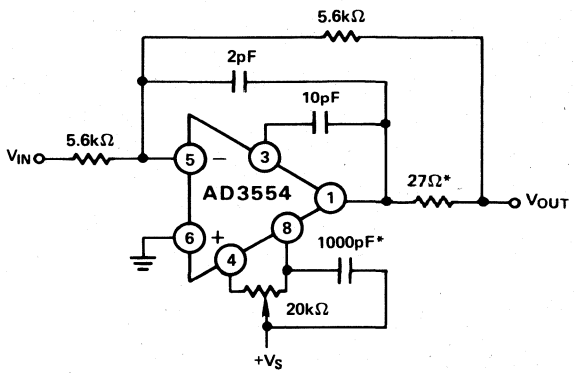
SHORT CIRCUIT PROTECTION

The AD3554 is short circuit protected for continuous output shorts to ground. Output shorts to either supply will destroy the device.

HEAT SINKING

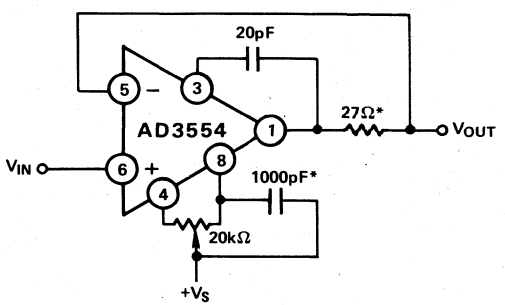
The AD3554 does not require heat sinking for most applications. However, at extreme temperature and full load conditions a heat sink will be necessary as indicated in the maximum power dissipation curve. We recommend connecting the heat sink to the amplifier case and keeping the combination ungrounded.

TYPICAL CIRCUITS



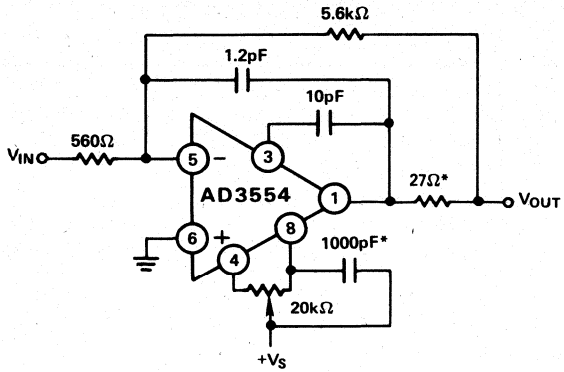
*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 19. Unity Gain Inverter



*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 20. Follower



*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 21. Inverting Gain of 10 Amplifier

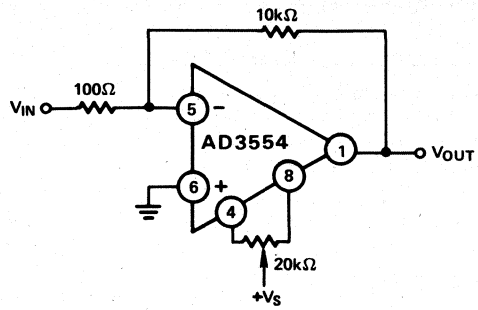


Figure 22. Inverting Gain of 100 Amplifier

AD9685/AD9687

FEATURES

2.2ns Propagation Delay – AD9685BD/BH
2.7ns Propagation Delay – AD9687BD
0.5ns Latch Set-Up Time
Pin-Compatible to Am685/687 but FASTER
+5V, −5.2V Supply Voltages

APPLICATIONS

Ultra-High-Speed A/D Converters
Ultra-High-Speed Line Receivers
Peak Detectors
Threshold Detectors

GENERAL DESCRIPTION

The AD9685BD/BH and AD9687BD are ultra-fast comparators manufactured with a high performance bipolar process which makes it possible to obtain incredibly short propagation delays and latch set-up times.

The AD9685BD/BH is a single comparator which is pin-compatible with the Am685, but has speed capabilities that far outstrip the earlier unit. The AD9687BD is pin-for-pin compatible with the Am687 and, like its predecessor, is a dual comparator; its speed capabilities are far superior to the Am687.

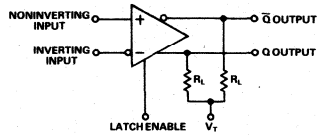
Both Analog Devices units have differential inputs and complementary outputs fully compatible with ECL logic levels. Their output current levels are capable of driving 50Ω terminated transmission lines, and their high resolution make them ideally suited for a variety of analog-to-digital signal processing applications.

AD9685BD/BH Single Comparator

A latch function allows the AD9685BD/BH to be operated in a sample-hold mode. When the Latch Enable (LE) is ECL HIGH, the comparator functions normally. When the Latch Enable is driven LOW, its outputs are locked in the logic state dictated by the input conditions at the time of the latch input transition. If the latch function is not used, the Latch Enable input should be connected to ground.

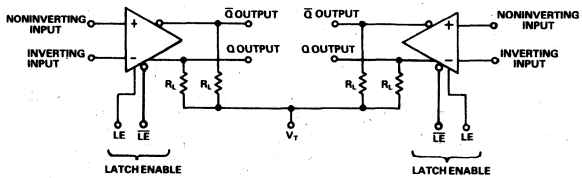
In addition to its speed advantages over the earlier Am685, the AD9685BD/BH also dissipates less power because it operates on a positive 5 volt supply instead of the 6 volts required by the AMD device.

AD9685BD/BH FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9687BD FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9687BD Dual Comparator

The latch function of the AD9687BD provides an ability to operate the unit in either a track-hold or sample-hold mode. The latch function inputs are separated on the two comparators and are designed to be driven from the complementary outputs of a standard ECL logic gate. When LE is High and $\overline{LE}$ is LOW, the normal comparator function is in operation. When LE is forced LOW and $\overline{LE}$ is driven HIGH, the outputs of the comparator being exercised are locked in their existing logical states, as determined by the input conditions present at the time of arrival of the latch signal. If the latch function is not used on either one of the two comparators in the AD9687BD, the appropriate Latch Enable input should be connected to ground; the companion $\overline{\text{Latch Enable}}$ input can be left open.

The AD9687BD is basically two AD9685BD/BH units in a single package and operates in a similar fashion to a pair of the single comparators.

SPECIFICATIONS (typical @ +25°C with nominal supply voltages unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS	AD9685BD/BH	AD9687BD
Supply Voltages (V_{CC} and V_{EE})	±6V	*
Power Dissipation	336mW	500mW
Input Voltage	±5V	*
Differential Input Voltage	3.5V	*
Output Current	30mA	*
Operating Temperature Range	−30°C to +85°C	*
Storage Temperature Range	−55°C to +150°C	*
Lead Temperature (soldering, 10 seconds)	300°C	*

ELECTRICAL CHARACTERISTICS	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage[1]	V_{OS}	−5		+5	*		*	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$		20			*		µV/°C
Input Offset Current	I_{OS}			5			*	µA
Input Bias Current	I_B		10	20		*	*	µA
Input Voltage Range	V_{CM}	−2.5		+2.5	*		*	V
Common Mode Rejection Ratio	CMRR	80			*			dB
Input Resistance	R_{IN}	60			*			kΩ
Input Capacitance	C_{IN}		3			*		pF
Input/Output Logic Levels								
Output HIGH Voltage	V_{OH}	−0.96		−0.81	*		*	V
Output LOW Voltage	V_{OL}	−1.85		−1.65	*		*	V
Positive Supply Voltage	V_{CC}	+4.75	+5	+5.25	*	*	*	V
Negative Supply Voltage	V_{EE}	−4.95	−5.2	−5.45	*	*	*	V
Positive Supply Current	I_{CC}		19	23		30		mA
Negative Supply Current	I_{EE}		23	34		54		mA
Supply Voltage Rejection Ratio	S_{VRR}		60			*		dB
Power Dissipation	P_{DISS}		210	300		430		mW
SWITCHING CHARACTERISTICS								
Propagation Delays[2]								
Input to Output HIGH	$t_{pd}+$		2.2	3		2.7	4	ns
Input to Output LOW	$t_{pd}-$		2.2	3		2.7	4	ns
Latch Enable to Output HIGH	$t_{pd}+(E)$		2.5	3		2.7	4	ns
Latch Enable to Output LOW	$t_{pd}-(E)$		2.5	3		2.7	4	ns
Latch Enable								
Pulse Width	$t_{pw}(E)$	3	2		*	*		ns
Minimum Set-Up Time	t_s		0.5	1		*	*	ns
Minimum Hold Time	t_h			1			*	ns

NOTES
[1] R_S = 100 ohms
[2] Propagation delays measured with 100mV pulse; 5mV overdrive.
*Specifications same as AD9685BD/BH.
Specifications subject to change without notice.

DEFINITION OF TERMS

V_{OS} INPUT OFFSET VOLTAGE – The potential difference required between the input terminals to obtain zero potential difference between the outputs.

I_{OS} INPUT OFFSET CURRENT – The difference between the currents into the inputs when there is zero potential difference between the outputs.

I_B INPUT BIAS CURRENT – The average of the two input currents. This is a chip design trade-off parameter. Internally, it is desirable to have high values of I_B for circuit performance requirements; externally, it is desirable to have I_B as low as possible.

V_{CM} INPUT VOLTAGE RANGE – The range of input voltages for which offset and propagation delay specifications are valid.

CMRR COMMON MODE REJECTION RATIO – The ratio of input voltage range to the peak-to-peak change in input offset voltage over that range.

R_{IN} INPUT RESISTANCE – The resistance looking into either terminal with the other grounded.

C_{IN} INPUT CAPACITANCE – The capacitance looking into either input pin with the other grounded.

V_{OH} OUTPUT HIGH VOLTAGE – The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} OUTPUT LOW VOLTAGE – The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I_{CC} POSITIVE SUPPLY CURRENT – The current required from the positive supply to operate the comparator.

I_{EE} NEGATIVE SUPPLY CURRENT – The current required from the negative supply to operate the comparator.

S_{VRR} SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

P_{DISS} POWER DISSIPATION – The power dissipated by the comparator with both outputs terminated in 50 ohms to −2V.

$t_{pd}+$ INPUT TO OUTPUT HIGH DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

$t_{pd}-$ INPUT TO OUTPUT LOW DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd}+(E)$ LATCH ENABLE TO OUTPUT HIGH DELAY – The propagation delay measured from the 50% point of the Latch Enable (LE) signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd}-(E)$ LATCH ENABLE TO OUTPUT LOW DELAY – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

$t_{pw}(E)$ MINIMUM LATCH ENABLE PULSE WIDTH – The minimum time the Latch Enable signal must be HIGH to acquire and hold an input signal.

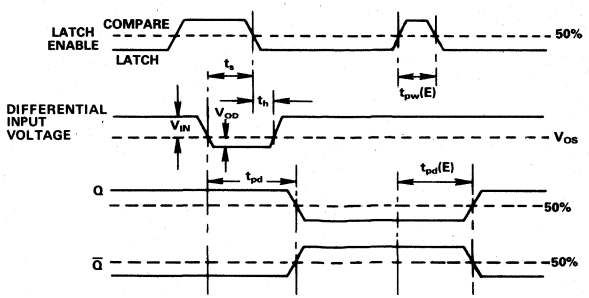
t_s MINIMUM SET-UP TIME – The minimum time before the negative transition of the Latch Enable pulse that an input signal must be present to be acquired and held at the outputs.

t_h MINIMUM HOLD TIME – The minimum time after the negative transition of the Latch Enable signal that an input signal must remain unchanged to be acquired and held at the outputs.

OTHER SYMBOLS

T_C	Case Temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_S	Supply voltages	V_{IN}	Input pulse amplitude
V_{CC}	Positive supply voltage	V_{OD}	Input overdrive
V_{EE}	Negative supply voltage	f	Frequency

TIMING DIAGRAM



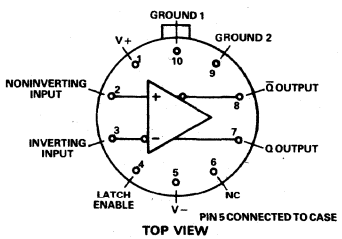
The Timing Diagram illustrates a series of events in the AD9685BD/BH; the terms and their relationships are also valid for the AD9687BD. The relationships which are shown should not be interpreted as "typical", since several parameters have multiple values; and the worst case conditions are shown in the Timing Diagram.

The top line of the diagram shows two Latch Enable (LE) pulses; each is high for "compare" and low for "latch". The first pulse illustrates the compare function in which part of the input action takes place during the "compare" mode. The second one illustrates a compare function interval during which there is no change in input.

The leading edge of the input signal, shown here as a large amplitude, small overdrive pulse, switches the comparator after a time interval t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch trailing (falling) edge and, to be acquired, must be maintained for a time t_h after that edge. After t_h, the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of tpw(E) is required for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.

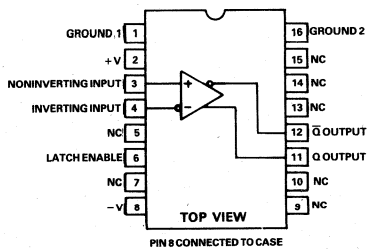
PIN CONFIGURATIONS

TO-100



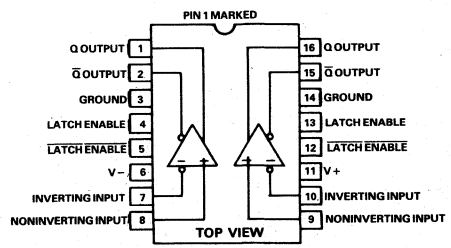
AD9685BH Pin Configuration Package Option[1] — TO-100

DIP



AD9685BD Pin Configuration Package Option[1] — Q16C

DIP



AD9687BD Pin Configuration Package Option[1] — D16A

NOTE
[1] See Section 19 for package outline information.

ANALOG DEVICES

Ultra Fast FET Operational Amplifier

ADLH0032G/ADLH0032CG

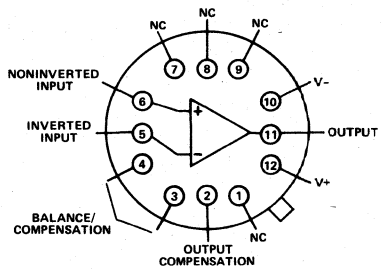
FEATURES

- 2nd Source; Replaces All LH0032G
- High Slew Rate; 500V/μs
- Wide 70MHz Bandwidth
- Operation Guaranteed -55°C to +125°C (ADLH0032G)
- High Input Impedance of $10^{12}\Omega$
- 2mV Input Offset Voltage

APPLICATIONS

- High Speed DAC Comparators
- ADC and SHA Input Buffers
- High Speed Integrators
- Video Amplifiers

ADLH0032G/ADLH0032CG
PIN DESIGNATIONS



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The ADLH0032G and ADLH0032CG are high slew rate, high input impedance, differential operational amplifiers, suitable for numerous applications in high-speed signal processing. These second source devices are the same in every characteristic as other LH0032G/LH0032CG amplifiers, and thus are particularly suited for comparator applications due to their high allowable differential input capabilities (±15V), ease of output clamping, and high output drive capabilities.

Featuring a wide 70MHz bandwidth, high input impedance ($10^{12}\Omega$), and high output drive capacity, the ADLH0032G and ADLH0032CG have already been designed into such applications as summing amplifiers in high-speed DACs, Buffer Amps in ADCs and high-speed SHAs, as well as other applications normally reserved for special purpose video amplifiers.

The ADLH0032G is guaranteed over the extended temperature range from -55°C to +125°C, while the commercial grade ADLH0032CG is guaranteed from -25°C to +85°C. Both devices are packaged in a TO-8 metal can package.

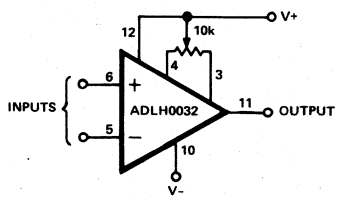


Figure 1. Offset Null

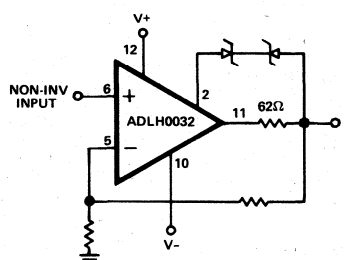


Figure 2. Output Short Circuit Protection

SPECIFICATIONS

Model **ADLH0032G, ADLH0032CG**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±18V
Power Dissipation		See Characteristic Curves
Differential Input Voltage		±30V
Input Voltage		$\pm V_S$
Operating Temperature Range	ADLH0032G	-55°C to +125°C
	ADLH0032CG	-25°C to +85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (soldering, 10sec)		300°C

Parameter	Conditions	ADLH0032G min	ADLH0032G typ	ADLH0032G max	ADLH0032CG min	ADLH0032CG typ	ADLH0032CG max	Units
DC ELECTRICAL CHARACTERISTICS[1]								
Input Offset Voltage[2]	T_J = +25°C		2	5 10		5	15 20	mV
Input Offset Current[2]	T_J = +25°C		5	25 25		10	50 5	pA nA
Input Bias Current[2]	T_J = +25°C		10	100 50		25	200 15	pA nA
Average Offset Voltage Drift			25	50		25	50	µV/°C
Large Signal Voltage Gain	V_{OUT} = ±10V, F = 1kHz, R_L = 1kΩ, T_C = +25°C V_{OUT} = ±10V, R_L = 1kΩ, F = 1kHz	60 57	70		60 57	70		dB dB
Input Voltage Range		±10	±12		±10	±12		V
Output Voltage Swing	R_L = 1kΩ	±10	±13.5		±10	±13		V
Power Supply Rejection Ratio	ΔV_S = ±10V	50	60		50	60		dB
Common Mode Rejection Ratio	ΔV_{IN} = 10V	50	60		50	60		dB
Supply Current	T_C = +25°C		18	20		20	22	mA
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	A_V = +1, ΔV_{IN} = 20V	350	500		350	500		V/µs
Settling Time to 1% of Final Value	A_V = -1, ΔV_{IN} = 20V		100			100		ns
Settling Time to 0.1% of Final Value	A_V = -1, ΔV_{IN} = 20V		300			300		ns
Small Signal Rise Time	A_V = +1, ΔV_{IN} = 1V		8	20		8	20	ns
Small Signal Delay Time	A_V = +1, ΔV_{IN} = 1V		10	25		10	25	ns
MTBF Meantime Between Failures	1.0608 X 10^7 Hours							
PACKAGE OPTION[4]			H12A			H12A		

NOTES

[1] These specifications apply for V_S = ±15V and -55°C to +125°C for the ADLH0032G and -25°C to +85°C for the ADLH0032CG.

[2] Due to high speed automatic test techniques employed these parameters are correlated to junction temperature.

[3] These specifications apply for V_S = ±15V, R_L = 1kΩ, T_C = +25°C.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range
ADLH0032CG	-25°C to +85°C
ADLH0032G	-55°C to +125°C

POWER SUPPLY DECOUPLING

The ADLH0032G/ADLH0032CG, like most high-speed circuits, are sensitive to stray capacitances and layout. Power supplies should be bypassed as near to ±V (Pins 10 and 12) as possible, using low inductance capacitors such as 0.01μF disc ceramics. Components for compensation should also be located close to the appropriate pins to reduce stray capacitances. A large ground plane area for low-impedance ground paths is highly recommended.

HEAT SINKING

The ADLH0032G/ADLH0032CG are specified for operation without any heat sink. Since internal power dissipation does create a significant temperature rise, improved bias current performance can be achieved by using a small heat sink such as the Thermalloy 2241 or equivalent. Since the case of the ADLH0032G/ADLH0032CG has no internal connection, it may be electrically connected to the heat sink. This, however, will affect the stray capacitances to all pins, therefore requiring adjustment of all circuit compensation values.

INPUT CAPACITANCE

Inverting Input:

For optimum performance, the inverting input should be compensated by a small capacitance, around 10pF, across the feedback resistor. This is because the 5pF input capacitance may cause significant time constants with high-value resistors. The capacitor value may be changed somewhat depending on the effects of layout and closed loop gain.

Noninverting Input:

To divert leakage currents away from the noninverting input and to reduce the effective input capacitance, it is desirable to bootstrap the case and/or a guard conductor to the inverting input. The resulting input capacitance of a unity gain follower configured this way will be less than 1 picofarad.

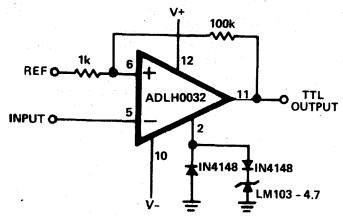


Figure 3. High Impedance, High Speed Comparator

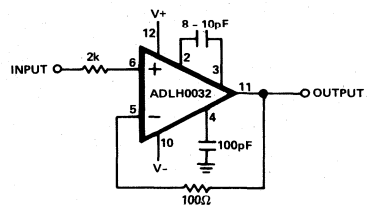


Figure 5. Unity Gain Follower

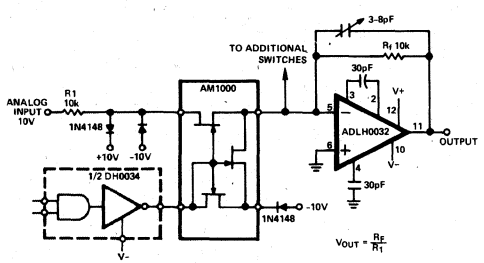


Figure 4. Current Mode Multiplexer

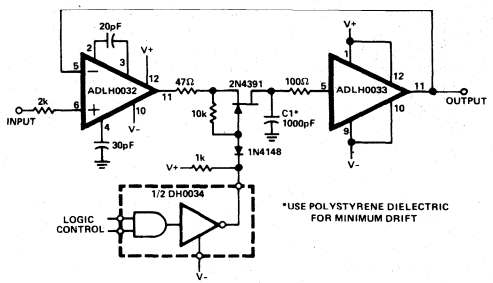
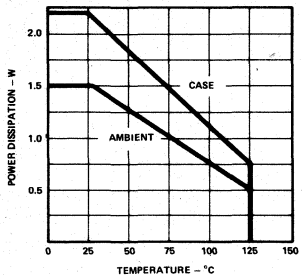
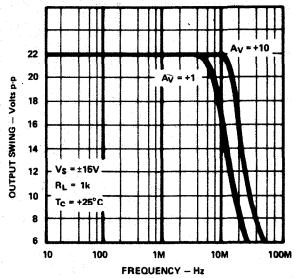


Figure 6. High Speed Sample and Hold

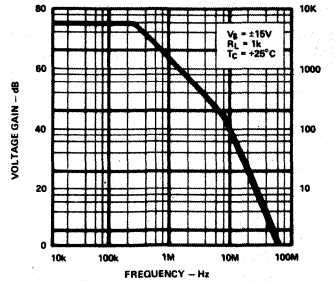
Typical Performance Curves



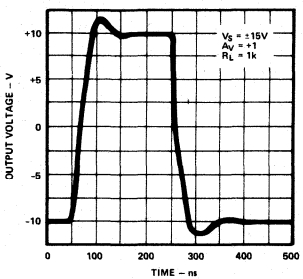
Maximum Power Dissipation



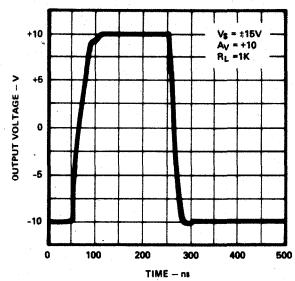
Large Signal Frequency Response



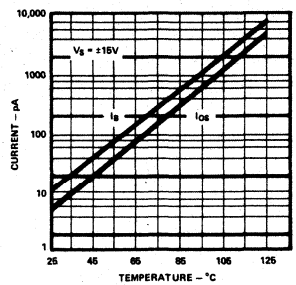
Open Loop Frequency Response



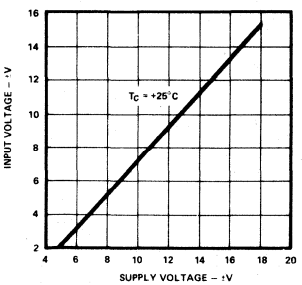
Large Signal Pulse Response



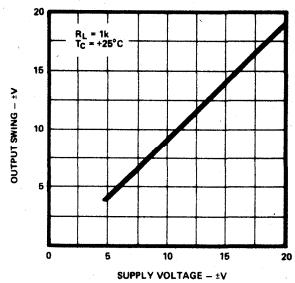
Large Signal Pulse Response



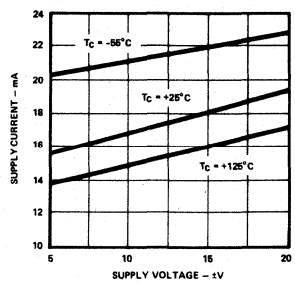
Input Bias and Offset Current vs. Temperature



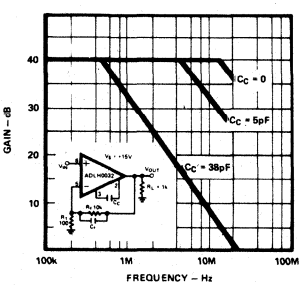
Input Voltage Range



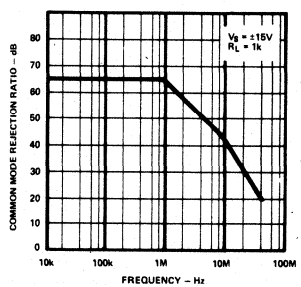
Output Swing



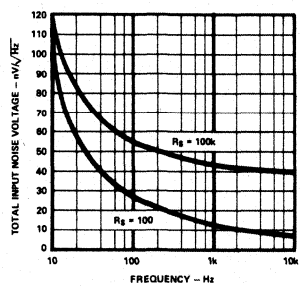
Supply Current vs. Supply Voltage



Closed Loop Frequency Response



Common Mode Rejection Ratio vs. Frequency



Total Input Noise Voltage vs. Frequency *Includes Contribution From Source Resistance*

ADLH0033G/ADLH0033CG

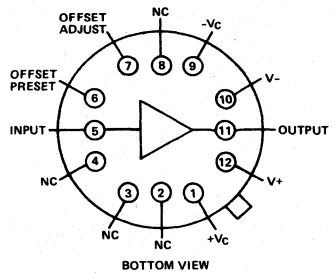
FEATURES

- 2nd Source–Replaces All LH0033G Series
- Wide Bandwidth–dc to 100MHz
- High Slew Rate–1500V/μs
- Operates on Single or Dual Power Supplies
- Operation Guaranteed -55°C to +125°C (ADLH0033G)
- High $10^{11}\ \Omega$ Input Impedance

APPLICATIONS

- High-Speed Line Drivers
- Video Impedance Transformation
- High-Speed A/D Input Buffers
- Nuclear Instrumentation Amplifiers
- Coaxial Cable Drive

ADLH0033G/ADLH0033CG
PIN DESIGNATIONS



TO-8 PACKAGE

GENERAL DESCRIPTION

The ADLH0033G and ADLH0033CG are superhigh speed (1500V/μs slew rate) and high input impedance ($10^{11}\ \Omega$) buffer amplifiers, designed to replace all LH0033 series amplifiers in applications such as high-speed line drivers or as high impedance buffers for fast A/D converters and comparators.

The ADLH0033G and ADLH0033CG are rated for operation over the voltage range of ±5V to ±20V. The ADLH0033G is guaranteed over the temperature range of -55°C to +125°C, while the commercial grade ADLH0033CG is guaranteed over the range of -25°C to +85°C.

Guaranteed operation over temperature of the ADLH0033G is achieved by using specially selected junction FET's and the latest state-of-the-art laser trimming techniques. They are available in the industry standard 12 pin TO-8 metal can.

OPERATION WITHIN AN OP AMP LOOP

When using the ADLH0033G/ADLH0033CG as a current booster or isolation buffer with op amps such as LH0032, 118, 741, etc., an isolation resistor of at least 47Ω must be used between the op amp's output and the input of the ADLH0033G.

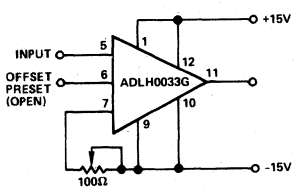


Figure 1. Offset Adjustment

HEAT SINKING

To assure maximum output drive capability of the ADLH0033G/ADLH0033CG over temperature, heat sinks should be used. The cases are electrically isolated from the circuit and thus may be connected to system grounds.

POWER SUPPLY BYPASSING

To prevent oscillation, power supply bypassing is recommended. Use low-inductance ceramic disc caps, keeping lead lengths as short as possible (1/4" to 1/2" max from device package), connected between ground plane and each supply lead. Use one or two 0.1μF caps in parallel with a 4.7μF tantalum for best results.

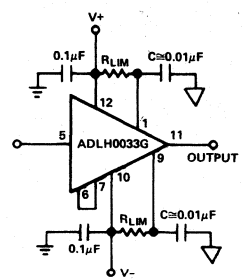


Figure 2. Short Circuit Protection Using Current Limiting Resistors (R_{LIM})

SPECIFICATIONS

	ADLH0033G	ADLH0033CG
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage (V+ – V–)	40V	
Maximum Power Dissipation (see curves)	1.5W	
Maximum Junction Temperature	175°C	
Input Voltage	Equal to Supplies	
Continuous Output Current	±100mA	
Peak Output Current	±250mA	
Operating Temperature ADLH0033G	–55°C to +125°C	
ADLH0033CG	–25°C to +85°C	
Storage Temperature Range	–65°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	300°C	

		ADLH0033G			ADLH0033CG			
Parameter	**Conditions**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Units**
DC ELECTRICAL CHARACTERISTICS[1,2]								
Input Bias Current	T_C = 25°C		0.1	0.15		0.15		nA
				10			5	nA
Input Impedance	R_L = 1kΩ	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Voltage Gain	V_{IN} = 1V rms, f = 1kHz, R_L = 1kΩ, R_S = 100kΩ	0.96	0.98	1.0	0.96	0.98	1.0	V/V
Output Offset Voltage	R_S = 100kΩ, T_C = 25°C		5	10		12	20	mV
	R_S = 100kΩ			15			25	mV
Output Offset Voltage TC	R_S = 100kΩ		50	100		50	100	μV/°C
Output Impedance	V_{IN} = 1V rms, f = 1kHz		6	10		6	10	Ω
	R_S = 100kΩ, R_L = 1kΩ							
Output Voltage Swing	R_L = 1kΩ	±12	±13		±12	±13		V
	R_L = 100Ω, T_C = 25°C	±9			±9			V
	V_S = ±5V, R_L = 1kΩ		6			6		V p-p
Supply Current	V_{IN} = 0V, V_S = ±15V		20	25		21	25	mA
	V_S = ±5V		18			18		mA
Power Consumption	V_{IN} = 0V, V_S = ±15V		600	660		630	720	mW
	V_S = ±5V		180			180		mW
AC ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 1kΩ)								
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1V rms		100			100		MHz
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Rise Time	ΔV_{IN} = 0.5V		2.9			3.2		ns
Propagation Delay	ΔV_{IN} = 0.5V		1.2			1.5		ns
Harmonic Distortion	f>1kHz		<0.1			<0.1		%
MTBF								
Meantime Between Failure	1.962×10^7 hours							
PACKAGE OPTION[3]			H12A			H12A		

NOTES

[1] Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, –15V applied to pins 9 and 10, and pin 6 connected to pin 7.

[2] Unless otherwise noted, specifications apply over a temperature range, $-55°C \leq T_C \leq +125°C$ for the ADLH0033G, and $-25°C \leq T_C \leq +85°C$ for the ADLH0033CG. Typical values shown are for T_C = 25°C.

[3] See Section 19 for package outline information.

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range
ADLH0033CG	–25°C to +85°C
ADLH0033G	–55°C to +125°C

LAYOUT CONSIDERATIONS

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling, stray capacitance, and the like.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical.

OFFSET ADJUSTMENT

The ADLH0033G/ADLH0033CG are factory trimmed for output voltage offsets well within the guaranteed limits, thereby eliminating the need to calibrate each device individually. To use this feature, simply connect Pin 6 (OFFSET PRESET) to Pin 7 (OFFSET ADJUST).

When it is desirable to eliminate any errors due to output offsets, the circuit of Figure 1 may be used to adjust these errors to zero.

SHORT CIRCUIT PROTECTION

The circuit of Figure 2 is used to protect the ADLH0033G/ADLH0033CG from short circuits on the output. The value of R_{LIM} is determined by the following:

$$R_{LIM} \cong \frac{V+}{I_{sc}} = \frac{V-}{I_{sc}}$$

Where I_{sc} = Output Current under short circuit conditions $\leq$100mA.

Note that output voltage swing will also be somewhat limited in this configuration; however, decoupling of Pins 1 and 9 through disc type capacitors to ground as shown in Figure 2 will restore full output swing for transient pulses.

OPERATION WITH ASYMMETRICAL SUPPLIES

Since Symmetrical Power Supplies may not always be desirable or available, the ADLH0033G/ADLH0033CG is designed to operate on Asymmetrical Supplies. This causes an apparent output offset; however, this is because of the amplifier's gain of less than unity. To accurately predict the output voltage shift due to Asymmetrical Supplies, use the following formula:

$$A_{VO} \cong (1 - A_V)\frac{(V+ - V-)}{2} = 0.005\ (V+ - V-)$$

Where A_V = No Load Voltage Gain, typically 0.99
V+ = Positive Supply Voltage
V- = Negative Supply Voltage

Of course, these apparent offsets may be adjusted to zero by using the circuit shown in Figure 1, OFFSET ADJUSTMENT.

CAPACITIVE LOADING

The ADLH0033G/ADLH0033CG have been designed to drive capacitive loads of several thousand picofarads (such as coaxial cable) without oscillation. In these applications, peak current resulting from (C X dv/dt) should be limited below the absolute maximum peak current rating of ±250mA.

Also, power dissipation due to driving capacitive loads plus standby power should be kept below the total power rating of 1.5W.

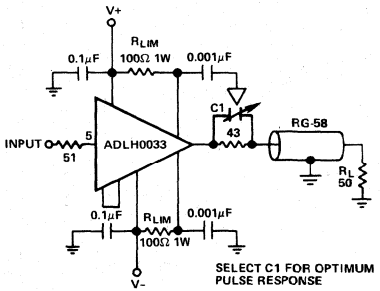


Figure 5. Coaxial Cable Drive

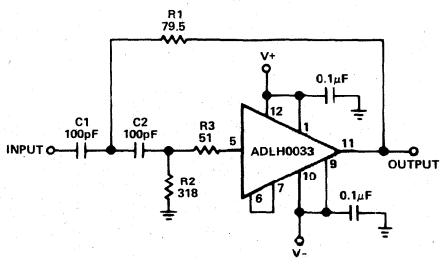


Figure 6. Wideband Two Pole High Pass Filter

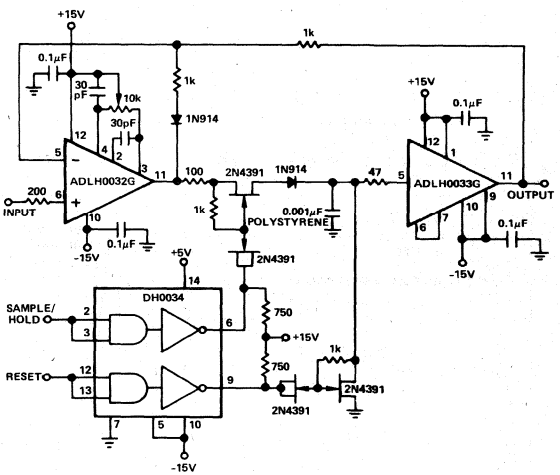


Figure 7. High Speed Peak Detector

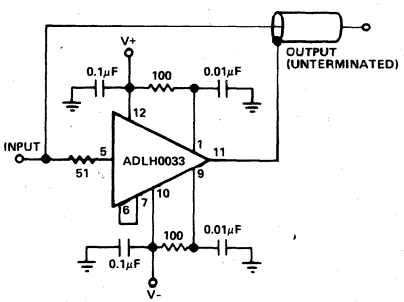
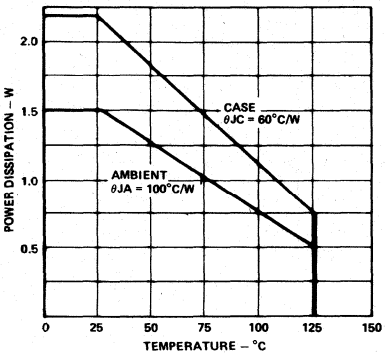
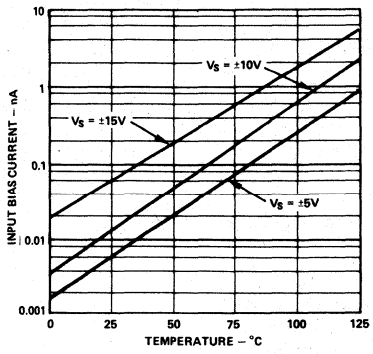


Figure 8. High Speed Shield/Line Driver

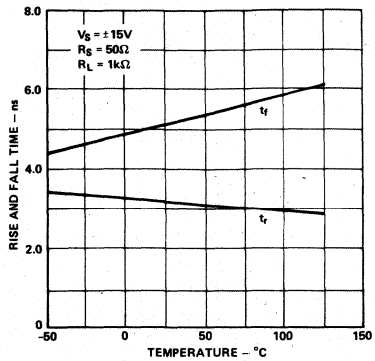
Typical Performance Curves



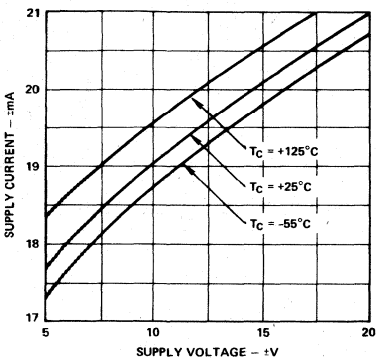
Power Dissipation vs Temperature



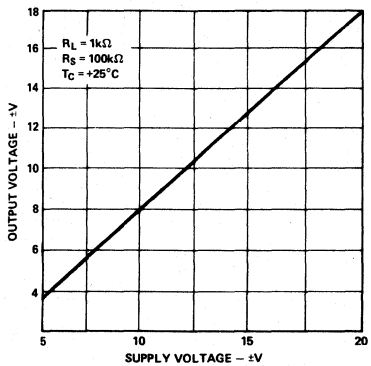
Input Bias Current vs Temperature



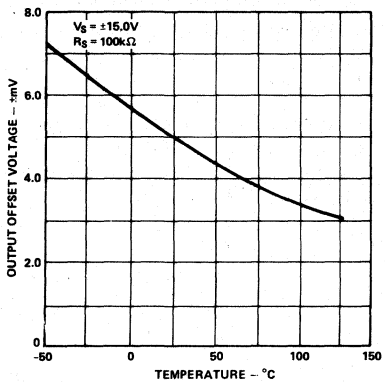
Rise and Fall Time vs Temperature



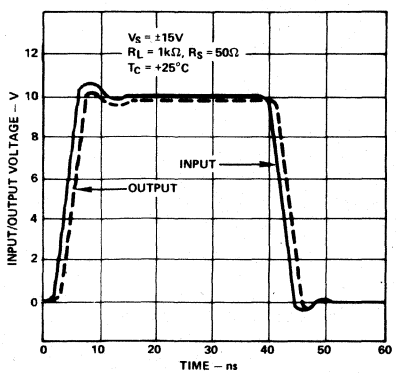
Supply Current vs Supply Voltage



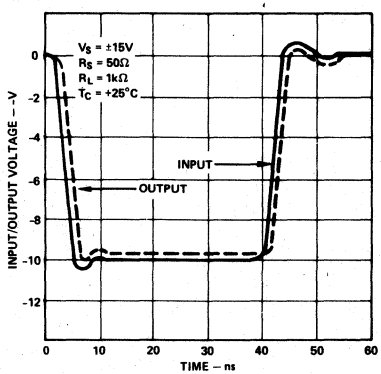
Output Voltage vs Supply Voltage



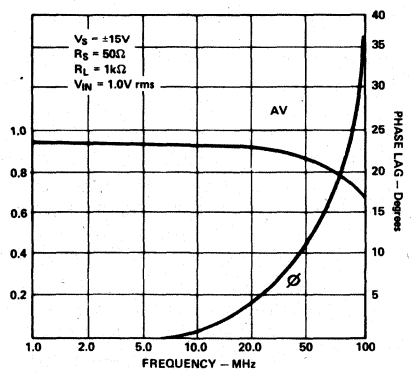
Output Offset Voltage vs Temperature



Positive Pulse Response



Negative Pulse Response



Frequency Response

ANALOG DEVICES

Ultra-Low Offset Voltage Op Amp

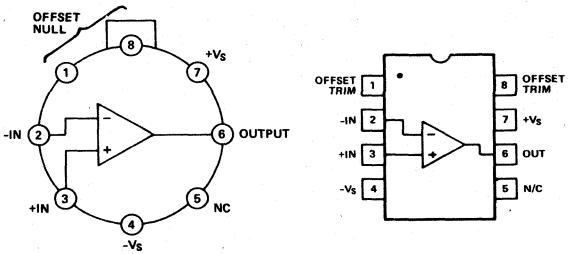
AD OP-07

4

FEATURES

Ten Times More Gain Than Other OP-07 Devices (3.0M min)
Ultra-Low Offset Voltage: 10μV
Ultra-Low Offset Voltage Drift: 0.2μV/°C
Ultra-Stable vs. Time: 0.2μV/month
Ultra-Low Noise: 0.35μV p-p
No External Components Required
Monolithic Construction
High Common Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A Sockets

AD OP-07 FUNCTIONAL BLOCK DIAGRAM



H-PACKAGE N-PACKAGE

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed loop gain applications. Input offset voltages as low as 10μV, bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C and long-term stability of 0.2μV/month eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common mode input voltage range (±14V) high common mode rejection ratio (up to 126dB) and high differential input impedance (50MΩ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. The devices are packaged in either TO-99 hermetically-sealed metal cans or plastic 8-pin mini DIPS.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultra-low offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultra-low input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-07E			AD OP-07C			AD OP-07D		
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
OPEN LOOP GAIN	A_{VO}	2,000	5,000		1,200	4,000		1,200	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	±12.5	±13.0		±12.0	±13.0		±12.0	±13.0	
		±12.0	±12.8		±11.5	±12.8		±11.5	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	75		60	150		60	150
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift							(Note 2)			(Note 2)
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	(Note 2) 2.0		0.5	(Note 2) 3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	3.8		0.8	6.0		0.8	6.0
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8 (Note 2)	35		12 (Note 2)	50		12 (Note 2)	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	±4.0		±1.8	±7.0		±2.0	±12
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13 (Note 2)	35		18 (Note 2)	50		18 (Note 2)	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{IN} CM		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	±13.0	±14.0		±13.0	±14.0		±13.0	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common Mode Rejection Ratio	CMRR	106	123		100	120		94	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	4.0		3.5	5.0		3.5	5.0
Power Consumption	P_D		90	120		105	150		105	150
			6.0	8.4		6.0	8.4		6.0	8.4
Rejection Ratio	PSRR	94	107		90	104		90	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70
PACKAGE OPTION[4]										
"N" Package										
8-Pin MINI DIP – (N8A)			AD OP-07EN			AD OP-07CN			AD OP-07DN	
"H" Package										
TO-99 – (H08B)			AD OP-07EH			AD OP-07CH			AD OP-07DH	

NOTES

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, AD OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.

[2] Parameter is not 100% tested; 90% of units meet this specification.

[3] Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the intitial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested: 90% of units meet this specification.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

AD OP-07AH			AD OP-07H				
MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**TEST CONDITIONS**	**UNITS**
3,000	5,000		**2,000**	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		**1,500**	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		**300**	1,000		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		**±12.5**	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		**±12.0**	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		**±10.5**	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		**±12.0**	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	**25**		30	**75**	Note 1	μV
	25	**60**		60	**200**	Note 1, T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	**0.6**		0.3	**1.3**	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 3	μV/Month
	0.3	**2.0**		0.4	**2.8**		nA
	0.8	**4.0**		1.2	**5.6**	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	**±2.0**		±1.0	**±3.0**		nA
	±1.0	**±4.0**		±2.0	**±6.0**	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz, Note 2	μV p-p
	10.3	18.0		10.3	18.0	f_O = 10Hz, Note 2	nV/√Hz
	10.0	13.0		10.0	13.0	f_O = 100Hz, Note 2	nV/√Hz
	9.6	11.0		9.6	11.0	f_O = 1kHz, Note 2	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz, Note 2	pA p-p
	0.32	0.80		0.32	0.80	f_O = 10Hz, Note 2	pA/√Hz
	0.14	0.23		0.14	0.23	f_O = 100Hz, Note 2	pA/√Hz
	0.12	0.17		0.12	0.17	f_O = 1kHz, Note 2	pA/√Hz
±13.0	±14.0		**±13.0**	±14.0			V
±13.0	±13.5		**±13.0**	±13.5		T_{min} to T_{max}	V
110	126		**110**	126		V_{CM} = ±CMVR	dB
106	123		**106**	123		V_{CM} = ±CMVR, T_{min} to T_{max}	dB
	3.0	**4.0**		3.0	**4.0**	$V_S = \pm 15V$	mA
	90	120		90	120	$V_S = \pm 15V$	mW
	6.0	8.4		6.0	8.4	$V_S = \pm 3V$	mW
100	110		**100**	110		$V_S = \pm 3V$ to $\pm 18V$	dB
94	106		**94**	106		$V_S = \pm 3V$ to $\pm 18V$, T_{min} to T_{max}	dB
-55		+125	-55		+125		°C
	—			—			
	AD OP-07AH			AD OP-07H			

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

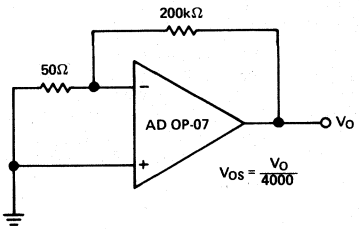
Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-07A, OP-07	-55°C to +125°C
OP-07E, OP-07C, OP-07D	0 to +70°C
Lead Temperature Range (Soldering, 60sec)	300°C

NOTES:

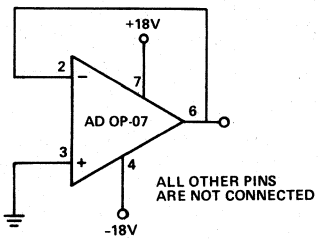
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.



Offset Voltage Test Circuit



Burn-In Circuit

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

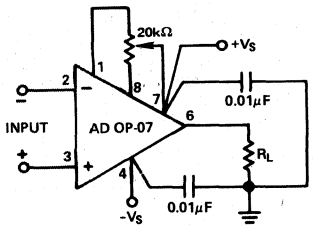


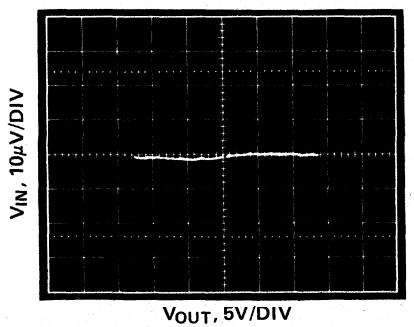
Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

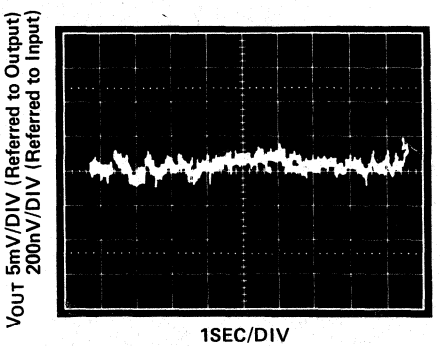
Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

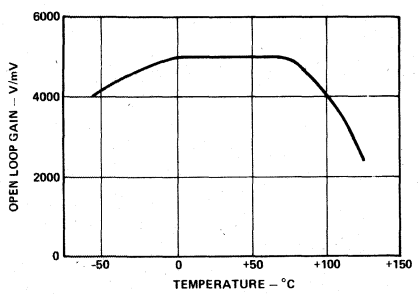
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



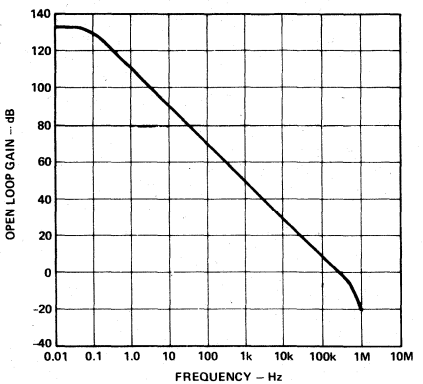
AD OP-07 Open Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

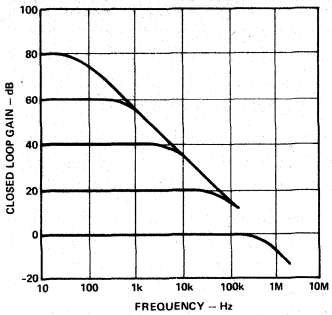


Open Loop Gain vs. Temperature

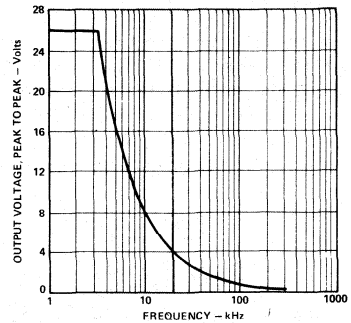


Open Loop Frequency Response

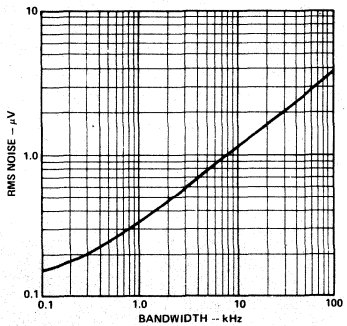
Typical Performance Curves



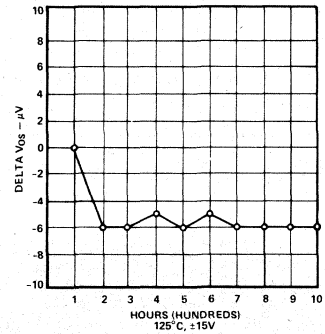
Closed Loop Response for Various Gain Configurations



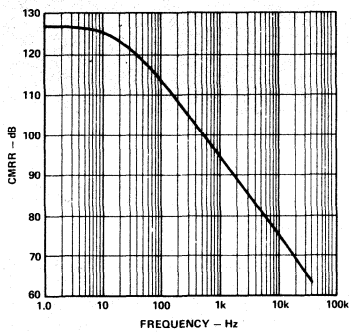
Maximum Undistorted Output vs. Frequency



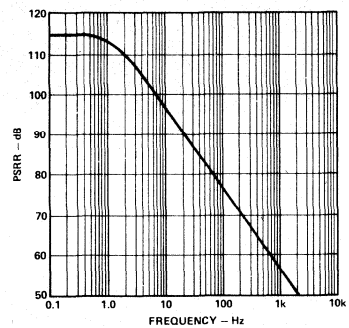
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



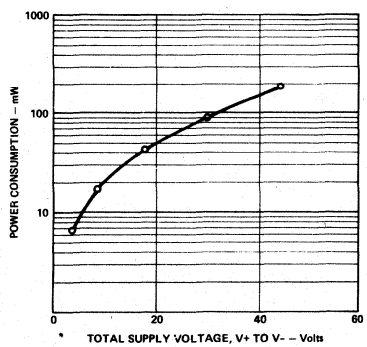
Offset Voltage vs. Time



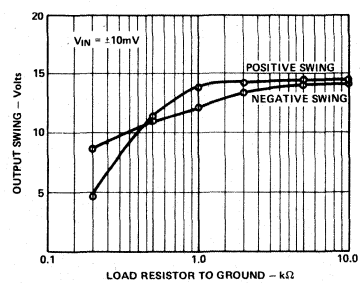
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance

ANALOG DEVICES

Ultra-Low Noise Precision Op Amp

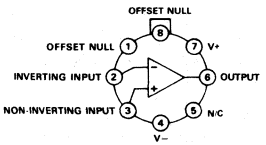
AD OP-27

4

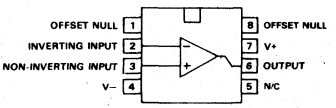
FEATURES

Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
Ultra-Low Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
High Slew Rate: 2.8V/μs
High Gain Bandwidth Product: 8MHz
Low Offset Voltage: 10μV
High CMRR: 126dB over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, 725, 714 and 741 Sockets

AD OP-27 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW



8-PIN MINI DIP
TOP VIEW

PRODUCT DESCRIPTION

The AD OP-27 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. State-of-the-art performance for high accuracy amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-27. As a device directly compatible with other low noise op amps, the AD OP-27 features industry standard dc performance; input offset voltages of 10μV and input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-27 is characterized by an e_n p-p of 80nV (0.1Hz to 10Hz), an e_n of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. AC specifications including a 2.8V/μs slew rate and an 8MHz gain bandwidth product are possible without sacrificing dc accuracy. Long term stability is assured by an input offset voltage drift specification of 0.2μV/month.

Source resistance related errors with the AD OP-27 are minimized by a low input bias current at ambient of ±10nA and an input offset current of 7nA. An input bias current cancellation circuit limits bias and offset currents over the extented temperature range to ±20nA and 15nA, respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-27 is available in six performance grades. The AD OP-27E, AD OP-27F and AD OP-27G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-27A, AD OP-27B and AD OP-27C are specified for −55°C to +125°C operation. All devices are available in TO-99 hermetically sealed metal cans, while the E, F and G grades are also packaged in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. Precision amplification of very low level, low frequency voltage inputs is enhanced by ultra-low input voltage noise.
2. The AD OP-27 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

MODEL		AD OP-27G			AD OP-27F			AD OP-27E		
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		–	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		**750**	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		**±11.7**	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	5.0	8.0		5.0	8.0		5.0	8.0	
Slew Rate	SR	1.7	2.8		1.7	2.8		1.7	2.8	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**50**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	**±60**
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	**50**
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		**±10.5**	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		**110**	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	5.6		3.0	4.6		3.0	4.6
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	**15**
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
T_{MIN}, T_{MAX}		−25		+85	−25		+85	−25		+85

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_p = 8k\Omega$ to $20k\Omega$.

[3]Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

Specifications subject to change without notice.

AD OP-27C			AD OP-27B			AD OP-27A			CONDITIONS	UNITS
MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
–	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
5.0	8.0		5.0	8.0		5.0	8.0			MHz
1.7	2.8		1.7	2.8		1.7	2.8		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	**1.8**		0.3	**1.3**		0.2	**0.6**	T_a = min to max (Note 2)	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 3)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	$nV/\sqrt{Hz}$
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	$nV/\sqrt{Hz}$
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	$nV/\sqrt{Hz}$
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	$pA/\sqrt{Hz}$
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	$pA/\sqrt{Hz}$
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	$pA/\sqrt{Hz}$
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		**±10.3**	±11.5		**±10.3**	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	5.6		3.0	4.6		3.0	4.6	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage (Note 3)	±0.7V
Differential Input Current (Note 3)	±25mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AD OP-27A, AD OP-27B, AD OP-27C	−55°C to +125°C
AD OP-27E, AD OP-27F, AD OP-27G	−25°C to +85°C
Lead Temperature Range (Soldering 60sec)	300°C

NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
MINI-DIP (N)	36°C	5.6mW/°C

Note 2: For supply voltages less than ± 18V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: The AD OP-27's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

AD OP-27 ORDERING GUIDE

Model	Package Option[1]	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-27-GH	TO-99	−25 to +85	100	1.8
AD OP-27-GN	MINI-DIP (N8A)	−25 to +85	100	1.8
AD OP-27-FH	TO-99	−25 to +85	60	1.3
AD OP-27-FN	MINI-DIP (N8A)	−25 to +85	60	1.3
AD OP-27-EH	TO-99	−25 to +85	25	0.6
AD OP-27-EN	MINI-DIP (N8A)	−25 to +85	25	0.6
AD OP-27-CH	TO-99	−55 to +125	100	1.8
AD OP-27-BH	TO-99	−55 to +125	60	1.3
AD OP-27-AH	TO-99	−55 to +125	25	0.6

NOTE

[1]See Section 19 for package outline information.

APPLICATION NOTES FOR THE AD OP-27

The AD OP-27 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for optimum AD OP-27 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

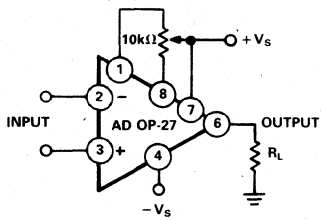


Figure 1. Optional Offset Nulling Circuit

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-27. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature—a temperature close to the device's package.

Output stability with the AD OP-27 is possible with capacitive loads of up to 2000pF and ±10V output swings. Larger capacitances should be decoupled with a 50Ω resistor.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-27 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

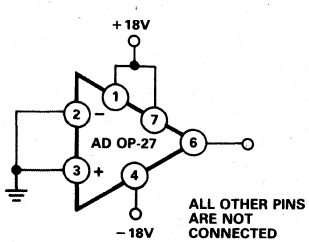


Figure 2. Burn-In Circuit

SLEW RATE DISCUSSION

In unity gain buffer applications with feedback resistances of less than 100Ω where the input is driven with a fast, large (greater than 1V) pulse, the output waveform will appear as in Figure 3.

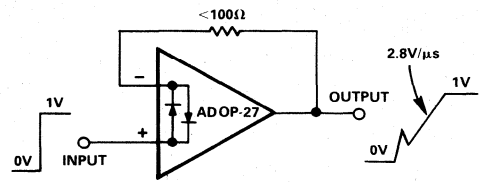


Figure 3. Unity Gain Buffer/Pulsed Operation

During the initial portion of the output slew the input protection back-to-back diodes effectively short the output to the input. A current limited only by the output short circuit protection will be drawn from the source. After the input diodes saturate, the amplifier will slew at its nominal 2.8V/μs. With feedback resistances of more than 500Ω the output is capable of handling the current requirements without limiting (less than 20mA at 10V) and the amplifier will stay in the linear region.

As with all operational amplifiers a feedback resistance of greater than 2kΩ will create a pole with the input capacitance (8pF). Additional phase shift will be introduced and the phase margin will be reduced. A small capacitor (20 to 50pF) in parallel with the feedback resistor will alleviate this problem.

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-27 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

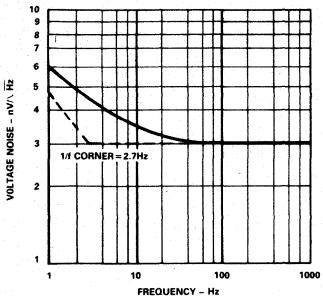
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

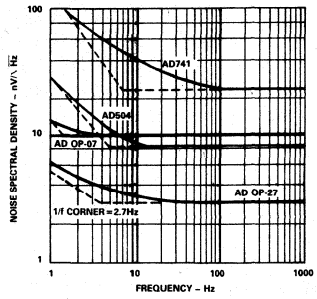
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the 1/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee 1/f and white noise performance over the rated frequency spectrum.

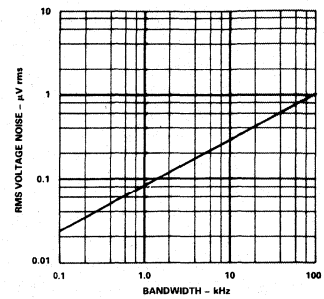
Typical Performance Curves (@ $T_A = +25°C$, $V_S = \pm 15V$)



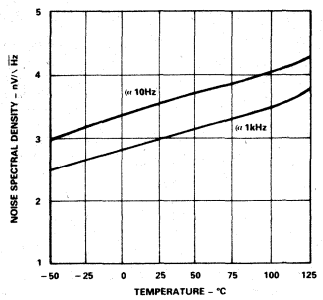
Input Voltage Noise Spectral Density



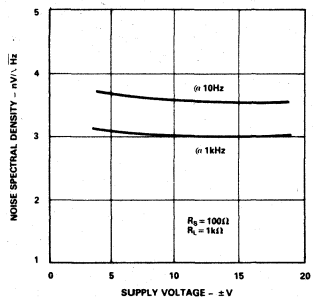
Comparison of Op Amp Input Voltage Noise Spectrums



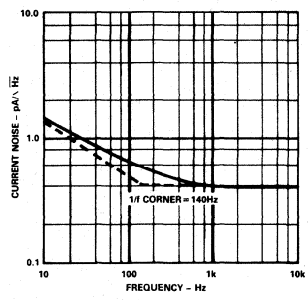
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



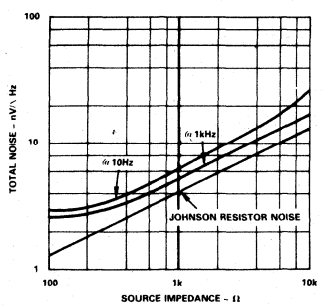
Input Voltage Noise vs. Temperature



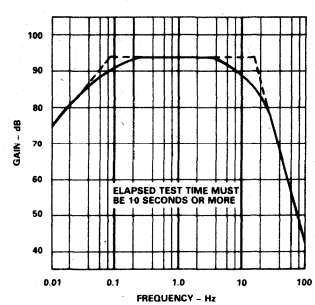
Input Voltage Noise vs. Supply Voltage



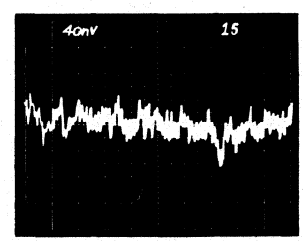
Input Current Noise Spectral Density



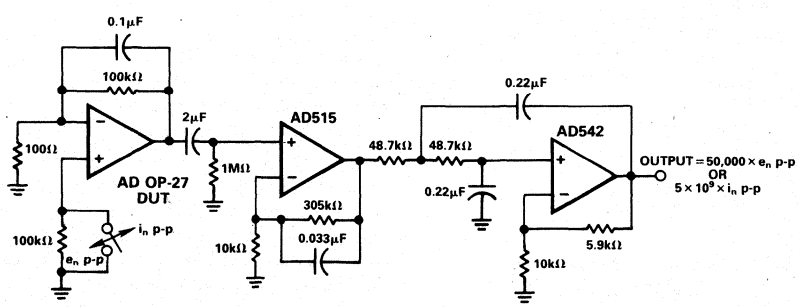
Total Noise vs. Source Impedance



0.1Hz to 10Hz Noise Test Frequency Response

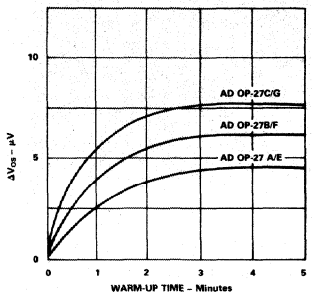


0.1Hz to 10Hz p-p Voltage Noise

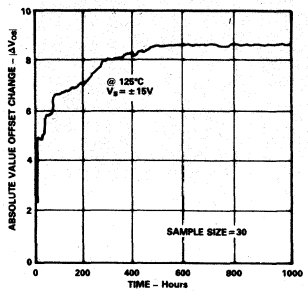


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

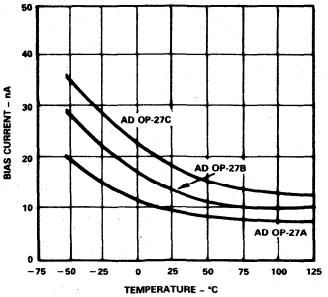
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



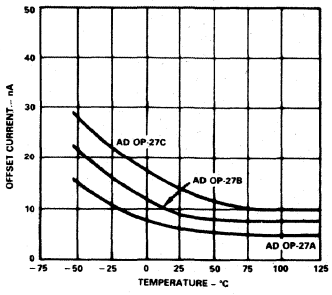
Input Offset Voltage Turn-On Drift vs. Time



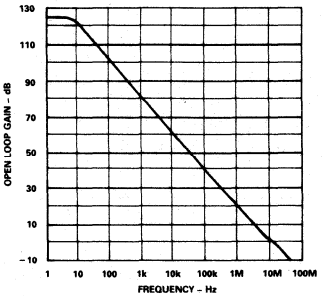
Long Term Offset Stability @ Temperature



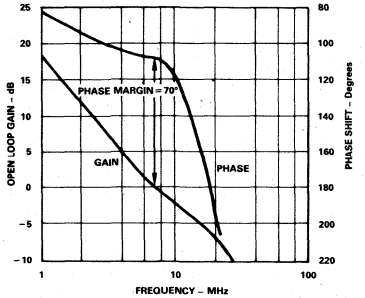
Input Bias Current vs. Temperature



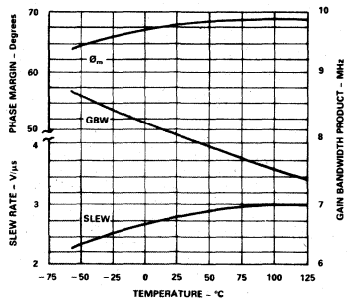
Input Offset Current vs. Temperature



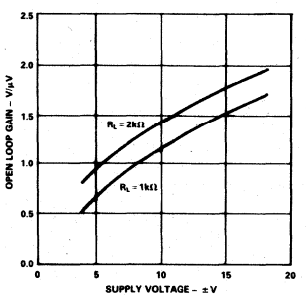
Open Loop Frequency Response



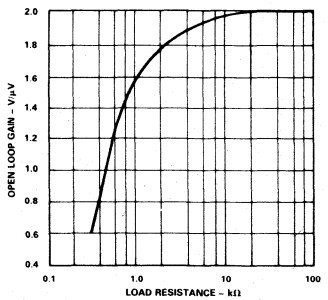
Open Loop Gain and Phase Shift vs. Frequency



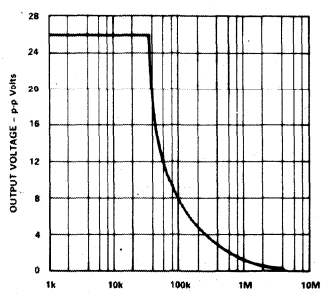
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



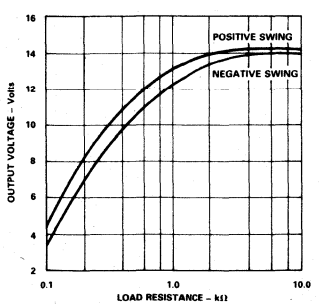
Open Loop Gain vs. Supply Voltage



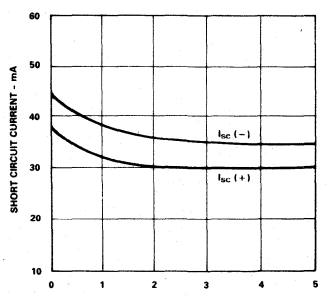
Open Loop Gain vs. Resistive Load



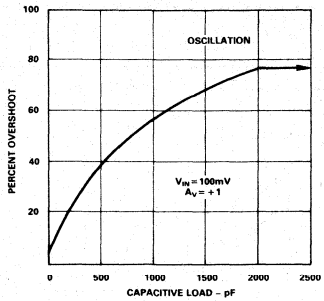
Undistorted Output Swing vs. Frequency



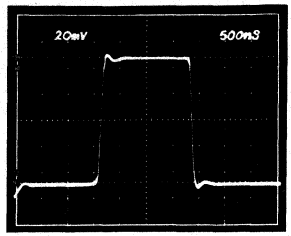
Output Swing vs. Resistive Load



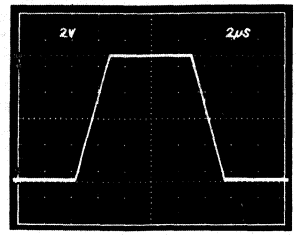
Output Short Circuit Current vs. Time



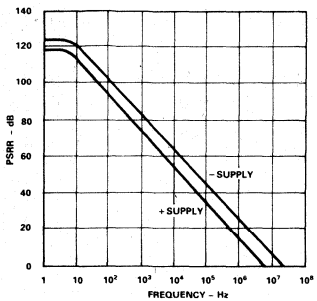
Small Signal Overshoot vs. Capacitive Load



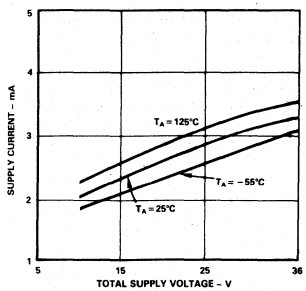
Unity Gain Follower Pulse Response (Small Signal)



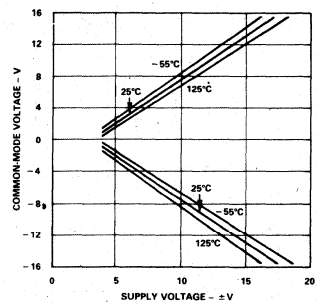
Unity Gain Follower Pulse Response (Large Signal)



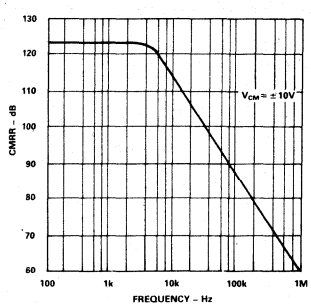
Power Supply Rejection Ratio vs. Frequency



Supply Current vs. Supply Voltage



Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency

ANALOG DEVICES

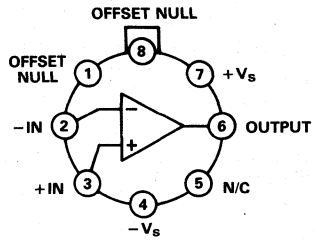
Ultra-Low Noise, High Speed Precision Op Amp

AD OP-37

FEATURES

Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
High Speed: 17V/μs
High Gain Bandwidth Product: 63MHz
Ultra-Low Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, LH0044, 5130, 3510, 725, 714 and 741 Sockets in Gains > 5

AD OP-37 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD OP-37 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. High speed accurate amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-37 in applications requiring gains greater than five. This instrumenation grade op amp features industry standard dc performance; input offset voltages of 10μV and input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-37 is characterized by an e_n p-p of 80nV (0.1Hz to 10Hz), an e_n of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. High speed performance is assured by a 17V/μs slew rate and a 63MHz gain bandwidth product. Long term stability is guaranteed by an input offset voltage drift specification of 0.2μV/month.

Source resistance related input errors with the AD OP-37 are minimized by a low input bias current of ±10nA and an input offset current of 7nA. An input bias current cancellation circuit restricts bias and offset currents over the extended temperature range to ±20nA and 15nA, respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-37 is available in six performance grades. The AD OP-37E, AD OP-37F and AD OP-37G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-37A, AD OP-37B and AD OP-37C are specified for −55°C to +125°C operation. All devices are available in TO-99 hermetically sealed metal cans, while the industrial grades are also packaged in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. High speed accurate amplification (gains > 5) of very low level low frequency voltage inputs is enhanced by a high gain bandwidth product and ultra-low input voltage noise.
2. The AD OP-37 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common-mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

MODEL		AD OP-37G			AD OP-37F			AD OP-37E		
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		**750**	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		**±11.7**	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	45	63		45	63		45	63	
		–	40		–	40		–	40	
Slew Rate	SR	11	17		11	17		11	17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**50**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	**±60**
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	**50**
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		**±10.5**	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		**110**	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	5.6		3.0	4.6		3.0	4.6
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	**15**
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
T_{MIN}, T_{MAX}		−25		+85	−25		+85	−25		+85
PACKAGE[4]										
TO-99			AD OP-37GH			AD OP-37FH			AD OP-37EH	
MINI-DIP (N8A)			AD OP-37GN			AD OP-37FN			AD OP-37EN	

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_p = 8k\Omega$ to $20k\Omega$.

[3]Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

[4]See Section 19 for package outline information.

Specifications subject to change without notice.

AD OP-37C			AD OP-37B			AD OP-37A			CONDITIONS	UNITS
MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
–	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
45	63		45	63		45	63		$f_o = 10kHz$	MHz
–	63		–	40		–	40		$f_o = 1MHz$	MHz
11	17		11	17		11	17		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	**1.8**		0.3	**1.3**		0.2	**0.6**	T_a = min to max (Note 2)	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 3)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	$nV/\sqrt{Hz}$
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	$nV/\sqrt{Hz}$
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	$nV/\sqrt{Hz}$
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	$pA/\sqrt{Hz}$
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	$pA/\sqrt{Hz}$
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	$pA/\sqrt{Hz}$
±11.	±12.3		**±11.**	±12.3		**±11.**	±1			
±10.2	±11.5		**±10.3**	±11.5		**±10.3**	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	5.6		3.0	4.6		3.0	4.6	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C
AD OP-37CH			AD OP-37BH			AD OP-37AH				
–			–			–				

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 3) . . . . . ±0.7V
Differential Input Current (Note 3) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-37A, AD OP-37B, AD OP-37C . −55°C to +125°C
AD OP-37E, AD OP-37F, AD OP-37G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

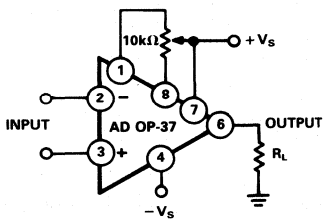
NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

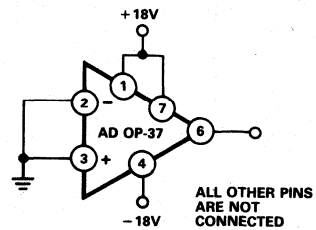
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
MINI-DIP (N)	36°C	5.6mW/°C

Note 2: For supply voltages less than ± 18V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: The AD OP-37's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ± 0.7V, the input current should be limited to 25mA.



Optional Offset Nulling Circuit



Burn-In Circuit

AD OP-37 ORDERING GUIDE

Model	Package	Temperature Range (°C)	Max Initial Offset (µV)	Max Offset Drift (µV/°C)
AD OP-37-GH	TO-99	−25 to +85	100	1.8
AD OP-37-GN	MINI-DIP	−25 to +85	100	1.8
AD OP-37-FH	TO-99	−25 to +85	60	1.3
AD OP-37-FN	MINI-DIP	−25 to +85	60	1.3
AD OP-37-EH	TO-99	−25 to +85	25	0.6
AD OP-37-EN	MINI-DIP	−25 to +85	25	0.6
AD OP-37-CH	TO-99	−55 to +125	100	1.8
AD OP-37-BH	TO-99	−55 to +125	60	1.3
AD OP-37-AH	TO-99	−55 to +125	25	0.6

ANALOG DEVICES

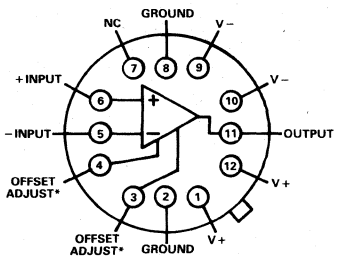
Fast Settling Video Operational Amplifier

HOS-050, 050A, 050C

FEATURES
- 80ns Settling to 0.1%; 200ns to 0.01%
- 100MHz Gain Bandwidth Product
- 55MHz 3dB Bandwidth
- 100mA Output @ ±10V

APPLICATIONS
- D/A Current Converter
- Video Pulse Amplifier
- CRT Deflection Amplifier
- Wideband Current Booster

HOS-050/A/C PIN DESIGNATIONS



*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.

TO-8
BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-050, HOS-050A, and HOS-050C op amps are very high speed wideband operational amplifiers designed to complement the Analog Devices' lines of high speed data acquisition products. They feature a 100MHz gain bandwidth product; slew rate of 300V/μs; and settling time of 80ns to ±0.1%.

The HOS-050A, HOS-050, and HOS-050C have typical input offset voltages of 10mV, 25mV, and 45mV, respectively.

All models have a rated output of ±100mA minimum, and an exceptional noise spec of only 7μV rms, dc to 2MHz; they are ideally suited for a broad range of video applications.

FAST-SETTLING OP AMPS

At one time, operational amplifiers could be specified according to slew rates, bandwidth, and drive capability; and these parameters would be sufficient. Settling time was not considered until the use of high speed video D/A converters became widespread.

The conversion speed of the D/A can be limited by the settling time of the output amplifier, so it has become essential to select an op amp whose settling time is compatible with the D/A converter.

The increased emphasis on settling time has, in some cases, created a preoccupation with slew rates in the minds of some designers. But slew rate is only one component in establishing settling time.

The amount of overshoot, and the ringing which are present at the end of a step function change also have an effect. These parameters, in turn, are influenced by the bandwidth (or lack of it) when operating the op amp with closed loop gains greater than one.

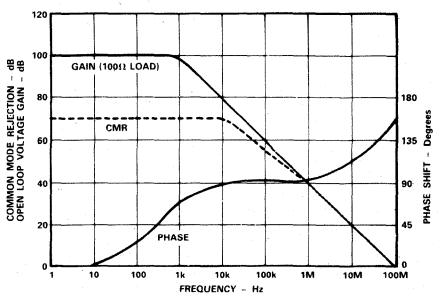


Figure 1. HOS-050 Frequency Response

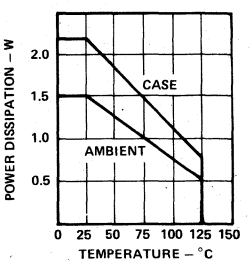


Figure 2. Power Dissipation vs. Temperature

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise specified)

Model	HOS-050	HOS-050A	HOS-050C
ABSOLUTE MAXIMUM RATINGS			
Supply Voltages (V_S)	±18V	*	*
Power Dissipation	See Figure 2	*	*
Input Voltage	$\pm V_S$	*	*
Differential Input Voltage	$\pm V_S$	*	*
Operating Temperature Range (case)	−55°C to +125°C	*	−25°C to +85°C
Junction Temperature	175°C	*	*
Storage Temperature Range	−65°C to +150°C	*	*
Lead Temperature (soldering, 10 sec.)	300°C	*	*

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Open Loop Gain	R_L = 100Ω		100			*			*		dB
Rated Output											
Current											
(not short circuit protected)	R_L = >100Ω		±100			*			*		mA
Voltage	R_L = >200Ω	±10			*			*			V
Input Offset Voltage	Adjustable to Zero										
Initial	@ +25°C		25	35		10	15		45	65	mV
vs. Temperature			50	150		20	35		75	200	µV/°C
vs. Power Supply Voltage			0.5			*			*		mV/V
Input Bias Current											
Initial	@ +25°C		1	2		*	*		*	*	nA
vs. Temperature			Doubles			*			*		/10°C
Input Offset Current											
Initial	@ +25°C		±100			*			*		pA
Input Impedance											
Differential	}In parallel with 5pF		10^{10}			*			*		Ω
Common Mode			10^{10}			*			*		Ω
Input Voltage Range											
Common Mode		±10		±18	*		*	*		*	V
Differential				±18			*			*	V
Common Mode Rejection			70			*			*		dB
Input Noise	R_{FF} = 100Ω; R_{FB} = 1kΩ										
dc to 100kHz			5			*			*		µV rms
dc to 2MHz			7			*			*		µV rms

AC ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Slew Rate	A = −1; R_{FF} = R_{FB} = 500Ω; Load = 100Ω		300			*			*		V/µs
Noninverting Slew Rate	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 100Ω		320			*			*		V/µs
Overload Recovery	50% Overdrive		400			*			*		ns
Gain Bandwidth Product	R_{FF} = R_{FB} = 500Ω		100			*			*		MHz
Small Signal Bandwidth, −3dB	A = −1; R_{FF} = R_{FB} = 500Ω		45			*			*		MHz
	A = −1; R_{FF} = R_{FB} = 1000Ω		35			*			*		MHz
	A = −2; R_{FF} = R_{FB} = 500Ω; R_{FB} = 1000Ω		35			*			*		MHz
	A = −4; R_{FF} = R_{FB} = 250Ω; R_{FB} = 1000Ω		30			*			*		MHz
Output Impedance				<1			*			*	Ω
Noninverting Bandwidth, −3dB	A = 2; R_{FF} = R_{FB} = 1000Ω; 100Ω load; 10pF capacitance										
	5-volt p-p output		25			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		55			*			*		MHz
	A = 3; R_{FF} = 500Ω; R_{FB} = 1000Ω; 100Ω, 1000 Ω; or 2000Ω load; 10pF capacitance										
	10-volt p-p output		17			*			*		MHz
	5-volt p-p output		25			*			*		MHz

AC ELECTRICAL CHARACTERISTICS[1] (Continued)		HOS-050			HOS-050A			HOS-050C			
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Noninverting Bandwidth, −3dB (continued)	A = 5; R_{FF} = 500Ω; R_{FB} = 2000Ω; 100Ω, 1000Ω, or 2000Ωload/10pF capacitance										
	5-volt p-p output		15			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		40			*			*		MHz
	1-volt p-p output		40			*			*		MHz
Full Power Bandwidth (−3dB)	Output = ±5V; A = −1; R_L = 100Ω		20			*			*		MHz
Settling Time to 0.1%	A = −1; R_{FF} = R_{FB} = 500Ω										
Inverting	V_{OUT} = ±5V		100			*			*		ns
(See Figure 5)	V_{OUT} = ±2.5V		80			*			*		ns
Noninverting	A = 2; R_{FF} = R_{FB} = 500Ω Max Load capacitance = 75pF										
	V_{OUT} = ±5V		200			*			*		ns
	V_{OUT} = ±2.5V		135			*			*		ns
Harmonic Distortion (See Figure 9)	A = −1; Load = 1000Ω Signal = 4MHz; 2V output		−63			*			*		dB
Noninverting Harmonic Distortion (See Figure 10)	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 1000Ω; Signal = 4MHz; 2V output		−59			*			*		dB
Power Supply											
Voltage	Rated performance		±15			*			*		V dc
Voltage	Operating range	±12		±18	*		*	*		*	V dc
Current	Quiescent		±20	±25		*	*		*	*	mA
Power Consumption	Quiescent		0.6			*			*		W
Power Dissipation				1.25			*			*	W
Temperature Range											
Operating (Case)	(See Figure 2 for	−55		+125	*		*	−25		+85	°C
Storage	Derating Information)	−65		+150	*		*	*		*	°C
Meantime Between Failures (MTBF)	MIL-HNBK 217; Ground; Fixed; Case = 70°C				6.27 × 10^6						Hours

Notes:
[1]Specification for Inverting Mode unless otherwise noted.
*Specification same as HOS-050

Individual socket assemblies (one per pin) are available from AMP as part number 6-330808-0.
Specifications subject to change without notice.

PIN DESIGNATIONS[1]

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	−INPUT
6	+INPUT
7	NC
8	GROUND
9	−V
10	−V
11	OUTPUT
12	+V

[1]SEE SECTION 19 (H12A) FOR PACKAGE OUTLINE INFORMATION.
*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.

The HOS-050 Series stands up under close scrutiny of these characteristics because of its 100MHz gain bandwidth product. The use of these amplifiers in a wide variety of applications has confirmed their suitability for video circuits.

VOLTAGE AMPLIFIERS/CURRENT BOOSTERS

Video op amps such as the HOS-050 are generally characterized by high gain bandwidth products, fast settling times, and high output drive.

One of the most common uses of video op amps is for D/A converter output voltage amplification or current boosting. Figure 3 is one example of this type of application. In this circuit, the internal resistance of the D/A is the feed forward resistor for the op amp.

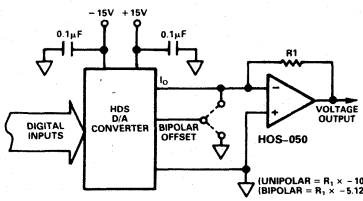


Figure 3. Inverting Unipolar or Bipolar Voltage Output

The HDS Series D/A converters are fast-settling, current output D/As available in 8-, 10-, and 12-bit resolutions. Both TTL and ECL versions are available, and settling times range from 10ns for 8-bit units through 40ns for 12-bit units.

The circuit which is shown will provide a negative unipolar output with binary coding on the input, and bipolar offset grounded. It will provide a bipolar output with complementary offset binary coding on the input, and bipolar offset connected to I_O.

An approximation of the total settling time for the D/A op amp combination is calculated by:

$$T_S = \sqrt{T_D^2 + T_O^2}$$

where T_D is D/A settling time and T_O is HOS-050 settling time.

This approximation is valid because both the D/A and the HOS-050 exhibit 6dB/octave roll-off charateristics (single pole response); and the combination of low D/A output capacitance and op amp input capacitance does not materially affect the formula.

The user of the HOS-050 should remember the current flowing in the feedback resistor (R1) must be subtracted from the output available from the HOS-050.

There is a tendency, because of this fact, to use a high value of feedback resistor to assure maximum current drive being available for driving low impedances; but this approach may create undesirable side effects.

Calculating the minimum load that can be driven under two conditions of feedback resistor values will serve to illustrate the difference.

Assume the feedback resistor value is 500Ω. If output voltage of the HOS-050 is 10 volts, and output current is 100mA, minimum load would be:

$$\frac{E_O \text{ max}}{I_O \text{ max} - I_{RFB}} = \frac{10V}{100mA - 20mA} = \frac{10V}{80mA} = 125\Omega \text{ minimum load}$$

where: E_O max = peak voltage needed
I_O max = maximum continuous current HOS-050 can produce
I_{RFB} = current in feedback resistor at peak voltage

Assume the feedback resistor value is 5,000Ω. Minimum load would be:

$$\frac{E_O \text{ max}}{I_O \text{ max} - I_{RFB}} = \frac{10V}{100mA - 2mA} = \frac{10V}{98mA} = 102\Omega \text{ minimum load}$$

Designs which strive for driving a minimum load (by increasing the feedback resistor) can create settling problems because of a fundamental characteristic of op amp circuits . . . the higher the feedback resistance, the slower the system response.

This phenomenon is the result of increased impedance for driving stray capacitances in the circuit employing the op amp, and fixed capacitances in the summing node.

Impedances need to be kept as low as possible consistent with low distortion; and stray capacitances need to be eliminated to the maximum possible extent. A large ground plane structure is recommended to help assure low ground impedances. In addition, 0.1μF ceramic capacitors and 3-10μF tantalum capacitors connected as close as possible to power supply inputs will decrease the potential for parasitic oscillations and other noise signals.

Another argument for limiting the size of the feedback resistor is because of its effect on bandwidth. Bandwidth of the HOS-050 op amp and the value of the feedback resistor are inversely related.

At any given gain of the op amp, the gain setting with the widest bandwidth will be the one which employs the lower value of feedback. As an example, a gain of 1 can be achieved with $R_{FF} = R_{FB} = 500\Omega$; or $R_{FF} = R_{FB} = 1{,}000\Omega$. Small-signal bandwidth for the first combination is typically 45MHz; bandwidth for the second is typically 35MHz.

OFFSET AND GAIN ADJUSTMENT

Figure 4 shows a method of using the HOS-050 op amp which allows adjusting the offset and gain of the output voltage.

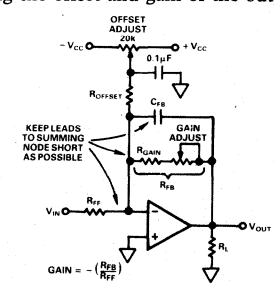


Figure 4. HOS-050 Offset and Gain Adjust

As shown, the gain of the circuit is established by the equation:

$$G = -\left(\frac{R_{FB}}{R_{FF}}\right)$$

where R_{FB} is the total of R_{GAIN} and Gain Adjust.

Once the user has established the desired gain for the illustrated circuit, the value of R_{FB} can be used to determine the correct value of R_{OFFSET} with the equation:

$$R_{OFFSET} = -\left(\frac{V_{CC} \times R_{FB}}{\Delta E_O}\right)$$

where ΔE_O is the desired amount of offset on the output.

Assume $\pm V_{CC} = \pm 15V$; $R_{GAIN} = 900\Omega$; Gain Adjust = 100Ω; the desired change on the output = ± 1 volt.

Under these conditions, R_{OFFSET} will be $15k\Omega$:

$$R_{OFFSET} = -\left(\frac{15V \times [900 + 100]}{1V}\right)$$

$$R_{OFFSET} = -\left(\frac{15kV}{1V}\right)$$

$$R_{OFFSET} = 15{,}000\Omega$$

Figure 4 shows bipolar output operation. If unipolar output is desired, the appropriate V_{CC} should be removed from the Offset Adjust potentiometer.

The 0.1μF capacitor attached to the wiper arm of the Offset Adjust control isolates the control and helps prevent adjustment noise from appearing on the output of the HOS-050.

C_{FB} can be any value between 0 and 20pF, depending on the value of R_{GAIN}; and should be selected to optimize settling time for the particular circuit layout in which the HOS-050 is being used.

The Gain Adjust control should be a low value, low inductance cermet trimming potentiometer.

Note: R_{FF}, R_{GAIN}, C_{FB} and R_{OFFSET} must be located as close to the summing node of the HOS-050 as physically possible. This helps prevent additional capacitance in the summing node and corresponding bad effects on frequency response and settling times.

Variable controls (such as Offset Adjust and Gain Adjust) should never be tied to the summing node of the op amp. Their correct electrical locations are those shown in Figure 4.

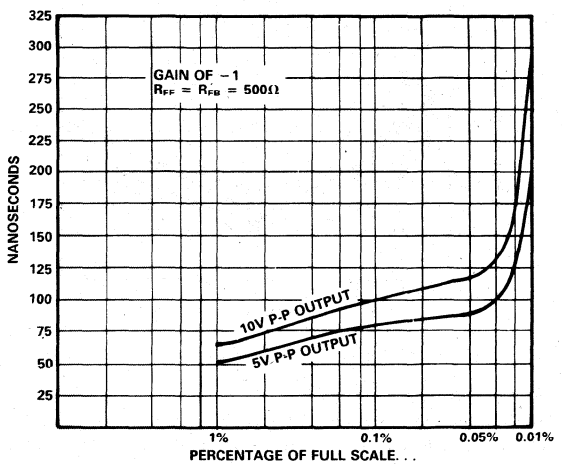


Figure 5. Settling Time – Inverting Mode

SETTLING TIME MEASUREMENT

Although there are some exceptions, most members of industry are in agreement on the description which says settling time is:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

The well-informed user needs to be alert to the consequences of settling time specs which do not meet that description.

This definition encompasses the major components which comprise settling time. They include (1) propogation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for his application.

Figure 6 is the test circuit for measuring settling time to 0.1%. This method creates a "false" summing junction and the error band is observed at that point.

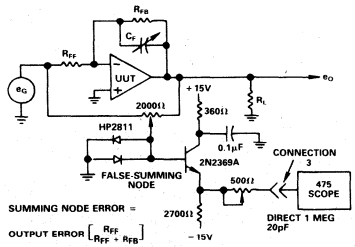


Figure 6. Settling Time Test Circuit for 0.1% Settling

If one were to attempt the measurement at the "true" summing junction of the op amp, the results would be misleading. All scope probes will add capacitance to the input and will change the response of the system. Making the measurement at the output of the amplifier is also impractical, since scope nonlinearities and reading inaccuracies caused by overdriving the scope preclude accurate measurements to the tolerances which are required.

The false summing junction method causes the amplifier to subtract the output from the input; only one-half the actual error appears at the false junction, and it can be measured to the required accuracies.

The false junction is clamped with diodes to limit the voltage excursion appearing at that point. This is necessary because the amplifier will be overdriven and one-half its input voltage will appear at the junction. Without the clamps, the scope used for making the measurement would be overdriven and its recovery time would mask the settling time of the amplifier.

The test circuit for measuring settling time to 0.01%, Figure 7, is simply an extension of the same basic technique. Measuring to the closer tolerance requires additional gain in the circuit driving the oscilloscope.

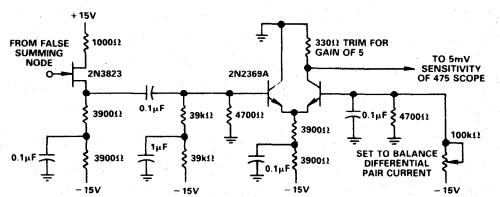


Figure 7. Settling Time Test Circuit for 0.01% Settling

IMPEDANCE MATCHING

The characteristics of the HOS-050 operational amplifier make it an ideal choice for matching the impedances of video circuits to the impedances of transmission lines.

In this application, source and load terminating resistors will cause the output voltage to be halved at the end of the cable

being driven by the op amp. This makes it necessary to set the gain of the circuit to provide twice the desired voltage.

Three different values of resistors and cables are "phantomed" into the figure as examples of possible characteristic impedances which might be used. Figure 8 is *not* meant to imply the HOS-050 can drive three cables simultaneously.

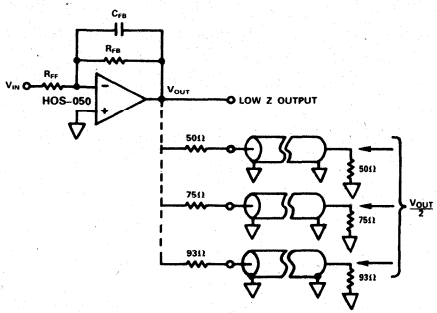


Figure 8. HOS-050 Impedance Matching

NONINVERTING OPERATION

The vast majority of video operational amplifiers display marked differences in settling times and bandwidths when operated in a noninverting mode instead of the inverting mode. There are a number of valid reasons for this characteristic.

Most high-speed op amps use feed-forward compensation for optimizing performance in the inverting mode. This is necessary to obtain wide gain-bandwidth products while maintaining dc performance in these types of devices. In effect, the op amp has a wideband ac channel which is not perfectly matched to the dc channel.

Feed-forward techniques enhance the performance of the op amp in the inverting mode by incresing the slew rate and small-signal bandwidth. These techniques, however, also decrease the amplifier's tolerance to stray capacitances, so must be employed judiciously.

The overall input capacitance of the op amp is kept as low as possible in the design; and any mismatch in the capacitance of the two channels appears as an error in the output. Because of the inherently low total input capacitance of the op amp, even a small capacitive mismatch between channels shows up as a large effective error signal.

Decreasing the channel mismatch can be achieved only by complicating the design of the op amp with additional components, and rigorous selection of those components in the manufacturing process.

As a consequence, the mismatch is reduced to the smallest practical value consistent with the economics of producing and using the op amp. But it remains a mismatch, and manifests itself as a difference in performance in the inverting versus noninverting modes.

There are video op amps available at low cost which use a 741-type amplifier for high dc open loop gain in the noninverting channel. The user of these kinds of designs may sometimes gain an economic advantage, but at a high cost in performance. Bandwidths for noninverting applications are often measured in kHz, not MHz, for this approach.

A video op amp is acting as a voltage mode device at both inputs when operating in the noninverting mode. This contrasts with the inverting mode, where it is operating as a current mode device.

The Analog Devices HOS-050 has different performance characteristics when operating as a noninverting amplifier, but the care used in the design makes the differences less pronounced than they are in many competing units.

The HOS-050 can be considered a true differential video op amp. It requires little or no external compensation because its rolloff characteristics approach a 6dB/octave slope. This helps the user determine summing errors and loop response; and helps assure the stability of the system.

The performance parameters for both inverting and noninverting operation are shown elsewhere in this data sheet (see SPECIFICATIONS section and figures). A comparison of the characteristics will highlight the similarities in performance, with the exceptions noted above.

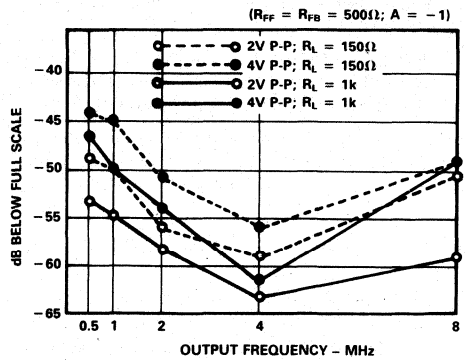


Figure 9. Harmonic Distortion – Inverting

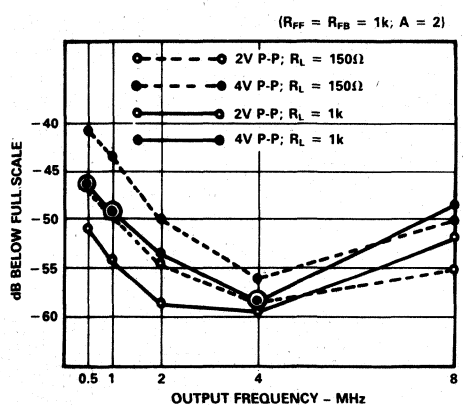


Figure 10. Harmonic Distortion – Noninverting

IN SUMMARY . . . A CAVEAT

Settling time specifications, bandwidth capabilities, harmonic distortion performance, and other parameters for video op amps cannot possibly include all possible situations and applications.

A multitude of seemingly insignificant conditions can have a major impact on the unit and its ability to operate in any given circuit.

The potential user is strongly urged to evaluate the effectiveness of the HOS-050 in the actual circuit in which it will be used. In many instances, the application conditions are different from the conditions used in specifying; there is no substitute for a trial in the proposed circuit to determine if the op amp will provide the desired results.

ANALOG DEVICES

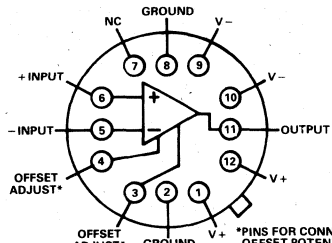
Low Offset, Fast Settling Video Operational Amplifier

HOS-060

FEATURES
- <1mV V_{OS}
- Low Drift
- 80ns Settling to 0.1%; 200ns to 0.01%
- 100mA Output @ ±10V

APPLICATIONS
- D/A Current Converter
- Video Pulse Amplifier
- CRT Deflection Amplifier
- Wideband Current Booster

HOS-060 PIN DESIGNATIONS



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-060 Operational Amplifier is an extension of the proven hybrid technology used in the HOS-050 series of op amps.

The FET input and high-performance characteristics, including wide bandwidth and fast settling, make it useful for a variety of applications in the processing of video signals.

Recent innovations in circuit design have been incorporated into the HOS-060 to make it extremely useful to the designer who needs outstanding performance in current boosting, voltage amplification, impedance matching, or a multiplicity of other high-frequency requirements.

Voltage offset and its temperature coefficient have been dramatically improved in the HOS-060; offset is as low as most high performance monolithic op amps.

The HOS-060 op amp is pin-for-pin compatible with its forerunner HOS-050 and is useable in the same diversity of video requirements. The reader is strongly urged to refer to the six-page data sheet for the HOS-050 op amp to obtain additional insight and details on potential uses for the HOS-060.

The HOS-060 Operational Amplifier package is the industry standard TO-8 metal can and operates over a case temperature range of −55°C to +125°C; the model number for the standard unit is HOS-060SH.

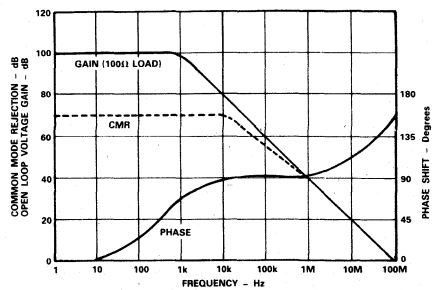


Figure 1. HOS-060 Frequency Response

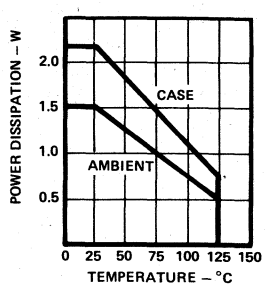


Figure 2. Power Derating

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise specified)

Model	HOS-060SH
ABSOLUTE MAXIMUM RATINGS	
Supply Voltages (V_S)	±18V
Power Dissipation	See Figure 2
Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Operating Temperature Range (case)	−55°C to +125°C
Junction Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec.)	300°C

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Units
Open Loop Gain	R_L = 100Ω		100		dB
Rated Output					
Current					
(not short circuit protected)	R_L = >100Ω		±100		mA
Voltage	R_L = >200Ω	±10			V
Input Offset Voltage	Adjustable to Zero				
Initial	@ +25°C		±0.5	±1	mV
−25°C to +125°C				±2	mV
vs. Case Temperature					
−55°C to +125°C			10		µV/°C
vs. Power Supply Voltage			0.5		mV/V
Input Bias Current					
Initial	@ +25°C		1	2	nA
vs. Temperature			Doubles		/10°C
Input Offset Current					
Initial	@ +25°C		±100		pA
Input Impedance					
Differential	}In parallel with 5pF		10^{10}		Ω
Common Mode			10^{10}		Ω
Input Voltage Range					
Common Mode		±10		±18	V
Differential				±18	V
Common Mode Rejection			70		dB
Input Noise	R_{FF} = 100Ω; R_{FB} = 1kΩ				
dc to 100kHz			5		µV rms
dc to 2MHz			7		µV rms

AC ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions	Min	Typ	Max	Units
Slew Rate	A = −1; R_{FF} = R_{FB} = 500Ω;				
	Load = 100Ω		300		V/µs
Noninverting Slew Rate	A = 2; R_{FF} = R_{FB} = 1000Ω;				
	Load = 100Ω		320		V/µs
Overload Recovery	50% Overdrive		400		ns
Gain Bandwidth Product	R_{FF} = R_{FB} = 500Ω		100		MHz
Small Signal Bandwidth, −3dB	A = −1; R_{FF} = R_{FB} = 500Ω		45		MHz
	A = −1; R_{FF} = R_{FB} = 1000Ω		35		MHz
	A = −2; R_{FF} = 500Ω;				
	R_{FB} = 1000Ω		35		MHz
	A = −4; R_{FF} = 250Ω;				
	R_{FB} = 1000Ω		30		MHz
Output Impedance				<1	Ω
Noninverting Bandwidth, −3dB	A = 2; R_{FF} = R_{FB} = 1000Ω;				
	100Ω load; 10pF capacitance				
	5-volt p-p output		25		MHz
	4-volt p-p output		30		MHz
	2-volt p-p output		55		MHz
	A = 3; R_{FF} = 500Ω;				
	R_{FB} = 1000Ω;				
	load = 100Ω, 1000Ω, or 2000Ω;				
	capacitance = 10pF				
	10-volt p-p output		17		MHz
	5-volt p-p output		25		MHz

AC ELECTRICAL CHARACTERISTICS[1] (Continued) **HOS-060SH**

Parameter	Conditions	Min	Typ	Max	Units
Noninverting Bandwidth, −3dB (continued)	A = 5; R_{FF} = 500Ω; R_{FB} = 2000Ω; 100Ω, 1000Ω, or 2000Ωload/10pF capacitance				
	5-volt p-p output		15		MHz
	4-volt p-p output		30		MHz
	2-volt p-p output		40		MHz
	1-volt p-p output		40		MHz
Full Power Bandwidth (−3dB)	Output = ±5V; A = −1; Load = 100Ω		20		MHz
Settling Time to 0.1%	A = −1; R_{FF} = R_{FB} = 500Ω				
Inverting	V_{OUT} = ±5V		100		ns
	V_{OUT} = ±2.5V		80		ns
Noninverting	A = 2; R_{FF} = R_{FB} = 500Ω Max Load capacitance = 75pF				
	V_{OUT} = ±5V		200		ns
	V_{OUT} = ±2.5V		135		ns
Harmonic Distortion (See Figure 5)	A = −1; Load = 1000Ω Signal = 4MHz; 2V output		−63		dB
Noninverting Harmonic Distortion (See Figure 6)	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 1000Ω; Signal = 4MHz; 2V output		−59		dB
Power Supply					
Voltage	Rated performance		±15		V dc
Voltage	Operating range	±12		±18	V dc
Current	Quiescent		±20	±25	mA
Power Consumption	Quiescent		0.6		W
Power Dissipation				1.25	W
Temperature Range					
Operating (Case)	(See Figure 2 for	−55		+125	°C
Storage	Derating Information)	−65		+150	°C

NOTES
[1]Specification for Inverting Mode unless otherwise noted.
*Specifications same as HOS-060SH.

Individual socket assemblies (one per pin) are available from AMP as part number 6-330808-0.
Specifications subject to change without notice.

PIN DESIGNATIONS[1]

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	−INPUT
6	+INPUT
7	NC
8	GROUND
9	−V
10	−V
11	OUTPUT
12	+V

NOTES
[1]SEE SECTION 19 (H12A) FOR PACKAGE OUTLINE INFORMATION.
*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.

VOLTAGE AMPLIFIERS/CURRENT BOOSTERS

Video op amps such as the HOS-060 are characterized by high gain bandwidth products, fast settling times, and high output drive.

One of the most common uses of video op amps is for D/A current to voltage conversion or current boosting. Figure 3 is one example of this type of application. In this circuit, the internal resistance of the D/A is the feed-forward resistor for the op amp.

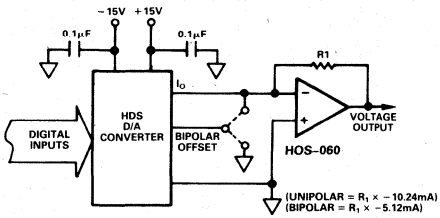


Figure 3. Inverting Unipolar or Bipolar Voltage Output

The circuit which is shown will provide a negative unipolar output with binary coding on the input, and the bipolar offset pin grounded. It will provide a bipolar output with complementary offset binary coding on the input, and bipolar offset connected to I_O.

OFFSET AND GAIN ADJUSTMENT

The low value of offset may preclude the need for adjustment, but Figure 4 shows a method of adjusting both offset and gain.

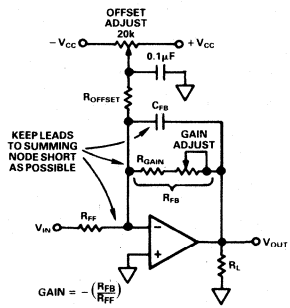


Figure 4. HOS-060 Offset and Gain Adjust

As shown, the gain of the circuit is established by the equation:

$$G = -\left(\frac{R_{FB}}{R_{FF}}\right) \text{ where } R_{FB} = R_{GAIN} + \text{Gain Adjust.}$$

Once the user has established the desired gain for the illustrated circuit, the value of R_{FB} can be used to determine the correct value of R_{OFFSET} with the equation:

$$R_{OFFSET} = -\left(\frac{V_{CC} \times R_{FB}}{\Delta E_O}\right)$$

where ΔE_O is the desired amount of offset on the output.

Note: R_{FF}, R_{GAIN}, C_{FB} and R_{OFFSET} must be located as close to the summing node of the HOS-060 as physically possible. This helps prevent additional capacitance in the summing node and corresponding bad effects on frequency response and settling times.

Variable controls (such as Offset Adjust and Gain Adjust) should never be tied to the summing node of the op amp. Their correct electrical locations are those shown in Figure 4.

NONINVERTING OPERATION

The vast majority of video operational amplifiers display marked differences in settling times and bandwidths when operated in a noninverting mode instead of the inverting mode. There are a number of valid reasons for this characteristic.

Most high-speed op amps use feed-forward compensation for optimizing performance in the inverting mode. This is necessary to obtain wide gain-bandwidth products while maintaining dc performance in these types of devices. In effect, the op amp has a wideband ac channel which is not perfectly matched to the dc channel.

Feed-forward techniques enhance the performance of the op amp in the inverting mode by increasing the slew rate and small-signal bandwidth. These techniques, however, also decrease the amplifier's tolerance to stray capacitances, so must be employed judiciously.

The Analog Devices HOS-060 has different performance characteristics when operating as a noninverting amplifier, but the care used in the design makes the differences less pronounced than they are in the designs of competing units.

The HOS-060 can be considered a true differential video op amp. It requires little or no external compensation because its rolloff characteristics approach a 6dB/octave slope. This helps the user determine summing errors and loop response; and helps assure the stability of the system.

The performance parameters for both inverting and noninverting operation are shown elsewhere in this data sheet (see SPECIFICATIONS section and figures). A comparison of the characteristics will highlight the similarities in performance, with the exceptions noted above.

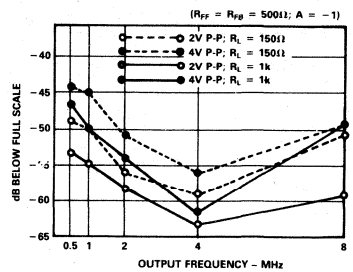


Figure 5. Harmonic Distortion – Inverting

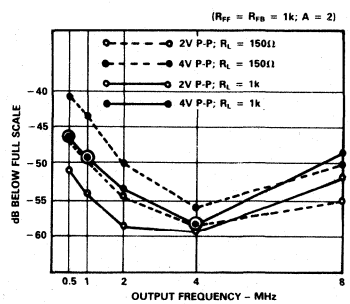


Figure 6. Harmonic Distortion – Noninverting

THE READER IS URGED TO CONSULT THE HOS-050 DATA SHEET FOR ADDITIONAL APPLICATIONS INFORMATION. THE HOS-060 IS PIN-FOR-PIN COMPATIBLE WITH THE HOS-050 SERIES AND CAN BE USED IN SIMILAR WAYS.

ANALOG DEVICES

Wide Bandwidth, High Speed Buffer Amplifiers

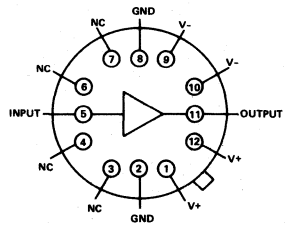
HOS-100AH, 100SH

4

FEATURES
- Wide Bandwidth – dc to 125MHz
- High Slew Rate – 1500V/μs
- Operation Guaranteed -55°C to +125°C (SH)
- High Output Drive – ±10V with 100Ω Load

APPLICATIONS
- Current Boosters
- High Speed A/D Input Buffers
- Nuclear Instrumentation Amplifiers
- Coaxial Cable Drive
- High Speed Line Drivers
- Video Impedance Transformation

HOS-100SH/HOS-100AH PIN DESIGNATIONS



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-100SH and HOS-100AH Bipolar Buffer Amplifiers are high-speed, voltage follower/buffers designed to provide high-current drive at frequencies from dc to over 125MHz, as well as providing ±10mA into 1kΩ loads (±100mA peak) at slew rates of 1500V/μs. Both units also exhibit excellent phase linearity (2°), and low distortion (<0.1%).

For commercial temperature ranges the HOS-100AH is specified for operation over the range of -25°C to +85°C (case). The HOS-100SH is specified for operation over the extended range of -55°C to +125°C (case).

The HOS-100SH and HOS-100AH are intended to fulfill a wide range of buffer applications, such as video impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high-speed line drivers and nuclear instrumentation amplifiers. Additionally, both amplifiers will continuously drive 50Ω coaxial cables or serve as yoke drives in high resolution CRT displays.

They are particularly well suited for current booster applications (Figure 3) within an op-amp loop where input impedance and bias current requirements are less stringent than in FET design.

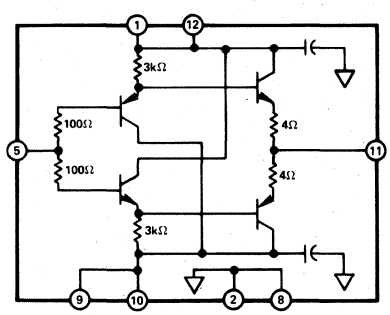


Figure 1. Schematic Diagram HOS-100

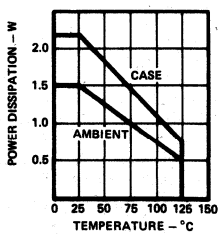


Figure 2. Power Derating

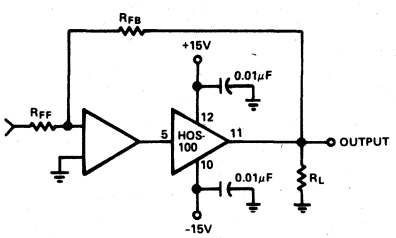


Figure 3. Current Booster

SPECIFICATIONS

PARAMETER	CONDITIONS	HOS-100SH MIN	HOS-100SH TYP	HOS-100SH MAX	HOS-100AH MIN	HOS-100AH TYP	HOS-100AH MAX	UNITS
DC ELECTRICAL CHARACTERISTICS[1,2]								
Input Bias Current	$T_C = 25°C$		5	20		5	25	μA
				25				μA
Input Impedance	V_{IN} = 1V rms, f = 1kHz R_L = 1k, $T_C = 25°C$	100	200		100	200		kΩ
Voltage Gain	V_{IN} = 1V rms, f = 1kHz R_L = 1k, $T_C = 25°C$	0.95	0.97	1.0	0.94	0.96	1.0	V/V
Output Offset Voltage	$R_S = 50Ω$, $T_C = 25°C$		5	10		10	25	mV
				25			35	mV
Output Offset Voltage T_C	$R_S = 50Ω$		25	75		25	75	μV/°C
Output Impedance	V_{IN} = 1V rms, f = 1kHz $R_S = 500Ω$, R_L = 1k		8	12		8	12	Ω
Output Voltage Swing	$R_S = 50Ω$, R_L = 1k	±12	±13		±12	±13		V
	$V_S = ±5V$, R_L = 1k		6			6		V
Supply Current	V_{IN} = 0V, $T_C = 25°C$							
	$V_S = ±15$		13	16		15	20	mA
	$V_S = ±5$		10			10		mA
Power Consumption	V_{IN} = 0V, $V_S = ±15V$ $T_C = 25°C$		390	480		450	600	mW
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	$V_{IN} = ±10V$	1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1V rms	100	125		100	125		MHz
Rise Time	$ΔV_{IN}$ = 0.5V		2	5		2	5	ns
Propagation Delay	$ΔV_{IN}$ = 0.5V		1.5			1.5		ns
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Harmonic Distortion			<0.1			<0.1		%
MTBF			$1.509X10^7$ hours					
PACKAGE TYPE[4]			H12A			H12A		

NOTES

[1] Unless otherwise noted, these specifications apply for +15V applied to Pin 12, and −15V applied to Pin 10.

[2] Unless otherwise noted, specifications apply over a temperature range, $-55°C \leq T_C \leq +125°C$ for the HOS-100SH, and $-25°C \leq T_C \leq +85°C$ for the HOS-100AH. Typical values shown are for $T_C = +25°C$.

[3] These specifications all measured with the following conditions: $T_C = +25°C$, $V_S = ±15V$, $R_S = 50Ω$, R_L = 1k.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ − V−) 40V
Maximum Power Dissipation 1.5W
Input Voltage . . . . . Equal to Supply Voltage
Maximum Continuous Output Current . . . . . ±100mA
Maximum Peak Output Current . . . . . ±250mA
Operating Temperature Range (Case) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Maximum Junction Temperature . . . . . +175°C

ORDERING INFORMATION

Model	Temperature Range
HOS-100AH	−25°C to +85°C
HOS-100SH	−55°C to +125°C

Instrumentation & Isolation Amplifiers

Contents

•New product since publication of *1982–1983 Databook Update.*

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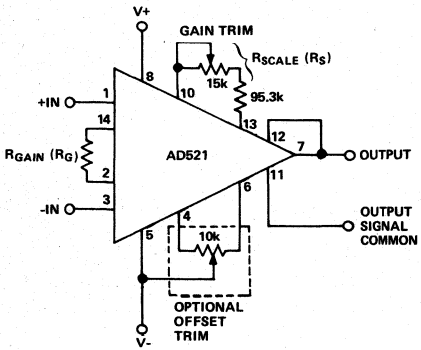
Instrumentation Amplifiers



AD521

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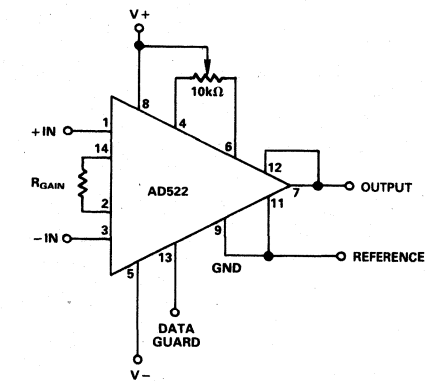
Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Low Drift: 2μV/°C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000



AD522

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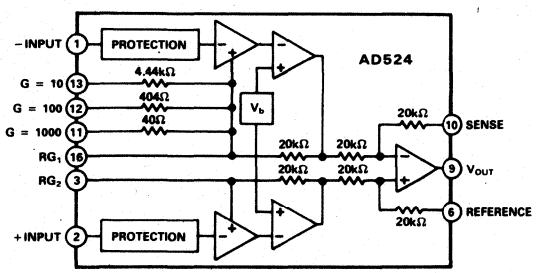
Performance
Low Drift: 2.0μV/°C (AD522B)
Low Nonlinearity: 0.005% (G = 100)
High CMRR: >110dB (G = 1000)
Low Noise 1.5μV p-p (0.1 to 100Hz)
Low Initial V_{OS}: 100μV (AD522B)

Versatility
Single-Resistor Gain Programmable: 1≤G≤1000
Output Reference and Sense Terminals
Data Guard for Improving ac CMR



AD524

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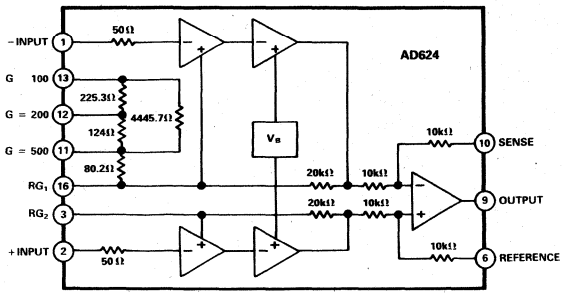
Low Noise: 0.3μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.003% (G = 1)
High CMRR: 120dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.5μV/°C
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 10, 100, 1000
Input Protection, Power On – Power Off
No External Components Required
Internally Compensated



AD624

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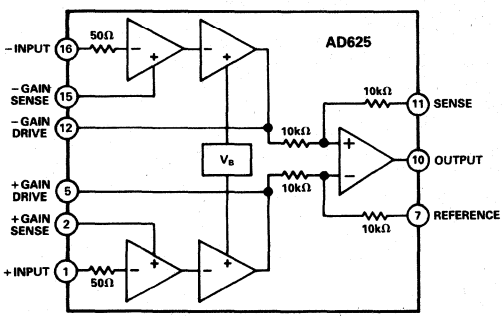
Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB max (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated



AD625

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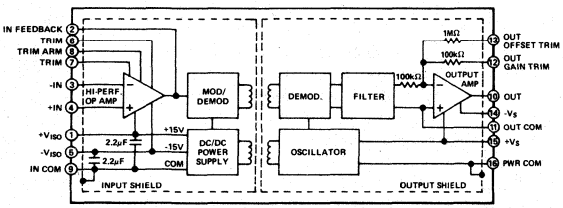
Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.001% max (G =1 to 500)
High CMRR: 130dB max (G = 500)
Low Offset Voltage: 25μV max
Low Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Internally Compensated
Versatile Gain Programming
Resistor Programmable Gain Amp
Software Programmable Gain Amp

Selection Guide
Isolation Amplifiers



MODEL 277

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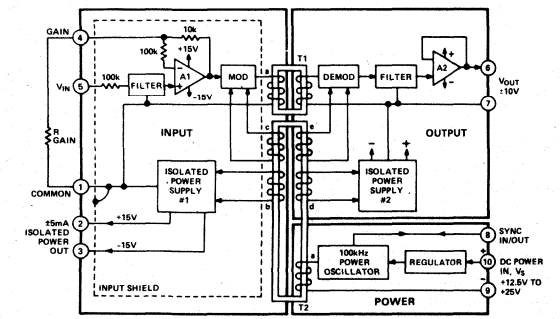
Versatile Op Amp Front End: Inverting, Noninverting, Differential Applications
Low Nonlinearity: 0.025% max, Model 277K
Low Input Offset Voltage Drift: 1μV/°C max, Model 277K
Floating Power Supply: ±15V dc @ ±15mA
High CMR: 160dB min @ dc
High CMV: 3500V_{rms}



MODEL 289

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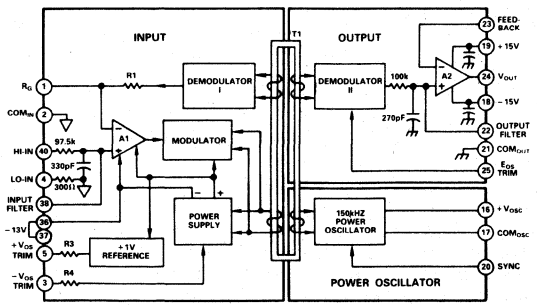
Low Nonlinearity: ±0.012% max (289L)
Frequency Response: (−3dB) dc to 20kHz (Full Power) dc to 5kHz
Gain Adjustable 1 to 100V/V, Single Resistor
3-Port Isolation: ±2500V CMV Isolation Input/Output
Low Gain Drift: ±0.005%/°C max
Floating Power Output: ±15V @ ±5mA
120dB CMR at 60Hz: Fully Shielded Input Stage
Meets UL Std. 544 Leakage: 2μA rms max, @ 115V ac, 60Hz



AD293

High Common-Mode Voltage: AD293 ±2500V peak max
Nonlinearity: ±0.05% max (AD293B)
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111
Hermetically Sealed Hybrid Construction

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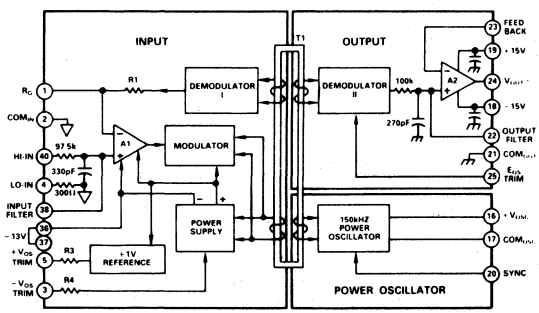

AD294

High Common-Mode Voltage: ±8000V peak max
Nonlinearity: ±0.05% of max
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz
Hermetically Sealed Hybrid Construction

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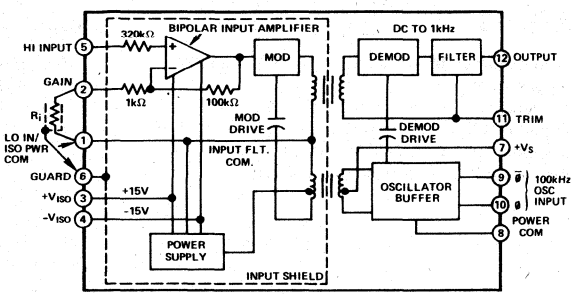
Selection Guide
Isolation Amplifiers



MODEL 284

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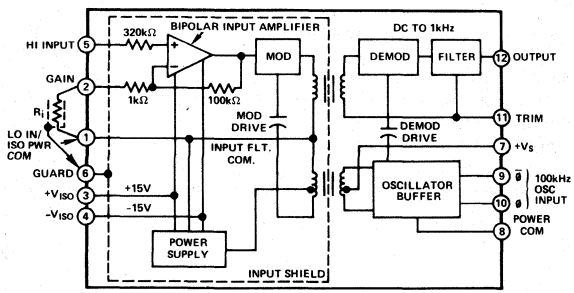
- High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous
- High CMR: 110dB min with 5kΩ Imbalance
- Low Nonlinearity: 0.05% @ 10V pk-pk Output
- High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
- Low Input Offset Voltage Drift: 10μV/°C, G = 100V/V
- Resistor Programmed Gain: 1 to 10V/V (284J)
- Isolated Power Supply: ±8.5V dc @ ± 5mA (284J)
- Meets IEEE Std 472: Transient Protection (SWC)
- Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.0μA max (284J)



MODEL 286

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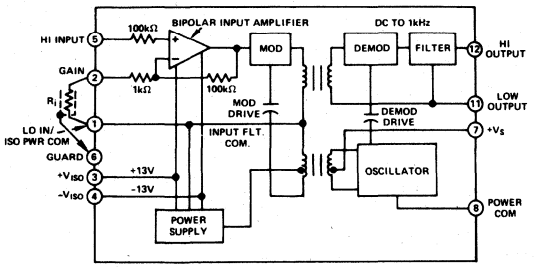
- High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous
- High CMR: 110dB min with 5kΩ Imbalance
- Low Nonlinearity: 0.05% @ 10V pk-pk Output
- High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
- Low Input Offset Voltage Drift: 10μV/°C, G = 100V/V
- Resistor Programmed Gain: 1 to 100V/V (286J)
- Isolated Power Supply: ±15V dc @ ± 15mA (286J)
- Meets IEEE Std 472: Transient Protection (SWC)
- Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.5μA max (284J)



MODEL 290A

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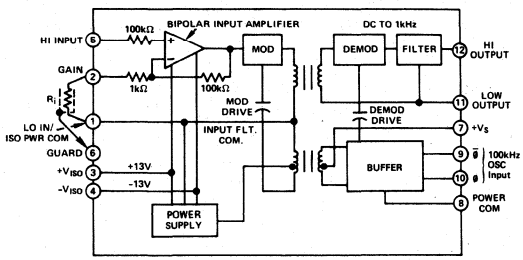
Isolated Power Supply: ±13V dc @ ±5mA (290A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ × 1.5″ × 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V



MODEL 292A

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Multichannel Capability Using External Oscillator (292A)
Isolated Power Supply: ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ × 1.5″ × 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

Orientation
Instrumentation & Isolation Amplifiers

An instrumentation amplifier is a committed "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain – usually from 1V/V to 1000V/V or more – and causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 1,

$$V_S - V_R = G\,(V^+ - V^-)$$

An ideal instrumentation amplifier responds only to the *difference* between the input voltages. If the input voltages are equal ($V^+ = V^- = V_{CM}$, the *common-mode voltage*), the output of the ideal instrumentation amplifier will be zero.

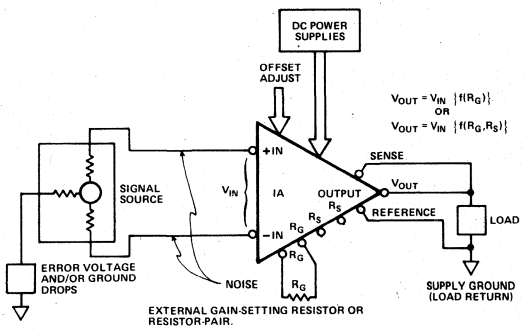


Figure 1. Basic Instrumentation Amplifier Functional Diagram

An amplifier circuit which is optimized for performance as an instrumentation-amplifier gain block has high input impedance, low offset and drift, low nonlinearity, stable gain, and low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples include: transducer amplification – for thermocouples, strain-gage bridges, current shunts, and biological probes, preamplification of small differential signals superimposed on high common-mode voltages, signal conditioning and (moderate) isolation for data acquisition, and signal translation for differential and single-ended signals wherever the common "ground" is noisy or of questionable integrity.

Instrumentation-amplifiers are usually chosen in preference to user-assembled op-amp circuitry, because they offer optimized, specified performance in low-cost, easy-to-use, compact packages. If the application calls for high common-mode voltages (typically, voltages in excess of the amplifier supply voltage), or if isolation impedances must be very high (e.g., $10^{10}\,\Omega$, with galvanic isolation, as in medical and industrial applications), the designer should consider an isolation amplifier.

SPECIFYING INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier chosen for a given application will be the lowest-cost device that satisfies the performance and environmental requirements. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. It is essential that the designer have a firm understanding of the specifications of instrumentation amplifiers and of the contributions of the various sources of error to the total error. The data sheets provide much useful application data on these devices, as well as examples of basic error analyses.

Definitions of the key specifications follow a brief discussion of instrumentation-amplifier architectures. For more-complete information on the fundamentals and applications of instrumentation amplifiers, a number of publications are available from Analog Devices.[1,2,3]

INSTRUMENTATION-AMPLIFIER ARCHITECTURE

All Analog Devices instrumentation amplifiers have two high-impedance input terminals, a set of terminals for gain-programming, an "output" terminal, and a pair of feedback terminals, labeled *sense* and *reference*, as well as terminals for power supply and offset trim.*

Two basic circuit concepts are employed. The AD522, AD524, AD624 and AD625 use variations of the well-known three-op-amp configuration, consisting of a differential input-output gain stage and subtractor stage. Gain ($\geq$1V/V) is set by the choice of a single gain-setting resistor, R_G. When the *sense* (V_S) feedback terminal is connected to the output terminal, and the *reference* terminal (V_R) is connected to power common, the output voltage appears between the output terminal and power common.

The V_S and V_R terminals may be used for remote sensing – to establish precise outputs in the presence of line drops; they may be used with an inside-the-loop booster follower to obtain power amplification without loss of accuracy; and they may be used to establish an output current that is precisely proportional to the difference signal. A voltage applied to the V_R terminal will bias the output by a predetermined amount. It is important always to maintain very low impedance (in relation to the specified V_S and V_R input impedances), when driving the V_S and V_R inputs, in order not to introduce common-mode, gain, and/or offset errors. In devices using the 3-amplifier configuration, the V_R terminal is sometimes used for "tweaking" common-mode rejection.

NOTES

[1] *"Applications Guide for Isolation Amplifiers*, 1984 edition, available upon request.

[2] "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, 1978, available upon request.

[3] *Transducer Interfacing Handbooks*, D.H. Sheingold, ed., 1980, $14.50, Analog Devices, Inc., P.O. Box 796, Norwood, MA 02062.

*In Model 612, *sense* is internally connected to the output terminal.

SPECIFICATIONS

Specification tables are generally headed by the legend: "specifications are typical at $V_S = \pm 15V$, $T_A = +25°C$, and rated load, unless otherwise noted." This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature), the significant effects are usually indicated within the specs. "Typical" means that the manufacturer's characterization process has shown this number to be "average," but individual devices vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Such specs are not uniquely applicable to instrumentation amps.

GAIN These specifications refer to the linear transfer function of the device; for example, the AD524 gain equation is: $G = 1 + \frac{40{,}000}{R_G}$ V/V. The value of R_G for a given gain value is: $R_G = \frac{40{,}000}{G - 1}\ \Omega$. For example, if G is to be 200V/V, R_G = 201 ohms.

Gain Range Specified at 1 to 1000, for example, the device may work at higher gains (1 V/V is minimum, except for the AD521), but the manufacturer does not specify performance outside the range. In practice, noise and drift may make higher gains impractical for a given device.

Equation Error (or "Gain Accuracy") The number given by this specification describes deviation from the gain equation when R_G is at its nominal value. The user can trim the gain or compensate for gain error elsewhere in the overall system. Systems using microprocessors (or computers, or other digital "intelligence") can be made self-calibrating, to take into account the lumped gain errors of all the stages in the analog portion of the system, from transducer to a/d converter.

Nonlinearity (or Gain Nonlinearity) Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best straight line," with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

Gain vs. Temperature These numbers give the deviations from the gain equation as a function of temperature.

SETTLING TIME is defined as that length of time required for the output voltage to approach and remain within a certain (±) tolerance of its final value. It is usually specified for a fast step that will drive the output through its full-scale range and it includes slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%, nor is settling time necessarily proportional to gain. Principal contributing factors include slew-rate limiting, underdamping (ringing), and thermal gradients ("long tails").

VOLTAGE OFFSET Voltage offset and common-mode rejection (see below) specifications are often considered the key figures of merit for instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involve "intelligent" processors can correct for offset errors in the whole measurement chain, but such applications are still relatively infrequent; in most applications, the instrumentation amplifier's contribution to system offset error must be defined.

Voltage offset and offset drift in instrumentation amplifiers are functions of gain.[4] The offset, measured at the output, is equal to a constant plus a term proportional to gain. For an amplifier with specified performance over a gain range from 1 to 1000, the constant is essentially the offset at unity gain, and the proportionality term (or slope) is equal to the change in output offset between G = 1 and G = 1000, divided by 999. To refer offset to the input (RTI), divide the total output offset by the gain. Since offset at a gain of 1000 is dominated by the proportional term, the slope is often called the "RTI offset, G = 1000." At any value of gain, the offset is equal to the unity-gain offset plus the product of the gain and the "RTI offset".

The same considerations apply to the offset drift. For example, the maximum RTI drift of the AD624C is specified at $0.25\mu V/°C$. Thus, the output drift is $(0.25\mu V/°C \times G) + 10\mu V/°C$ at any gain, G, in the range.

Voltage offset as a function of power supply level is also specified RTI at one or more gain settings.

INPUT BIAS AND OFFSET CURRENTS Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the junction-leakage of FET's. FET-input devices have lower bias currents than those using bipolar transistors, but FET leakage currents increase dramatically with temperature, approximately doubling every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

[4] There is a good explanation of the specification of offset in instrumentation amplifiers in ANALOG DIALOGUE 6–2 (1972), p. 14

Important Note
Although instrumentation amplifiers have differential inputs, there *must* be a return path for the bias currents. If it is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of "floating" sources, such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to common, or to the *guard* terminal. If a dc return path is impracticable, an *isolator* must be used.

COMMON-MODE REJECTION (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full-range common-mode voltage change (CMV), at a given frequency, and a specified imbalance of source impedance (e.g. 1kΩ source unbalance, at 60Hz). CMR is a logarithmic expression of the *common-mode rejection ratio* (CMRR): CMR = 20 $\log_{10}$ (CMRR). The common-mode rejection ratio is defined as the ratio of the signal gain, G, to the ratio of common mode signal appearing at the output to the input CMV.

In most instrumentation amplifiers, the CMR increases with gain, because the front-end configuration does not amplify common-mode signals, and the amount of common-mode signal appearing at the output stays relatively constant as the signal gain (G) increases.

However, at higher gains, amplifier bandwidth decreases. Since differences in phase shift through the differential input stage will show up as common-mode errors, CMR becomes more frequency-dependent at high gains.

ISOLATION AMPLIFIERS

The *isolation amplifier* (or *isolator*) has an input circuit that is galvanically isolated from the power supply and the output circuit. Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process-control systems.

Analog Devices Isolators described in this catalog use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input circuit.

CHOOSING AN ISOLATOR

The choice of an isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning), and the availability of isolated power for additional external front-end circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, a designers' guide[1], available upon request, provides information useful to the circuit designer.

Functional Characteristics The basic design of both amplifiers is identical. As shown in Figure 1, an amplifier is divided into three isolated sections—input, output, and power—coupled together by a single transformer. A power oscillator (which may be powered by system power or a separate power source) furnishes isolated power to the input amplifier, plus a carrier, which is modulated by the amplified input signal, coupled across the isolation barrier to the output section, demodulated, and buffer-amplified by a system-powered output amplifier.

Two significant innovations are responsible for the small size and excellent performance of these amplifiers. The first is an ultra-compact transformer, using screened wiring and well-conceived assembly technology. The second is an improvement in the use of the flyback (unclamped) portion of a blocking-oscillator waveform as the modulated signal carrier (U.S. Patent 4,286,225).

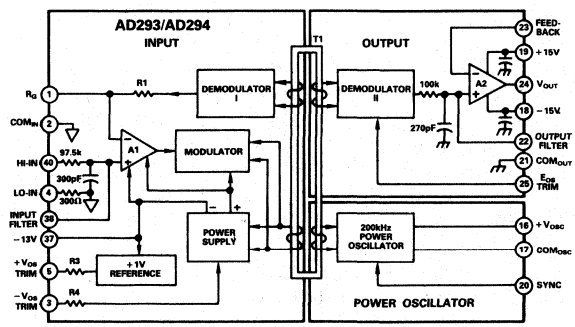


Figure 1. AD293/AD294 Block Diagram

*Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.

[1] *Analog Devices Applications Guide for Isolation Amplifiers* (1984)

As the block diagram shows, the synchronizable oscillator requires a two-wire power supply, which may be different (and (and isolated) from the power supply for the output amplifier, A2. The oscillator's output is coupled to (and loaded by, but isolated from) the circuitry connected to the other five identical transformer windings. One winding delivers power to the input amplifier, A1.

The flyback portion of the oscillator waveform is amplitude-modulate by A1's output signal, then coupled through separate transformer windings to a demodulator (I) in the amplifier's feedback path. Since A1 is an operational amplifier, the feedback signal must replicate the input signal (gain, from 1 to 100V/V, is equal to $1 + R_8/R_G$), and the transformer flux during flyback must be whatever is necessary to make this happen. The common flux, through an identical winding, applied to an identical demodulator (II), causes its output to be very nearly identical to the voltage at the output of the first demodulator, i.e., an accurately amplified version of the input signal. The other winding connected to Demodulator II provides a reference signal. The output of the demodulator is filtered and buffered by output amplifier, A2, which may be connected for gain values from 1 to 10V/V.

The AD293 and AD294 are *3-port* isolators; the input, output, and power sections are mutually isolated from one another. The use of separate substrates for the spiral-winding triplets of the transformer makes possible isolation of ±2500V (peak or continuous) for the AD293, and ±8000V (peak, 10ms pulse) for the AD294, between the input and output/power circuits. The high-temperature-fired dielectrics between the individual windings permit 500V rms of isolation between the output and power ports.

ANALOG DEVICES

Hybrid Industrial/ Medical Isolation Amplifier

AD293/AD294

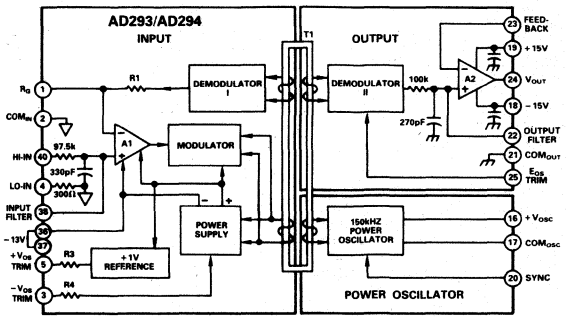
FEATURES

High Common-Mode Voltage:
AD293 ±2500V peak max, cont.
AD294 ±3500 peak max, cont.; ±8000V peak max Pulse
Nonlinearity: ±0.05% max (AD293B)
Adjustable Input & Output Gain: 1V/V to 1000V/V
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz

APPLICATIONS

Off Ground Signal Measurement
Industrial Control
Nuclear Instrumentation
High Voltage Protection for Data Acquisition Systems
Medical Diagnostic and Patient Monitoring Equipment

AD293/AD294 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD293/AD294 are low cost, high performance isolation amplifiers designed for accurate processing of low level, industrial sensor or biomedical signals, with true galvanic isolation from high common-mode voltages, transients and lethal ground fault currents. The true hybrid architecture of the AD293/AD294 includes a proprietary hybrid magnetic transformer, all housed in a low profile (0.3″) epoxy sealed, 40-pin ceramic package.

The AD293 features a maximum nonlinearity of 0.1% (AD293A) or 0.05% (AD293B) and maximum common-mode voltage isolation of either 2500V peak (continuous ac or dc) or 2500V rms (ac 60Hz, 1 minute). The AD294A provides a maximum nonlinearity of 0.1% and maximum common-mode voltage isolation of 3500V peak (continuous ac, dc) and common-mode voltage pulse (defibrillator) or transient protection of ±8000V peak.

In medical applications requiring patient isolation from lethal ground fault currents, the AD293/AD294 meet UL STD 544 leakage requirements by guaranteeing a maximum leakage current of 2μA rms (115V, 60Hz).

All versions provide small signal (−3dB) frequency response of 2.5kHz and a full power response of 200Hz (at gain of 1V/V). Both the input and output sections of the AD293/AD294 are gain programmable, allowing the user to tailor the amplifier to meet an application requirement.

WHERE TO USE THE AD293/AD294

Industrial: In process control systems, high CMV instrumentation and multi-channel computer interface systems, the AD293/AD294 provide guaranteed protection against high transient voltages, lethal ground fault currents and high common-mode voltages.

Medical: In biomedical and patient monitoring equipment such as ECG recorders, diagnostic systems and blood pressure monitors, the AD294A offers protection from lethal ground fault currents as well as 8kV peak defibrillator pulse inputs.

Low level signal recording and monitoring is achieved with the AD294A's low input noise (10μV p-p @ G = 100V/V) high CMR (100dB min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

Adjustable Gain: Gain can be selected at either the input, output, or both. Thus, circuit response can be tailored to the user's application. The input gain can be selected from 1V/V to 100V/V with a single resistor. The output gain can be selected from 1V/V to 10V/V with or without compensation. The AD293/AD294 provides the user with flexibility for circuit optimization without requiring external active components.

Buffered Output: The AD293/AD294 prevent inaccuracies related to low impedance loads by providing an uncommitted output amplifier capable of supplying ±10V @ 5mA min.

SPECIFICATIONS (typical @ + 25°C, & V_S = 15V unless otherwise noted)

MODEL	AD293A	AD293B	AD294A
GAIN			
Range	1 to 1000V/V	*	*
Formula (Input)	$G_{IN} = \left(1 + \frac{100k}{R_G}\right)$; $R_G \geq 1k\Omega$; G_{IN} max = 100		
(Output)	$G_{OUT} = \left(1 + \frac{R_A}{R_B}\right)$; $1 \leq G_{OUT} \leq 10$; G_{OUT} max = 10		
Deviation from Formula			
G = 1	± 1.0%	*	*
G > 1	± 3.0%	*	*
vs. Temperature (−25°C to +85°C)[1,2] (Gain = 1)	± 60ppm/°C max	*	*
(Gain > 1)	± 120ppm/°C max	*	*
Nonlinearity (± 5V swing)[2]	± 0.1% max	± 0.05% max	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	± 10V min	*	± 5V min
Max Safe Differential Input			
Continuous	120V rms max	*	*
1 Minute	240V rms max	*	*
Max CMV (Inputs to Outputs)			
Continuous (ac or dc)	± 2500V peak	*	± 3500V peak
ac, 60Hz, 1 minute Duration	2500V rms	*	3500V rms
Pulse, 10ms Duration, 1 pulse/10 sec	—	—	± 8000V peak
CMR (60Hz), G = 10V/V			
$R_S \leq 1k\Omega$ Balanced Source Impedance	108dB	*	*
$R_S \leq 1k$ Source Impedance Imbalance	100dB min	*	*
$R_S \leq 5k$ Balanced Source Impedance	—	—	100dB
$R_S \leq 5k$ Source Impedance Imbalance	—	—	95dB min
Leakage Current, Input to Output			
@ 115V ac, 60Hz	2μA rms max	*	*
Input Impedance, G = 1			
Differential	$150pF \| 10^8\Omega$	*	*
Overload	100kΩ	*	*
Common Mode	$30pF \| (5 \times 10^{10}\Omega)$	*	*
Input Bias Current			
Initial @ + 25 °C	2nA (5nA max)	*	*
vs. Temperature	20pA/°C	*	*
Input Noise			
Voltage			
0.05Hz to 100Hz	10μV p-p	*	*
10Hz to 1kHz	5μV rms	*	*
Current			
0.05Hz to 100Hz	50pA p-p	*	*
FREQUENCY RESPONSE			
Small Signal (−3dB) G = 1V/V to 100V/V	2.5kHz	*	*
Full Power, 20V p-p Output (10V p-p AD294)			
G = 1V/V (G_{IN} = 1V/V, G_{OUT} = 1V/V)	200Hz	*	*
G = 100V/V (G_{IN} = 100V/V, G_{OUT} = 1V/V)	100Hz	*	*
G = 10V/V (G_{IN} = 1V/V, G_{OUT} = 10V/V)	1.5kHz	*	*
Slew Rate	9.1V/ms	*	*
OFFSET VOLTAGE, REFERRED TO INPUT			
Inital, @ + 25°C, max	$\left(\pm 3 \pm \frac{22}{G_{IN}}\right)$mV	*	*
vs. Temperature (0 to + 70°C)	$\left(\pm 3 \pm \frac{150}{G_{IN}}\right)$μV/°C		$\left(\pm 10 \pm \frac{300}{G_{IN}}\right)$μV/°C max
(−25°C to + 85°C) max	$\left(\pm 10 \pm \frac{500}{G_{IN}}\right)$μV/°C max	$\left(\pm 5 \pm \frac{250}{G_{IN}}\right)$μV/°C	$\left(\pm 10 \pm \frac{1000}{G_{IN}}\right)$μV/°C
vs. Supply Voltage	$\left(\pm 0.01 \pm \frac{3}{G_{IN}}\right)$mV/V	*	*
RATED OUTPUT			
Voltage, 2kΩ Load	± 10V min	*	*
Output Impedance	< 1Ω	*	*
Output Ripple, (dc to 100kHz) Bandwidth	4mV p-p	*	*
POWER SUPPLY[3]			
Voltage, Rated Performance	± 15V dc ± 3%	*	*
Voltage, Operating[4]	± 12V dc ± 18V dc	*	*
Current, Quiescent (V_S = ± 15V)	+ 1mA, − 1mA	*	*
(+V_{OSC} = + 15V)	+ 11mA	*	*
ISOLATED POWER	− 13V dc @ 200μA	*	*
TEMPERATURE RANGE			
Rated Performance	− 25°C to + 85°C	*	*
Operating	− 40°C to + 100°C	*	*
CASE DIMENSIONS	2.64" × 0.86" × 0.35"	*	*
PACKAGE OPTION[5]	HY20A	*	*

NOTES
*Specifications same as AD293A.
[1]Gain temperature drift is specified as a percentage of output signal level @ 10V pk-pk.
[2]Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3]Recommended power supply, ADI Model 904, ± 15V @ 50mA output.
[4]Output Swing = 0.66V_S
[5]See Section 19 for package outline information.
Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	R_G	40	HI-IN
2	COM_{IN}		
3	$-V_{OS}$ TRIM	38	INPUT FILTER
4	LO-IN	37	−13V
5	$+V_{OS}$ TRIM	36	−13V
16	$+V_{osc}$	25	E_{OS} TRIM
17	COM_{OSC}	24	V_{OUT}
18	−15V	23	FEEDBACK
19	+15V	22	OUTPUT FILTER
20	SYNC	21	COM_{OUT}

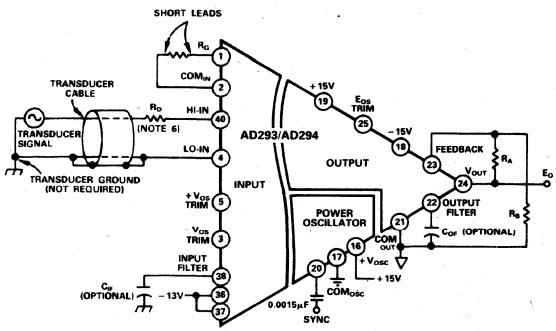
Synchronization: The unique hybrid transformer design and low power consumption of the AD293/AD294 result in very low RFI (carrier) levels which make it unnecessary to synchronize adjacent amplifiers in a multi-channel application, since "beat frequency" and cross talk caused by intermodulation are virtually eliminated.

If desired by the user, multiple AD293/AD294's may be synchronized by connecting a 0.0015μF capacitor in series with each amplifier's SYNC terminal (pin 20) and driving them with a TTL compatible, 150kHz (±10%) source. SYNC input impedance for each amplifier is approximately 8kΩ.

High Reliability: The AD293/AD294 are designed specifically to provide highly reliable operation in extremely harsh environments. These devices are available in epoxy sealed ceramic packages which use hybrid techniques and incorporate a revolutionary new hybrid magnetic transformer eliminating traditional wire wound methods.

INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of the AD293/AD294, care must be taken to keep the capacitance balanced about the input terminals. Use twisted shielded cable, for the input signal, to reduce inductive and capacitive pickup. The cable shield should be connected to the common-mode signal source and as close as possible to their respective terminal connections so pick-up can be minimized (shown in Figure 1).



NOTES:
1. GAIN RESISTORS R_G, R_A AND R_B, 1% 50ppm/°C METAL FILM TYPE.
2. INPUT GAIN $= 1 + \frac{100k}{R_G}$; $R_G \geq 1k$; MAX INPUT GAIN = 100V/V.
3. OUTPUT GAIN $= 1 + \frac{R_A}{R_B}$; $1 \leq$ OUTPUT GAIN ≤ 10.
   FOR OUTPUT GAIN > 1, A 33pF MAY BE REQUIRED ACROSS R_A.
4. $C_{IF} = \frac{1}{2\pi F(9.75 \times 10^4)}$ FARADS −330pF.
5. $C_{OF} = \frac{1}{2\pi F(10^5)}$ FARADS −270pF.
6. R_D IS REQUIRED ONLY FOR THE AD294 TO PROVIDE PROTECTION AGAINST DEFIBRILLATOR PULSES. USE TWO 240kΩ 1/2 WATT RESISTORS. WHEN MOUNTING, PLACE THEM IN SERIES AND AWAY FROM THE PCB.

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The AD293/AD294 attribute their outstanding performance to the innovation of a hybrid magnetic ceramic transformer T1 (shown in the block diagram of Figure 2). Windings are screened on two ceramic alumina substrates which are placed together separated by a ceramic isolation barrier. Then an E-core is carefully fitted around the substrates to complete the transformer.

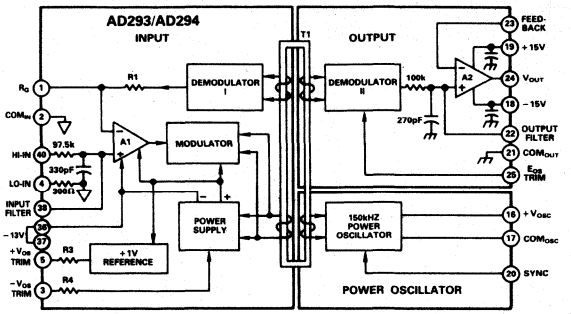


Figure 2. AD293/AD294 Block Diagram

Incorporating the carrier isolation technique, both power and signals are transferred between the amplifier's input stage and output circuitry via T1. The input signal is filtered and appears at the noninverting input of amplifier A1. This signal is then amplified by A1, with its gain (1V/V to 100V/V) determined by the value of resistance connected between R_G and COM_{IN}. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulator output voltage is filtered and then buffered by A2. Output gain (1V/V to 10V/V) and frequency compensation is determined by the value of resistance and capacitance selected between A2's feedback, V_{OUT}, and COM terminals. The 150kHz asymmetric square wave power oscillator drives the primary windings of transformer T1. The secondary windings of T1 then energizes the input power supply and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance effects are developed from stray capacitance that couple the input and output terminals together. The difference shown in Figure 3 between the AD293 and AD294 is a result of the separate transformer designs. Each terminal capacitance is shunted by leakage resistance exceeding $3.4 \times 10^9\Omega$.

Terminal Ratings: CMV performance is given in peak pulse and continuous ac or dc peak ratings. Continous peak ratings apply from dc up to the normal full power response frequencies. Figure 3 illustrates the AD293/AD294 ratings between terminals.

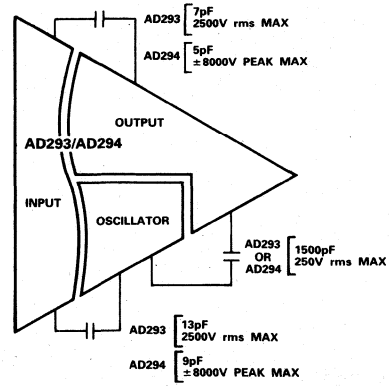


Figure 3. Interelectrode Capacitance and Terminal Ratings

OFFSET AND GAIN TRIM PROCEDURES

The calibration procedure, shown in Figure 4, illustrates the recommended techniques which can be used to minimize output error. In this example, the output span is +10V to −10V and gain = 100V/V (G_{IN} = 10V/V; G_{OUT} = 10V/V).

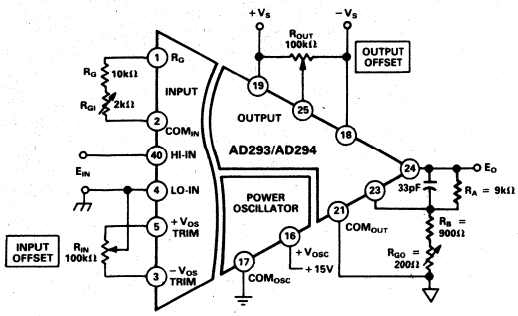


Figure 4. Recommended Offset & Gain Adjustments

Offset Adjustment

1. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
2. Apply E_{IN} = 0 volts and adjust R_{IN} for E_O = 0 volts.
3. Connect R_B to COM.
4. Adjust R_{OUT} for E_O = 0 volts.

Gain Adjustment

5. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
6. Apply E_{IN} = +1.000V and adjust R_{G_1} for E_O = +10.000V.
7. Connect R_B to COM.
8. Apply E_{IN} = +0.100V and adjust R_{G_0} for E_O = +10.000V.

LEAKAGE CURRENT LIMITS

The low coupling capacitance between input and output yields a ground leakage current of less than 2μA rms of 115V ac, 60Hz in the AD293/AD294 which meet standards established by UL STD 544.

For medical applications, the AD293/AD294 are designed to improve on patient safety current limits proposed by the F.D.A., U.L., A.A.M.I. and other regulatory agencies.

In patient monitoring equipment, such as ECG recorders, the AD293/AD294 will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. With the use of passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

PERFORMANCE CHARACTERISTICS

Phase vs. Frequency: The phase vs. frequency responses for the AD293/AD294, is shown in Figure 5. The bandwidth is sufficient for the majority of isolation applications where accurate signal measurements must be made in the presence of noise and high common-mode voltages.

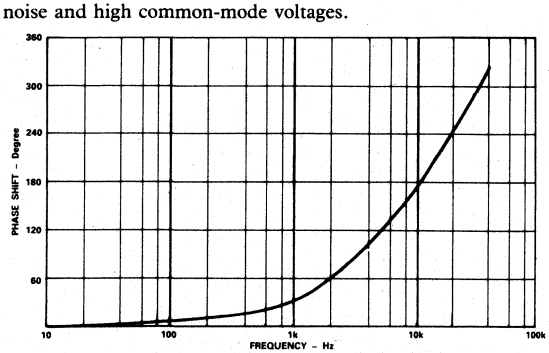


Figure 5. Typical AD293/AD294 – Phase vs. Frequency

Common-Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, input signal frequency and amplifier gain. CMR is rated at 60Hz and 1kΩ (AD293)/5kΩ (AD294) source impedance imbalance at a gain of 1V/V. Figure 6 illustrates the CMR vs. frequency characteristics for the AD293/AD294. CMR approaches 144dB at dc with sources impedance as high as 1kΩ (AD293)/5kΩ (AD294). Figure 7

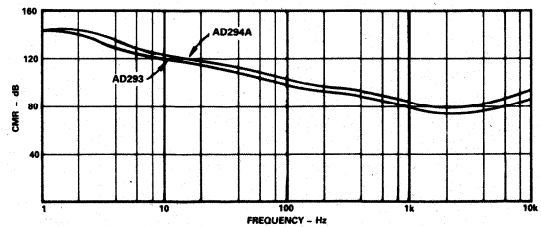


Figure 6. Typical AD293/AD294 – CMR vs. Frequency

illustrates the effect of source impedance imbalance on CMR performance at 60Hz for various gain settings. CMR is maintained greater than 60dB for source imbalances up to 100kΩ. As shown, increasing isolator gain increases CMR.

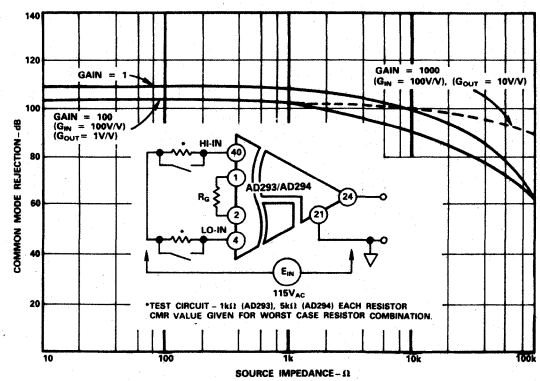


Figure 7. Typical AD293/AD294 – CMR vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise in a bandwidth from 10Hz to 100kHz is shown on the horizontal axis. The peak-to-peak value is derived by multiplying the rms value @ F = 100Hz (0.75μV rms) by 6.6.

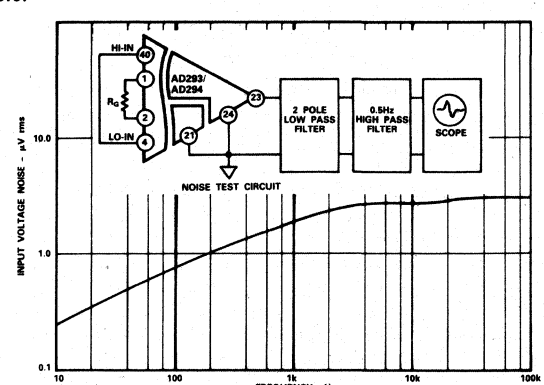


Figure 8. Typical AD293/AD294 – Input Noise vs. Frequency

For applications requiring improved noise performance, additional low pass filters may be placed at either the input or output sections to selectively roll-off noise and undesired signals beyond the bandwidth of interest.

Gain Nonlinearity vs. Gain

Figure 9, shows the AD293/AD294 gain nonlinearity vs. gain as a function of output gain. As input gain is increased, gain nonlinearity increases. Conversely, as output gain is increased to ten, gain nonlinearity decreases.

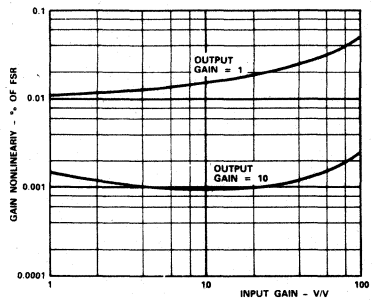


Figure 9. Typical AD293/AD294 – Gain Nonlinearity vs. Gain as a Function of Output Gain

Full Power Bandwidth vs. Gain

Figure 10 shows the full power bandwidth vs. gain with the input and output gain curves shown separately. As shown, the full power bandwidth with gain provided at the input is typically 200Hz. But with gain provided only at the output, the full power bandwidth approaches the small signal bandwidth.

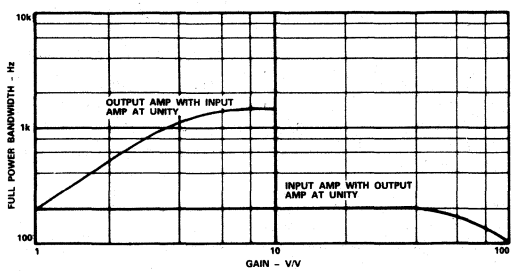


Figure 10. Typical AD293/AD294 - Full Power Bandwidth vs. Gain

Gain Nonlinearity vs. Output Swing

The gain nonlinearity vs. output swing, for the AD293/AD294, is illustrated in Figure 11. As shown, increasing either the input gain or the output swing will cause the gain nonlinearity to increase if the output gain is held to 1V/V.

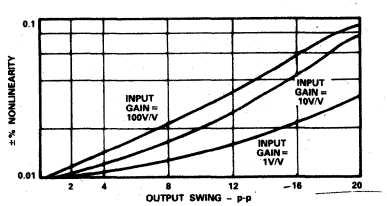


Figure 11. Typical AD293/AD294 - Gain Nonlinearity vs. Output Swing

OPTIMIZING THE AD293/AD294

The AD293/AD294 can be optimized for many applications as shown by the performance charts on the previous page. Gain and filtering can be implemented on both the input and output stages while providing true galvanic isolation. Provisions for an additional two poles of filtration are also available without the addition of external operational amplifiers. Due to their low power consumption and novel transformer design, the beat frequency problem normally associated with adjacent isolation amplifiers is eliminated. A sync terminal is provided for applications where ultra-sensitive circuitry might interpret the isolator carrier frequency.

SELECTING GAIN

The AD293/AD294 contain both input and output amplifiers (see Figures 1 and 2), the gains of which can be set independently. The selection of a particular combination tailors isolator properties to the application, minimizes errors, and optimizes frequency response.

Nonlinearity is the deviation of response from a straight line. This error arises from slight differences in responses of the input demodulator I and demodulator II, their respective transformer windings responses, and rectification of carrier signal in the input stage due to large signal amplitudes in this section. Hence, linearity is best obtained by raising output gain and lowering input gain.

Gain errors are deviations in slope from the predicted gain equation. Gain errors are attributable to the difference in gain between demodulators I and II. These errors are quite small, due to the highly predictable and uniform nature of the thick-film transformer. The gain drift of this portion of gain error is also small. Since this gain error source dominates at unity gain, the unity gain temperature coefficients of these units is very small. As input gain is taken, errors arise due to the inaccuracies of the internal feedback resistor R1, and user selected R_G. Failure of these resistors to temperature track introduces a gain TC. R1 is trimmed within ±3% and has a TC of ±100ppm/°C. Since the temperature coefficient of R1 is not user controllable, best gain TC at low gains is favored by taking output gain. The output stage also contributes gain error only when gain is taken. Here, both the feedback and gain resistors are user supplied and can be made as accurate as desired.

Offset errors are apparent both in the input stage and in the transformer-output stage combination. Provisions are available to eliminate these initial offset errors at both the input and output stages through trim potentiometers. These errors also have temperature dependence where at unity gain, output offset drift dominates. Taking output gain multiplies output drift by the gain taken. Taking input gain helps dilute output stage offset drift and is recommended where offset drift is to be minimized.

Errors due to small signal and large signal bandwidth limitations can also be optimized in the AD293/AD294. Small signal bandwidth is limited by lack of gain as frequency is raised, a condition caused by the necessity to limit bandwidth internally to preserve stability in the A1, modulator, input demodulator loop. The input stage contains most of the small signal bandwidth limitations thus, taking input gain limits small signal bandwidth (see Figure 10). The demodulators limit slew rate and large signal bandwidth. Apparent slew rate at the isolator output is

multiplied by gain taken in the output stage. With maximum gain taken in the output stage, large signal bandwidth for moderate swings approaches small signal bandwidth (shown in Figure 10). Thus applying input gain limits bandwidth while output gain enhances it.

FILTERING

With the AD293/AD294, the addition of filtering can be implemented in a number of different configurations without the use of external operational amplifiers. Capacitors can be placed in series with the input or output terminals or configured in combination with the gain setting resistors to tailor performance. An input filter terminal and an output filter terminal are provided for user selectable filtration. Characteristics are determined by the formulas shown in Figure 1.

REDUCING NORMAL-MODE VOLTAGE

A prime isolator function is the rejection of common-mode signals. The extremely high input to output resistance of isolators allows excellent rejection of dc common-mode voltages. As frequency rises, the small capacitance across the isolation barrier causes an ac common-mode current to flow through that barrier, which is proportional to applied common-mode voltage, frequency and barrier capacitance. Since the isolation mechanism (transformer T1) is more initimately connected to the input low terminal than the input high terminal, the bulk of common-mode current flows through the input low terminal. Any resistance in series with the input source and the input low terminal then develops a normal-mode voltage, which may constitute objectionable interference.

An isolator cannot separate normal-mode interference from the desired signal without help, but interference can be rejected in several ways.

Conversion of common-mode current to normal-mode voltage can be reduced by minimizing resistance in the input low lead. In the AD293/AD294 CMR is enhanced and input trimming sacrificed by returning the input signal to pin 2. With known stable source resistances common-mode current to normal-mode voltage conversion can also be cancelled as shown in Figure 13.

ISOLATED INDUSTRIAL APPLICATIONS

As illustrated in Figure 14, the AD293 can be applied where differential signal sources are used such as an isolated strain gauge. With a third wire connected to the common-mode potential of that source, a common-mode current is forced to flow through the third wire and through the isolation barrier; thus, sparing the differential input wires the necessity of conducting the common-mode current. In this manner, the isolator is responsive to only the differential inputs while ignoring the passage of common-mode currents. Input gain is selected via R_G and determined by the input gain formula.

MEDICAL APPLICATIONS

In medical applications, a good connection to the patient, even on the third wire cannot be guaranteed due to electrode resistance to and through the skin. Illustrated in Figure 12 is a medical front end with right leg drive powered by the AD294A. Here the common-mode drive amplifier helps force common-mode current to flow in the third wire in preference to the differential input wires. The FET input has low noise current to avoid development of voltage noise in the input protection resistors. These resistors protect the input from defibrillator pulses with the AD294A having the capability of withstanding an 8kV pulse. The patient is also protected from fault currents due to input component failure. It is necessary to connect the third wire to establish the input common-mode level. If not connected the input common-mode level, with respect to common of the input section power supplies, will cause the isolator to drift out of its linear range. Layout is also very important, both for common-mode rejection and isolation.

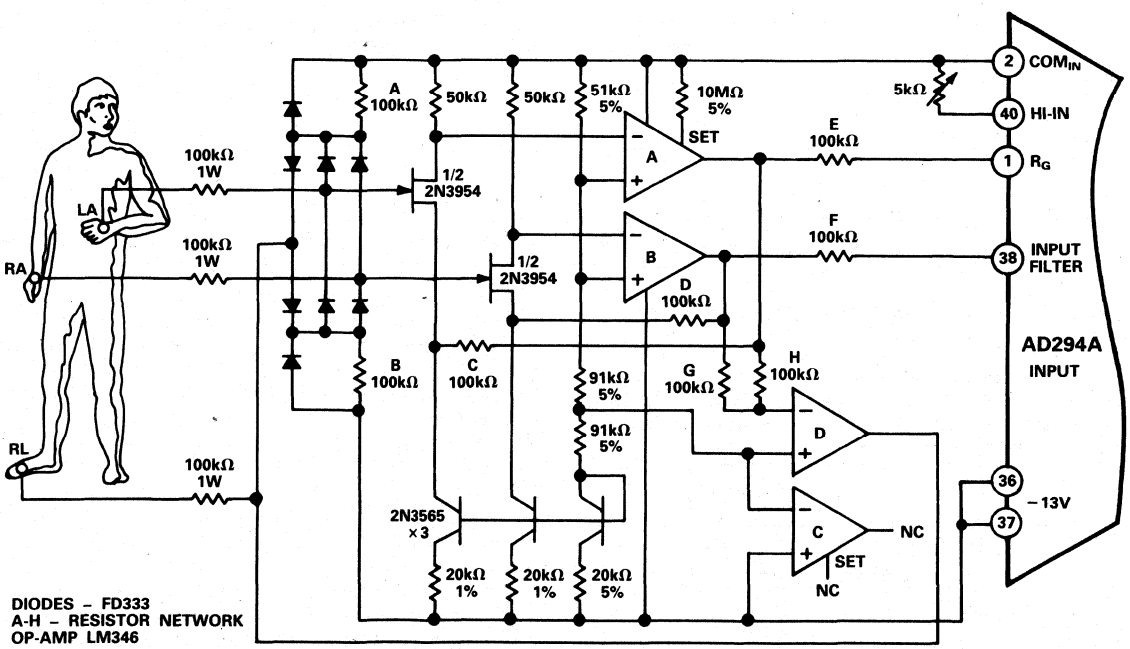


Figure 12. Multilead Medical Application Using the AD294A with Right Leg Drive

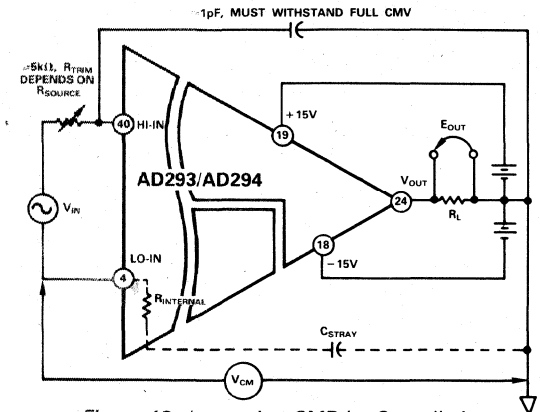


Figure 13. Improving CMR by Cancellation

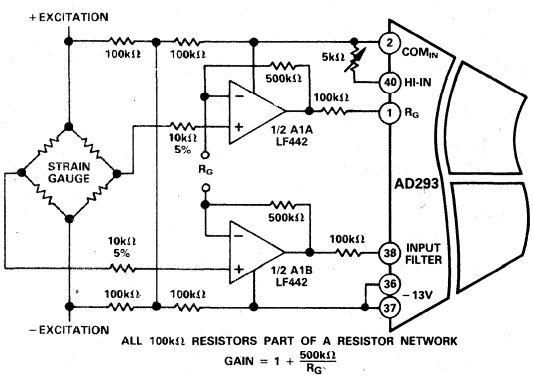


Figure 14. Isolated Strain Gauge Using Front End of AD293

CURRENT LOOP INTERFACE

Illustrated in Figure 15, the AD293 provides an isolated sensor interface that is compatible with standard 4-to-20mA current loops. Here high common-mode rejection and high common-mode voltage suppression are easily attained with the AD293. The AD293 conditions the 0V to 10V input signal and provides a proportional voltage at the isolator's output. Then the circuitry shown converts it into a 4 to 20mA current, which in turn, may be applied to the loop load R_L.

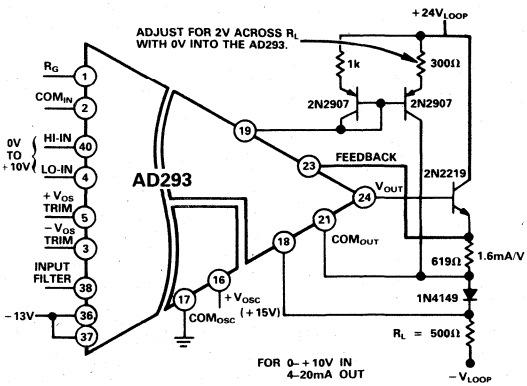


Figure 15. Isolated Current Loop Interface

TEMPERATURE MEASUREMENT AND COLD JUNCTION COMPENSATION

Illustrated in Figure 16, the AD293 can be used for isolated temperature measurements while providing cold junction compensation. With the circuitry connected as shown, the LM334 must be thermally connected to the cold junction terminal for an accurate temperature measurement to be made of this terminal. In this configuration, accurate temperature measurements using the industry's popular J type thermocouple can be made. For example, assume 1V out of the AD293 at 100°C. From the ANSI tables, the output voltage of a J thermocouple at 100°C is 0.005268V. Set the gain of the AD293 at 1V/0.005268V = 189.8, $R_G = 530\Omega$. With the thermocouple junction open, set the voltage between points A and B to 0.015V by adjusting the 500Ω pot. Connect a voltage reference source in place of the thermocouple. Set its output to zero. Set the output of the AD293 to zero by adjusting the 100Ω pot. Set the reference source to 0.005268V. The output of the AD293 should read 1V.

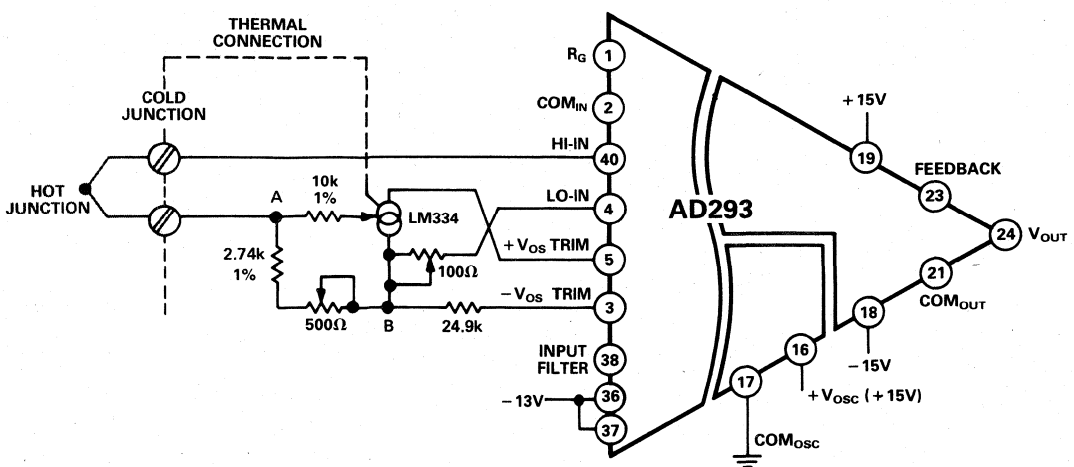


Figure 16. Temperature Measurement & Cold Junction Compensation

DRIVING CAPACITIVE LOADS

For driving capactive loads greater than 1000pF, compensation should be implemented as shown in Figure 17. Here a 100pF capacitor and 100Ω resistor are used to insure that the AD293 output stage remains stable. These components can also be changed to tailor frequency response to the particular application. The 100Ω resistor isolates the output of the AD293 while the 100pF provides response lead.

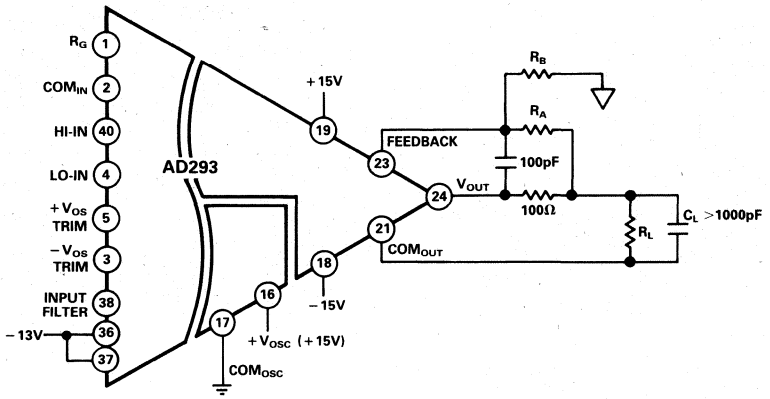


Figure 17. Driving Capacitive Loads

INCREASING OUTPUT DRIVE CAPABILITY

For applications requiring increased output drive, Figure 18 illustrates a single solution. Here the output voltage of the AD293 is conditioned and applied to the drive circuitry. R_A will supply the output stage with unity gain as connected. For gain to be added to the output stage, connect R_B as shown. Output gain will be determined by the output equation previously stated in the specifications. For output gain >1V/V, C_O should also be implemented so output stability will be insured. With this output drive circuitry, 200Ω loads can be easily driven with ±10V @ 50mA.

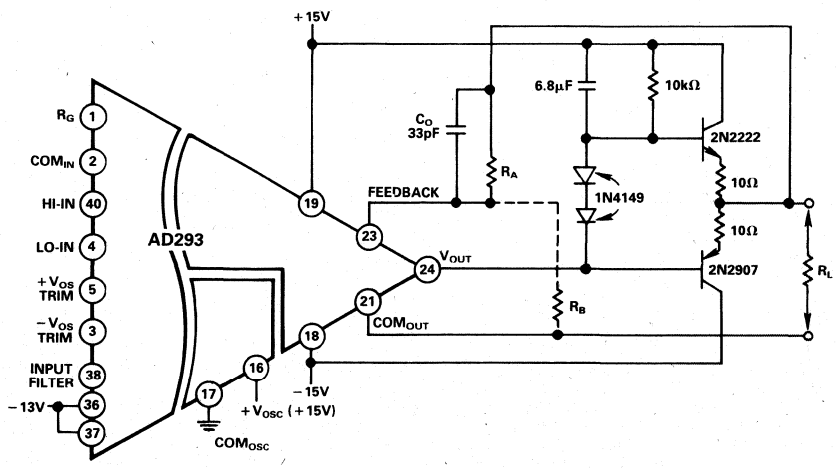


Figure 18. Increasing Output Drive Capability

ANALOG DEVICES

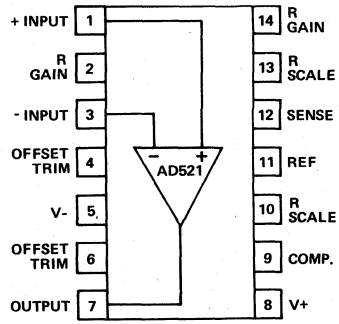
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Low Drift: 2μV/°C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000

AD521 FUNCTIONAL BLOCK DIAGRAM



TO-116

PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9 \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	*	*	*
Equation	$G = R_S/R_G V/V$	*	*	*
Error from Equation	(±0.25–0.004G)%	*	*	*
Nonlinearity (Note 2)				
1≤G≤1000	0.2% max	*	0.1% max	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	*	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*	*
Impedance	0.1Ω	*	*	*
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>2MHz	*	*	*
G = 10	300kHz	*	*	*
G = 100	200kHz	*	*	*
G = 1000	40kHz	*	*	*
Small Signal, ±1.0% Flatness				
G = 1	75kHz	*	*	*
G = 10	26kHz	*	*	*
G = 100	24kHz	*	*	*
G = 1000	6kHz	*	*	*
Full Peak Response (Note 3)	100kHz	*	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*	*
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7μs	*	*	*
G = 10	5μs	*	*	*
G = 100	10μs	*	*	*
G = 1000	35μs	*	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	*	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	*	*	*
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	2μV/°C max	**
vs. Supply	3μV/%	*	*	*
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	**
vs. Supply (Note 6)	$0.005V_{OS_O}$/%	*	*	*
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs. Supply	2%/V	*	*	*
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	$3 \times 10^9 \Omega \| 1.8pF$	*	*	*
Common Mode Input Impedance (Note 8)	$6 \times 10^{10} \Omega \| 3.0pF$	*	*	*
Input Voltage Range for Specified Performance (with respect to ground)	±10V	*	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*	*
Voltage at either input (Note 9)	V_S ±15V	*	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\,\mu V$	*	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\,\mu V$	*	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*	*
REFERENCE TERMINAL				
Bias Current	3μA	*	*	*
Input Resistance	10MΩ	*	*	*
Voltage Range	±10V	*	*	*
Gain to Output	1	*	*	*
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	*	*	*
Quiescent Supply Current	5mA max	*	*	*
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	*	*	–55°C to +125°C
Operating	–25°C to +85°C	*	*	–55°C to +125°C
Storage	–65°C to +150°C	*	*	*
PACKAGE OPTION[1]: TO-116 Style (D14A)	AD521JD	AD521KD	AD521LD	AD521SD

NOTES
[1] See Section 19 for package outline information.
*Specifications same as AD521JD.
**Specifications same as AD521KD.
Specifications subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S −0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 8.

5

DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.

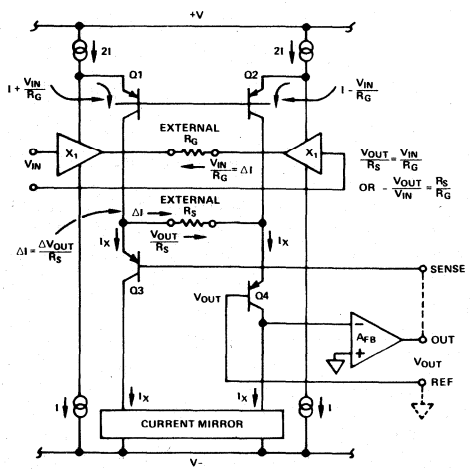


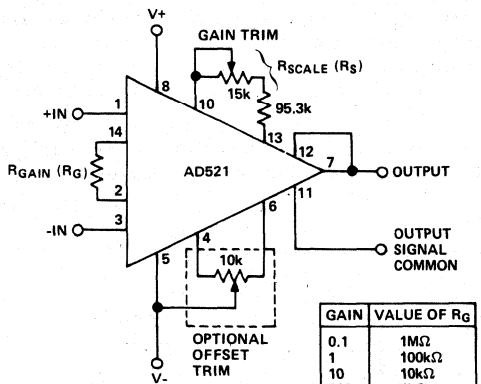
Figure 1. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 and above 1000 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V especially for gain equal to or less than 1.

2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

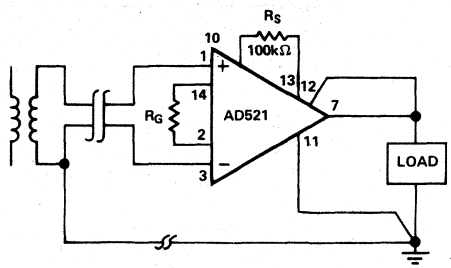


GAIN	VALUE OF R_G
0.1	1MΩ
1	100kΩ
10	10kΩ
100	1kΩ
1000	100Ω

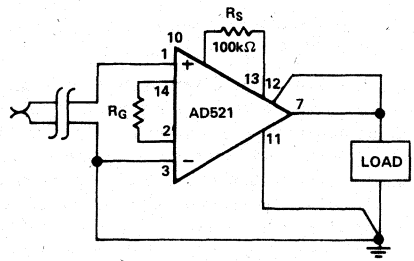
Figure 2. Operating Connections for AD521

3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 2). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.

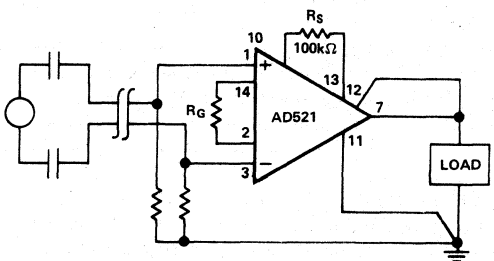
4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.



a). Transformer Coupled, Direct Return

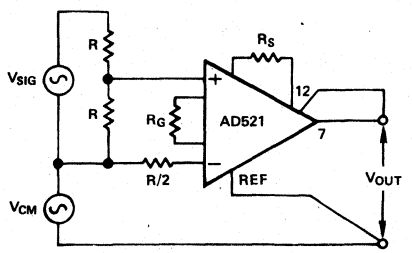


b). Thermocouple, Direct Return



c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE R_G TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for $V_{IN} \approx V_S = 10V$

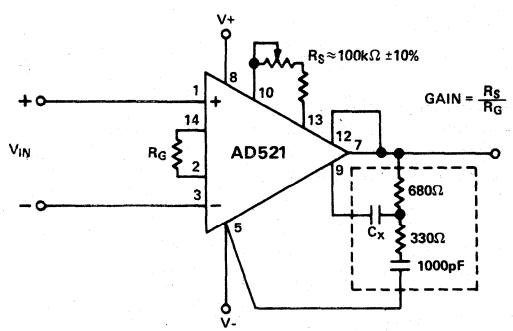
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V- to the output with little or no attenuation. Therefore, it is advisable to decouple the V- supply line to the output common or to pin 11.[1]



$$C_X = \frac{1}{100\pi f_t} \text{ when } f_t \text{ is the desired bandwidth.}$$

(f_t in kHz, C_X in μF)

Figure 5. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

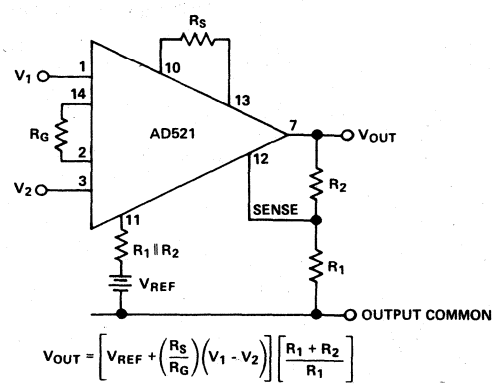
By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 2) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_G). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.



$$V_{OUT} = \left[V_{REF} + \left(\frac{R_S}{R_G}\right)(V_1 - V_2)\right]\left[\frac{R_1 + R_2}{R_1}\right]$$

Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R1 and R2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 6.

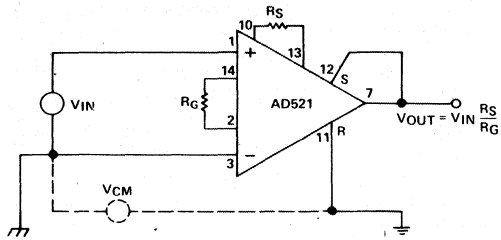


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

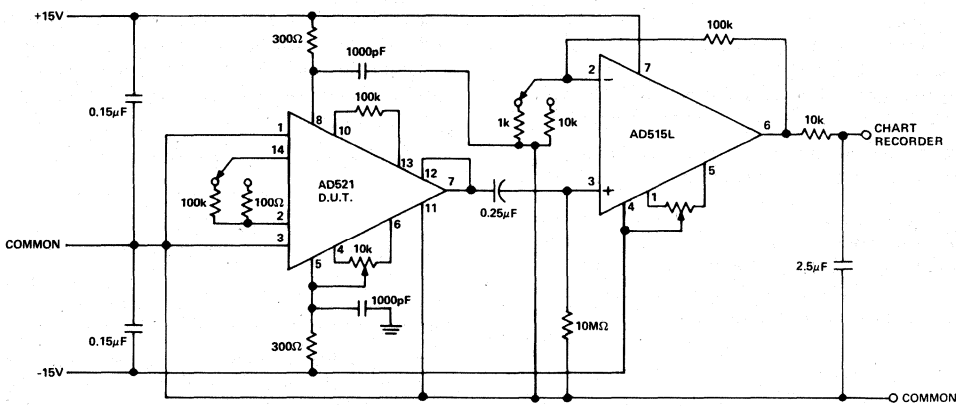


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

ANALOG DEVICES

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)

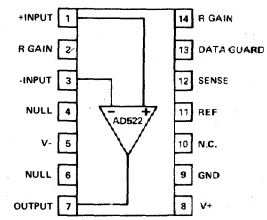
Versatility

- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR

AD522 FUNCTIONAL BLOCK DIAGRAM



14-PIN DIP

PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gauges, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 2.0μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the extended aerospace temperature range of -55°C to +125°C. All versions are packaged in a 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

SPECIFICATIONS[1] (typical @ +V_S = ±15V, R_L = 2kΩ & T_A = +25°C unless otherwise specified)

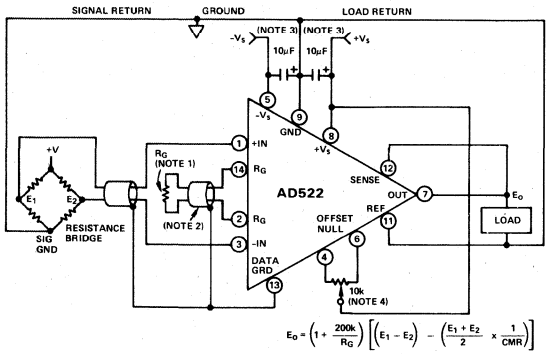
MODEL	AD522AD	AD522BD	AD522SD
GAIN			
Gain Equation	$1 + \frac{2\ (10^5)}{R_g}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	**
G = 1000	0.01%	0.005%	**
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	*	*
DYNAMIC RESPONSE (see Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/μs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
$1 < G < 1000$	$\pm(\frac{50}{G} + 6)$μV/°C	$\pm(\frac{25}{G} + 2)$μV/°C	$\pm(\frac{100}{G} + 6)$μV/°C
vs. Supply, max			
G = 1	±20μV/%	*	*
G = 1000	±0.2μV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	*	*
vs. Temperature	±100pA/°C	*	*
Input Offset Current			
Initial max, +25°C	±20nA	*	*
vs. Temperature	±100pA/°C	*	*
INPUT			
Input Impedance			
Differential	10^9Ω	*	*
Common Mode	10^9Ω	*	*
Input Voltage Range			
Maximum Differential Input, Linear	±10V	*	*
Maximum Differential Input, Safe	±20V	*	*
Maximum Common Mode, Linear	±10V	*	*
Maximum Common Mode Input, Safe	±15V	*	*
Common Mode Rjection Ratio, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1.5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	**
PACKAGE OPTION[2]	Ceramic[3] – HY14A	Ceramic[3] – HY14A	Metal – HY14D

NOTES
[1] Specifications guaranteed after 10 minute warm-up.
[2] See Section 19 for package outline information.
[3] Analog Devices reserves the right to ship metal packages in lieu of the standard ceramic packages for A and B grades.

*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



NOTES:
1. GAIN RESISTOR R_G SHOULD BE <5ppm/°C (VISHAY TYPE RECOMMENDED).
2. SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS. WHEN NOT USED, THE DATA GUARD PIN CAN BE LEFT UNCONNECTED.
3. POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS.
4. NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202-Y-10k) IS RECOMMENDED.

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

5

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table I)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table 1 lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocessor controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec. Sheet and Fig. 4)	±0.002	±0.002
Voltage Drift	$\frac{25\mu V/^\circ C}{\text{Gain}}$ + 2.0μV/°C = 4.5μV/°C R.T.I. = 0.00055%/°C (from Spec. Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs. F vs. G, typical curve)	±0.005	±0.005
Noise, R.T.O. (0.1 to 100Hz)	15μV (p-p) R.T.O. (from Spec. Sheet, Noise vs. G typical curve)	±0.0015	±0.0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec. Sheet) = ±50μV/°C = ±1.25μV R.T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table I. Error Sources

these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

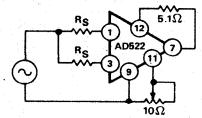


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in four drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

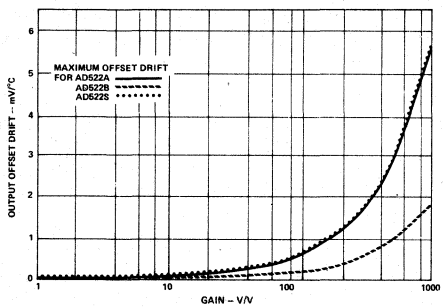


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

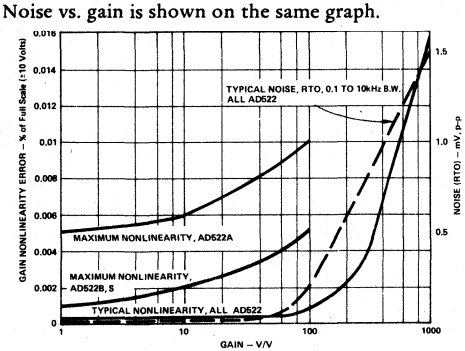


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

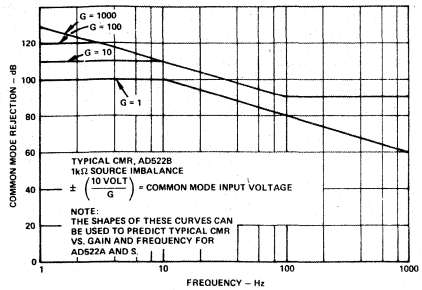


Figure 5. Common Mode Rejection vs. Frequency and Gain

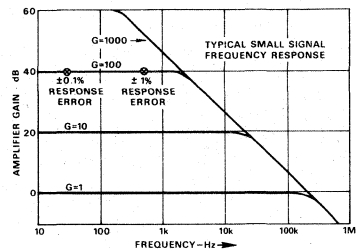


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

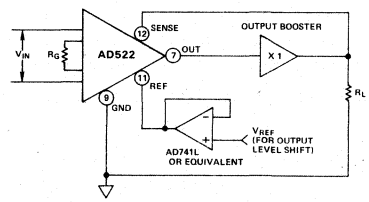


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

ANALOG DEVICES

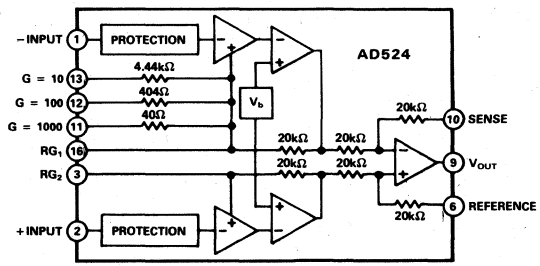
Precision Instrumentation Amplifier

AD524

FEATURES

- **Low Noise: 0.3μV p-p 0.1Hz to 10Hz**
- **Low Nonlinearity: 0.003% (G = 1)**
- **High CMRR: 120dB (G = 1000)**
- **Low Offset Voltage: 50μV**
- **Low Offset Voltage Drift: 0.5μV/°C**
- **Gain Bandwidth Product: 25MHz**
- **Pin Programmable Gains of 1, 10, 100, 1000**
- **Input Protection, Power On – Power Off**
- **No External Components Required**
- **Internally Compensated**

AD524 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from −25°C to +85°C. The "S" grade guarantees performance to specification over the extended temperature range −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 20V step (G = 100).

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 10			±0.25			±0.15			±0.1%			±0.25	%
G = 100			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±2.0			±1.0			±0.5			±2.0	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10, 100			±0.01			±0.005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0.01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			250			100			50			100	µV
vs. Temperature			2			0.75			0.5			2.0	µV/°C
Output Offset Voltage			5			3			2.0			3.0	µV
vs. Temperature			100			50			25			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 10	85			95			100			95			dB
G = 100	95			105			110			105			dB
G = 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_D)		±10			±10			±10			±10		V
Max Common Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 10	90			95			100			90			dB
G = 100	100			105			110			100			dB
G = 1000	110			115			120			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal – 3dB													
G = 1		1			1			1			1		MHz
G = 10		400			400			400			400		kHz
G = 100		150			150			150			150		kHz
G = 1000		25			25			25			25		kHz

Model	AD524A			AD524B			AD524C			AD524S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate		5.0			5.0			5.0			5.0		V/μs
Settling Time to 0.01%, 20V Step													
G = 1 to 100		15			15			15			15		μs
G = 1000		75			75			75			75		μs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		7			7			7			7		nV/√Hz
R.T.O.		90			90			90			90		nV/√Hz
R.T.I., 0.1 to 10Hz													
G = 1		15			15			15			15		μV p-p
G = 10		2			2			2			2		μV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		μV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ± 20%
I_{IN}		15			15			15			15		μA
Voltage Range	± 10			± 10			± 10			± 10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ± 20%
I_{IN}		15			15			15			15		μA
Voltage Range	± 10			± 10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	− 25		+ 85	− 25		+ 85	− 25		+ 85	− 55		+ 125	°C
Storage	− 65		+ 150	− 65		+ 150	− 65		+ 150	− 65		+ 150	°C
POWER SUPPLY													
Power Supply Range	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**	mA
PACKAGE[1]		D16A			D16A			D16A			D16A		

NOTES

[1]See Section 19 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Typical Characteristics

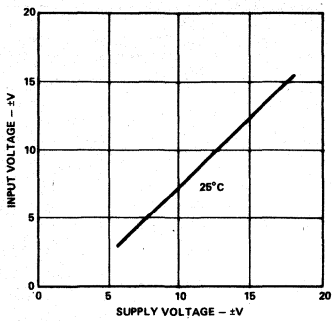


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

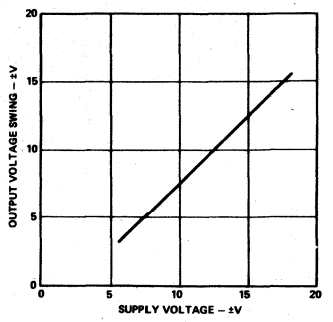


Figure 2. Output Voltage Swing vs. Supply Voltage

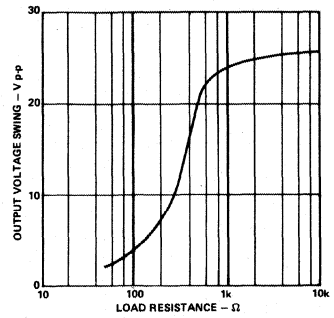


Figure 3. Output Voltage Swing vs. Resistive Load

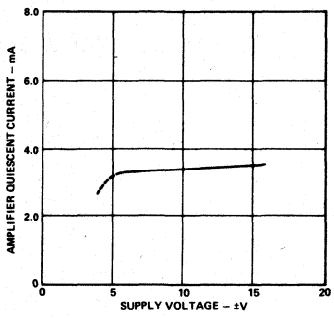


Figure 4. Quiescent Current vs. Supply Voltage

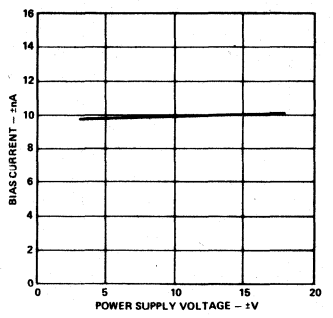


Figure 5. Input Bias Current vs. Supply Voltage

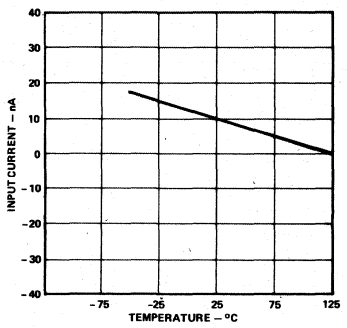


Figure 6. Input Bias Current vs. Temperature

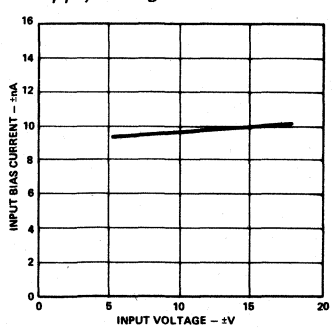


Figure 7. Input Bias Current vs. CMV

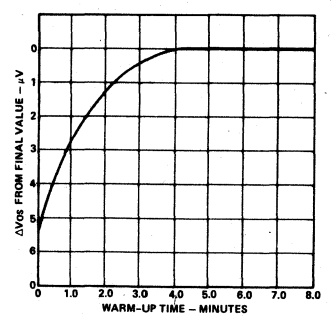


Figure 8. Offset Voltage, RTI, Turn on Drift, G = 1000

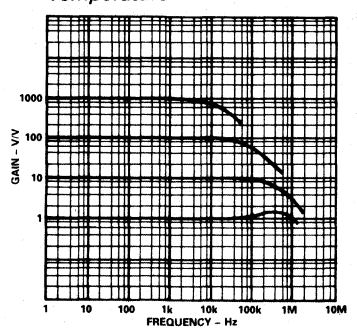


Figure 9. Gain vs. Frequency

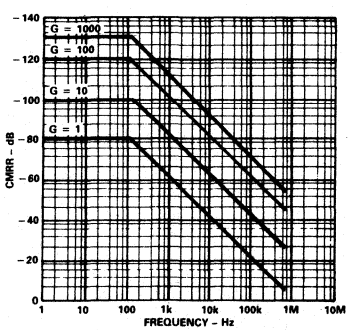


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

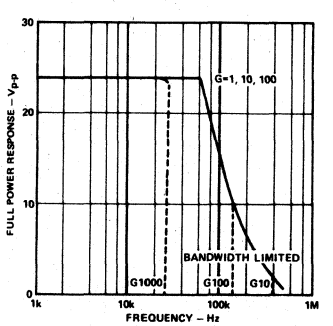


Figure 11. Large Signal Frequency Response

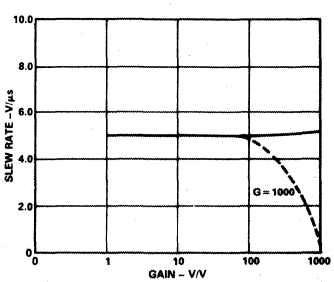


Figure 12. Slew Rate vs. Gain

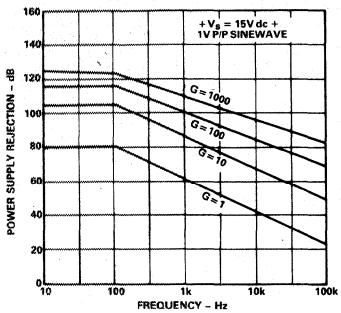


Figure 13. Positive PSRR vs. Frequency

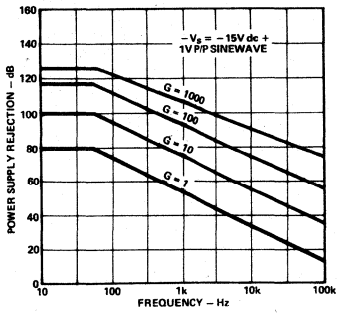


Figure 14. Negative PSRR vs. Frequency

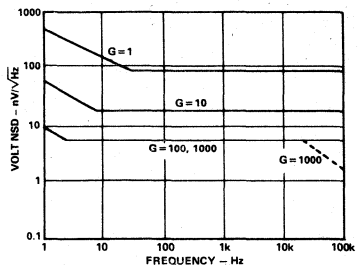


Figure 15. RTI Noise Spectral Density vs. Gain

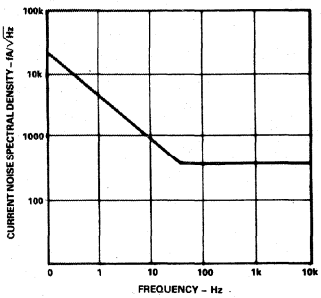


Figure 16. Input Current Noise

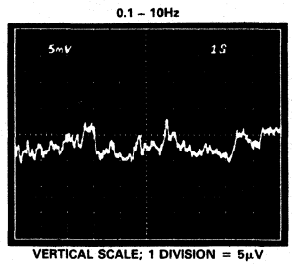


Figure 17. Low Frequency Noise – G = 1 (System Gain = 1000)

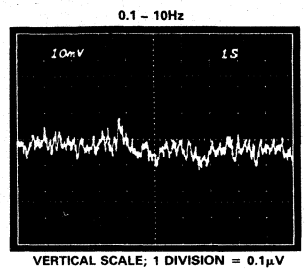


Figure 18. Low Frequency Noise – G = 1000 (System Gain = 100,000)

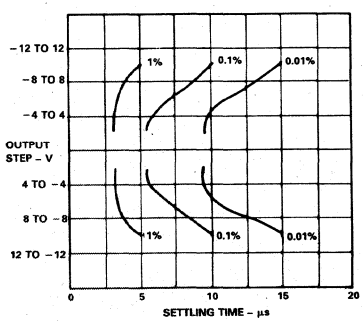


Figure 19. Settling Time Gain = 1

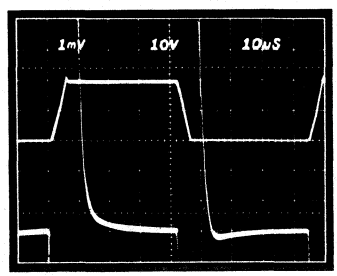


Figure 20. Large Signal Pulse Response and Settling Time – G = 1

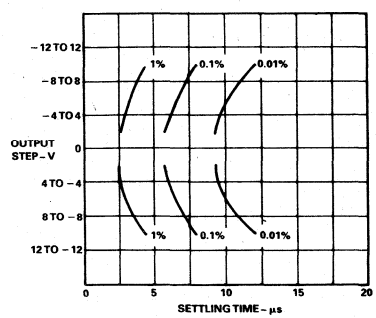


Figure 21. Settling Time Gain = 10

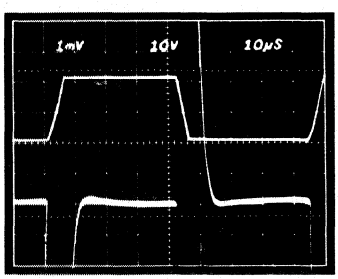


Figure 22. Large Signal Pulse Response and Settling Time G = 10

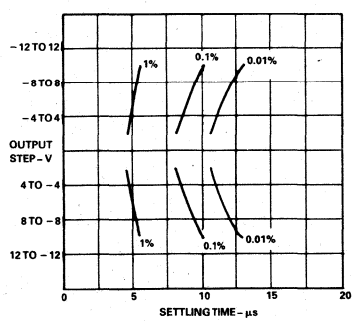


Figure 23. Settling Time Gain = 100

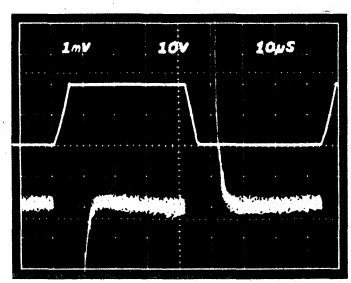


Figure 24. Range Signal Pulse Response and Settling Time G = 100

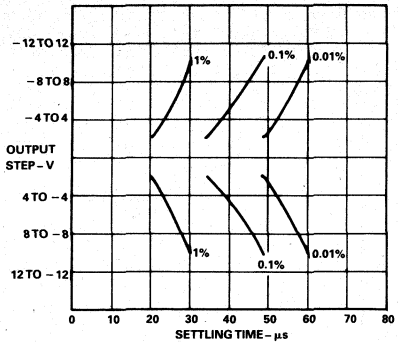


Figure 25. Settling Time Gain = 1000

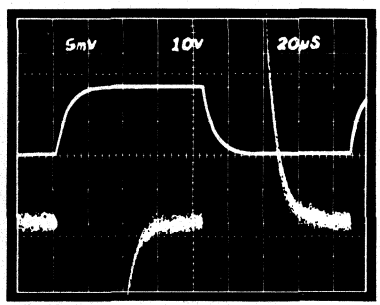


Figure 26. Large Signal Pulse Response and Settling Time G = 1000

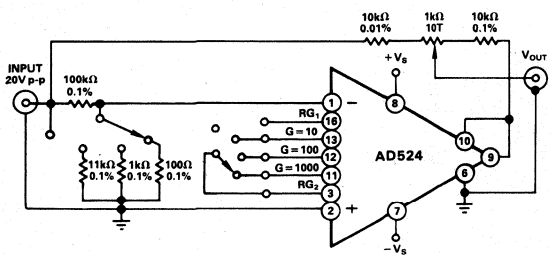


Figure 27. Settling Time Test Circuit

Theory of Operation

The AD524 is a monolithic instrumentation amplifier based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents Q1, Q2, Q3 and Q4 to be constant which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 30ppm. Second, the

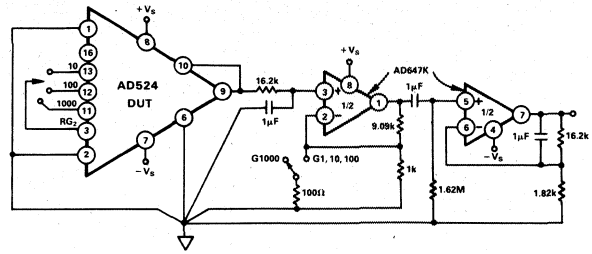


Figure 28. Noise Test Circuit

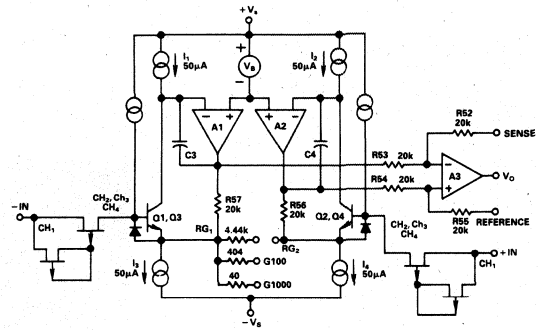


Figure 29. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit

gain bandwith product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $7nV/\sqrt{Hz}$ at G = 1000.

INPUT PROTECTION

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit input current to below 5mA with a full differential overload (36V) would require over 7k of resistance which would add $10nV\sqrt{Hz}$ of noise. To provide both input protection and low noise a special series protect FET was used.

A unique FET design was used to provide a bidirectional current limit, thereby, protecting against both positive and negative overloads. Under nonoverload conditions, three channels CH_2, CH_3, CH_4, act as a resistance ($\approx 1k\Omega$) in series with the input as before. During an overload in the positive direction, a fourth channel, CH_1, acts as a small resistance ($\approx 3k\Omega$) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH_1 and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3mA over the 36V range.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD524 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimize offset voltage changes in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gain of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G=1 RG_2 is not connected).

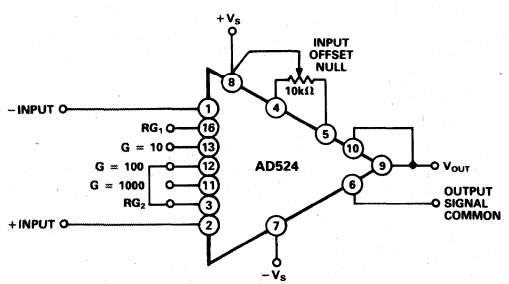


Figure 30. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between pins 3 and 16 which programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 31). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−50ppm/°C typ).

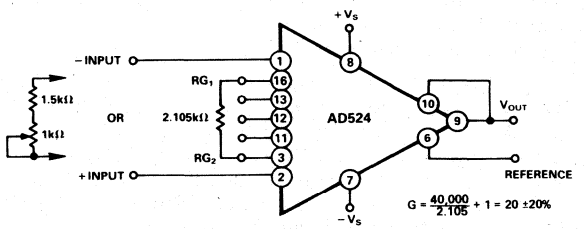


Figure 31. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor (Figure 32). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

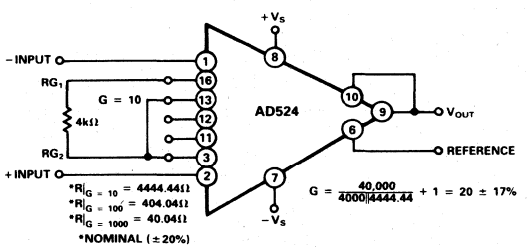


Figure 32. Operating Connections for G = 20, Low Gain T.C. Technique

The AD524 may also be configured to provide gain in the output stage. Figure 33 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

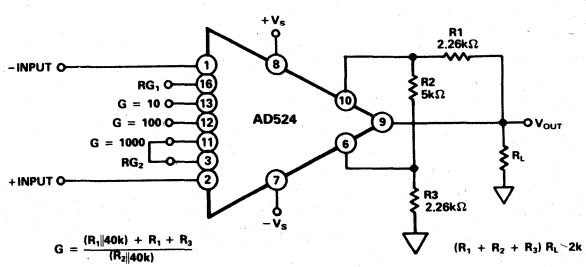


Figure 33. Gain of 2000

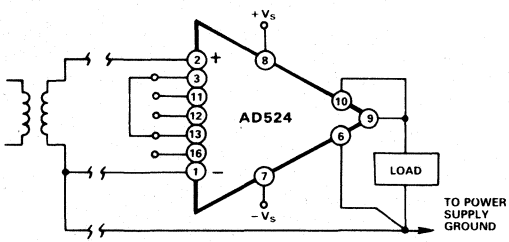
Output Gain	R2	R1,R3	Nominal Gain
2	5kΩ	2.26kΩ	2.02
5	1.05kΩ	2.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

Table I. Output Gain Resistor Values

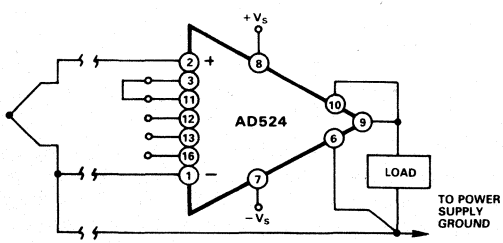
INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

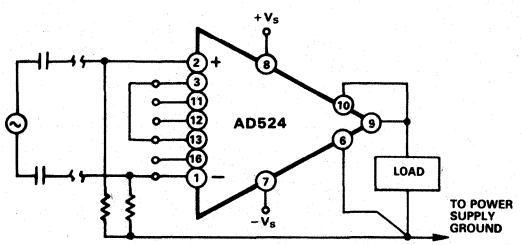
Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 34. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common mode rejection errors unless the shield is properly driven. Figures 35 and 36 shows active data guards which are configured to improve ac common mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

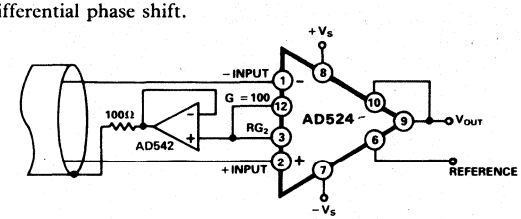


Figure 35. Shield Driver, G ≥ 100

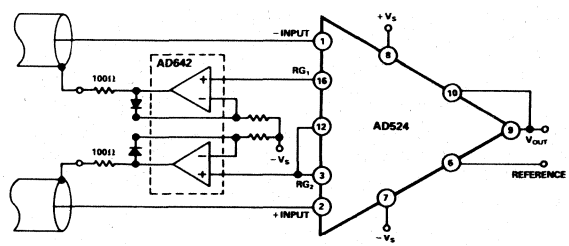


Figure 36. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths

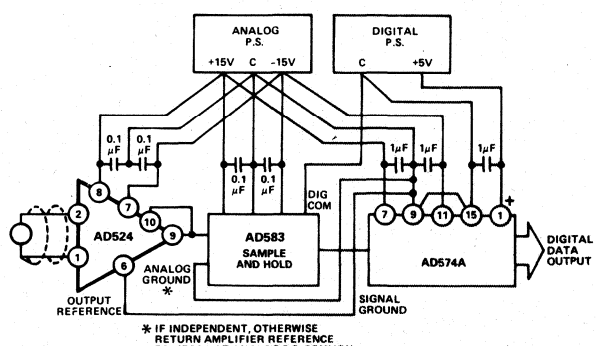


Figure 37. Basic Grounding Practice

have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

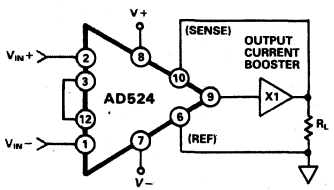


Figure 38. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 38 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset.

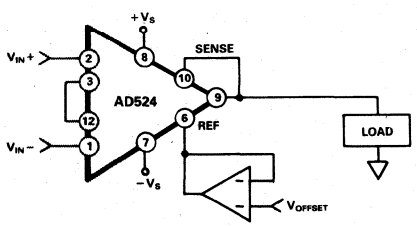


Figure 39. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA.

In the AD524 a reference source resistance will unbalance the CMR trim by the ratio of $20k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 86dB ($20k\Omega/1\Omega = 86dB$). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 39. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 40.

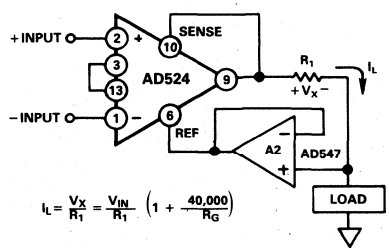


Figure 40. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 41 shows the AD524 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

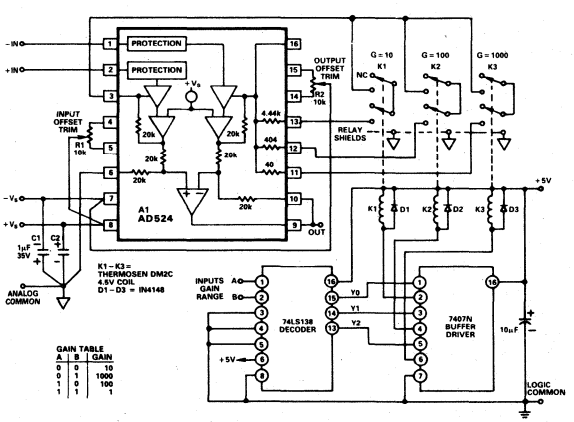


Figure 41. 3 Decade Gain Programmable Amplifier

The AD524 can also be connected for gain in the output stage. Figure 42 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common rejection ratio degradation.

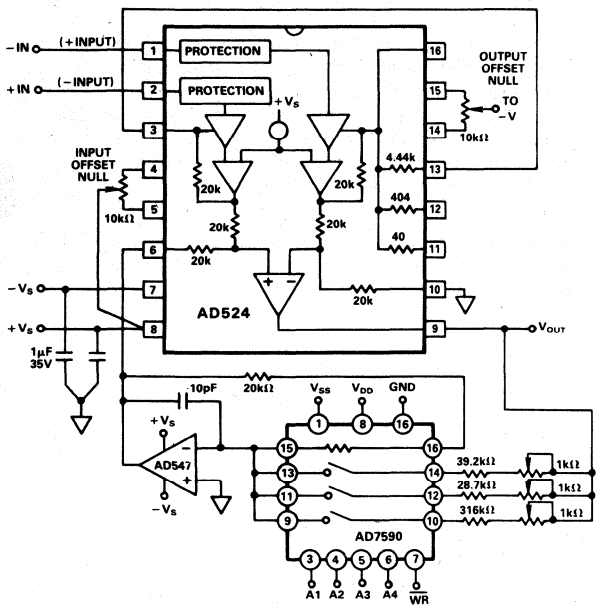


Figure 42. Programmable Output Gain

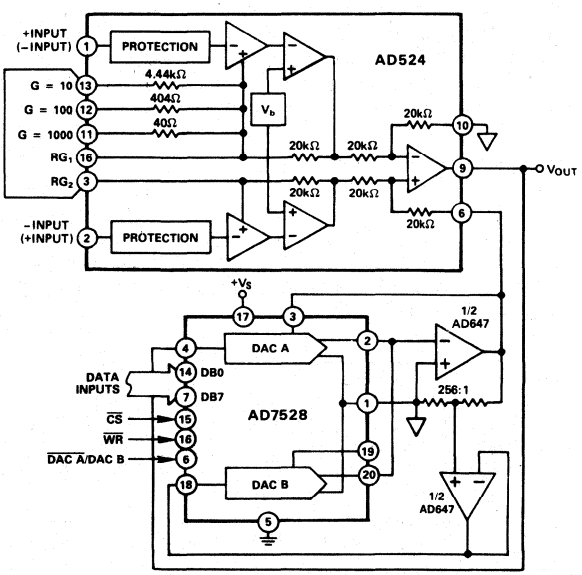


Figure 43. Programmable Output Gain Using a DAC

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 44 show a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

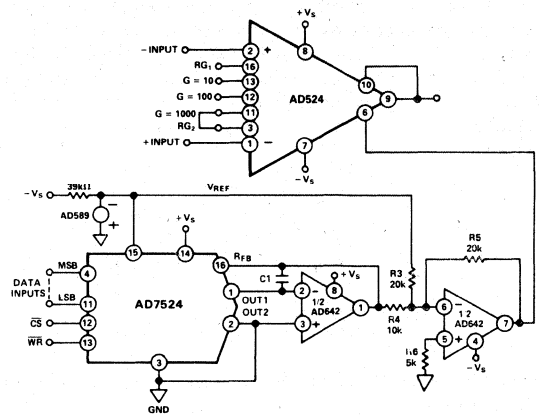


Figure 44. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For those applications Figure 45 provides a hardware solution.

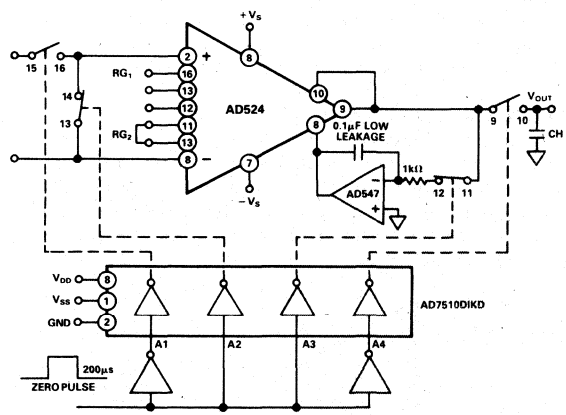


Figure 45. Auto-Zero Circuit

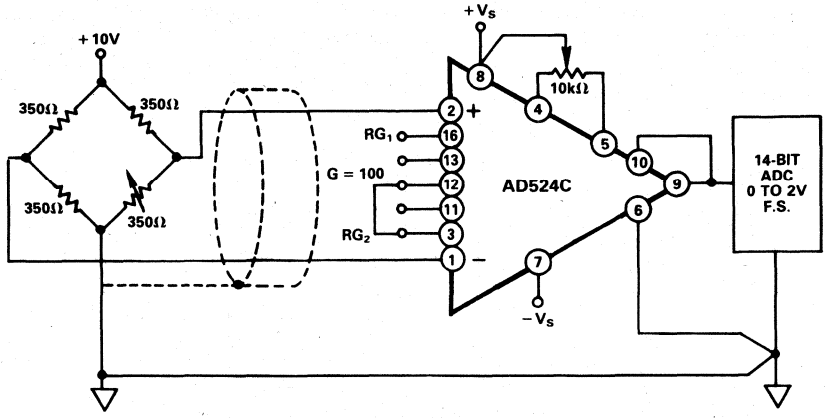


Figure 46. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 46 shows a differential transducer, unbalanced by 100Ω, supplying a 0 to 20mV signal to an AD524C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500ppm	2500ppm	2500ppm	–
Gain Instability	25ppm	(25ppm/°C)(60°C) = 1500ppm	–	1500ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30ppm	–	–	30ppm
Input Offset Voltage	±50μV, RTI	±50μV/20mV = ±2500ppm	2500ppm	2500ppm	–
Input Offset Voltage Drift	±0.5μV/°C	(±0.5μV/°C)(60°C) = 30μV 30μV/20mV = 1500ppm	–	1500ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±25μV/°C	(±25μV/°C)(60°C) = 1500μV 1500μV/20mV = 750ppm	–	750ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(100Ω) = 1.5μV 1.5μV/20mV = 75ppm	75ppm	75ppm	–
Bias Current – Source Imbalance Drift	±100pA/°C	(±100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(100Ω) = 1μV 1μV/20mV = 50ppm	50ppm	50ppm	–
Offset Current – Source Imbalance Drift	±100pA/°C	(100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 8.8μV 8.8μV/20mV = 444ppm	444ppm	444ppm	–
Noise, RTI (0.1–10Hz)	0.3μV p-p	0.3μV p-p/20mV = 15ppm	–	–	15ppm
		Total Error	6656.5ppm	10516.5ppm	45ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD524CD in Bridge Application

Figure 47 shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple–iron(+)–constantan– is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A.

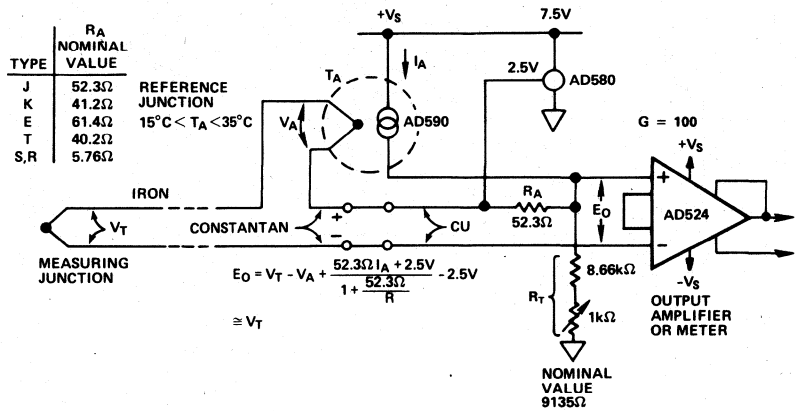


Figure 47. Cold-Junction Compensation

The microprocessor controlled data acquisition system shown in Figure 48 includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

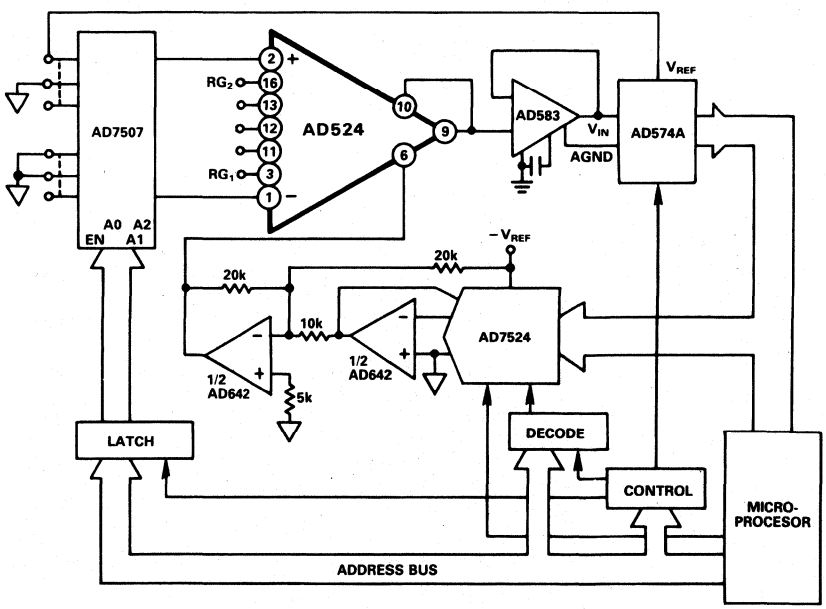


Figure 48. Microprocessor Controlled Data Acquisition System

ANALOG DEVICES

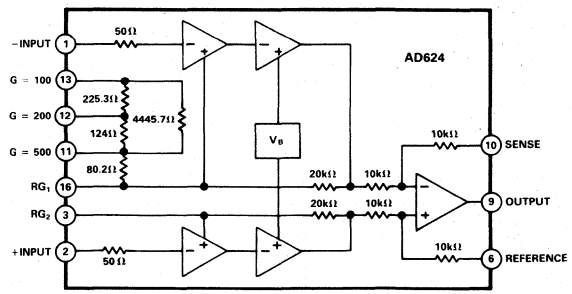
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB max (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

AD624 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD624 is a high precision low noise instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25μV/°C, output offset voltage drift of less than 10μV/°C, CMRR above 80dB at unity gain (130dB at G=500) and a maximum nonlinearity of 0.001% at G=1. In addition to these outstanding dc specifications the AD624 exhibits superior ac performance as well. A 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pre-trimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than $4nV/\sqrt{Hz}$ at 1kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pre-trimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD624A			AD624B			AD624C			AD624S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN													
Gain Equation (External Resistor Gain Programming)	$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			
Gain Range (Pin Programmable)	1 to 1000			1 to 1000			1 to 1000			1 to 1000			
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 100			±0.25			±0.15			±0.1			±0.25	%
G = 200, 500			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±1.0			±1.0			±1.0			±1.0	%
Nonlinearity													
G = 1			±0.005			±0.003			±0.001			±0.005	%
G = 100, 200			±0.005			±0.003			±0.001			±0.005	%
G = 500, 1000			±0.005			±0.005			±0.005			±0.005	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 100, 200			10			10			10			10	ppm/°C
G = 500, 1000			25			15			15			15	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			200			75			25			75	µV
vs. Temperature			2			0.5			0.25			2.0	µV/°C
Output Offset Voltage			5			3			2			3	µV
vs. Temperature			50			25			10			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	75			75			80			75			dB
G = 100, 200	95			105			110			105			dB
G = 500, 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±50			±50			±50			±50		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±20			±20			±20			±20		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_D)		±10			±10			±10			±10		V
Max Common Mode Linear (V_{CM})	$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 100, 200	100			105			110			100			dB
G = 500, 1000	110			120			130			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 100		150			150			150			150		kHz
G = 200		100			100			100			100		kHz
G = 500		50			50			50			50		kHz
G = 1000		25			25			25			25		kHz

Model	AD624A			AD624B			AD624C			AD624S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Slew Rate		5.0			5.0			5.0			5.0		V/μs
Settling Time to 0.01%, 20V Step													
G = 1 to 200		15			15			15			15		μs
G = 500		35			35			35			35		μs
G = 1000		75			75			75			75		μs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		4			4			4			4		nV/√Hz
R.T.O.		75			75			75			75		nV/√Hz
R.T.I., 0.1 to 10Hz													
G = 1		10			10			10			10		μV p-p
G = 100		0.3			0.3			0.3			0.3		μV p-p
G = 200, 500, 1000		0.2			0.2			0.2			0.2		μV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	**±5**	±15	**±18**	**±5**	±15	**±18**	**±5**	±15	**±18**	**±5**	±15	**±18**	V
Quiescent Current		3.5	**5**		3.5	5		3.5	**5**		3.5	**5**	mA
PACKAGE[1]		D16A			D16A			D16A			D16A		

NOTES

[1]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Typical Characteristics

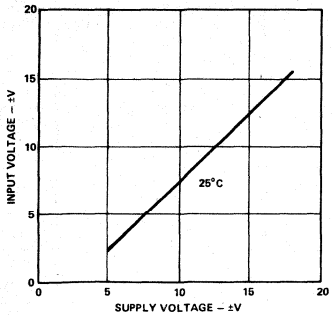


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

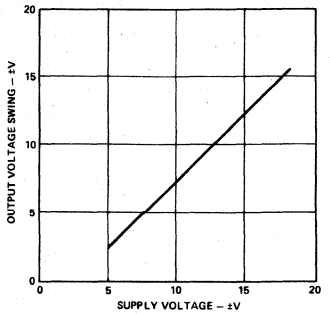


Figure 2. Output Voltage Swing vs. Supply Voltage

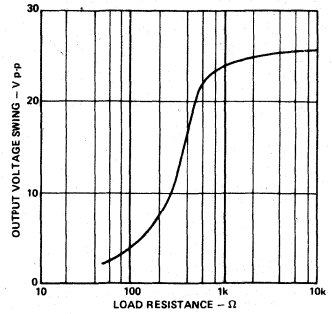


Figure 3. Output Voltage Swing vs. Resistive Load

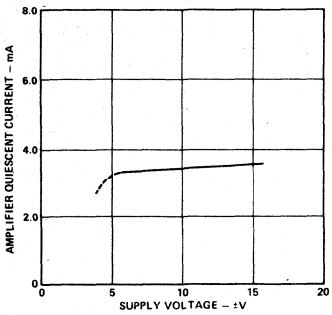


Figure 4. Quiescent Current vs. Supply Voltage

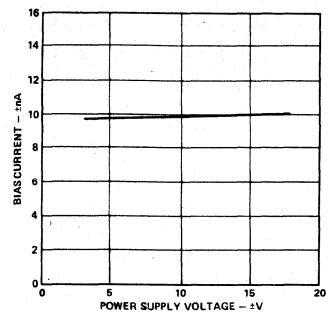


Figure 5. Input Bias Current vs. Supply Voltage

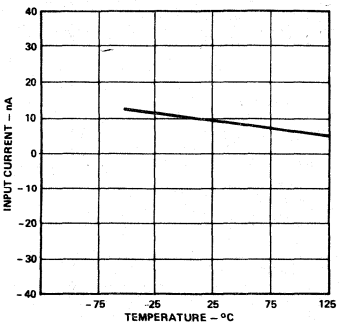


Figure 6. Input Bias Current vs. Temperature

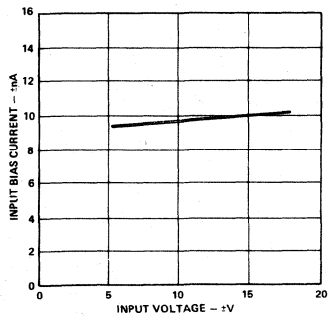


Figure 7. Input Bias Current vs. CMV

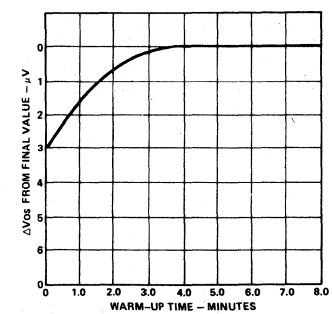


Figure 8. Offset Voltage, RTI, Turn On Drift

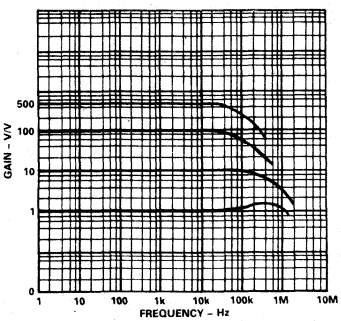


Figure 9. Gain vs. Frequency

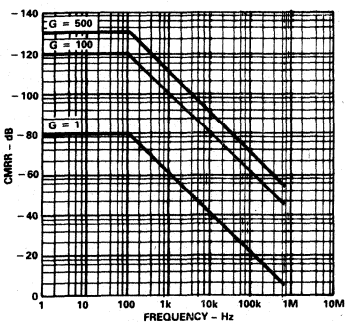


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

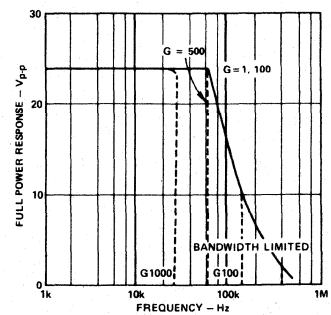


Figure 11. Large Signal Frequency Response

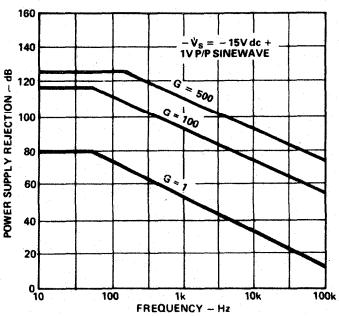


Figure 12. Positive PSRR vs. Frequency

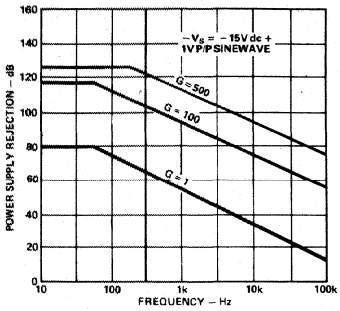


Figure 13. Negative PSRR vs. Frequency

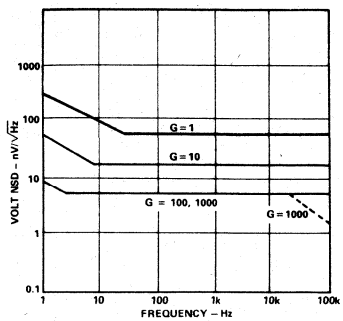


Figure 14. RTI Noise Spectral Density vs. Gain

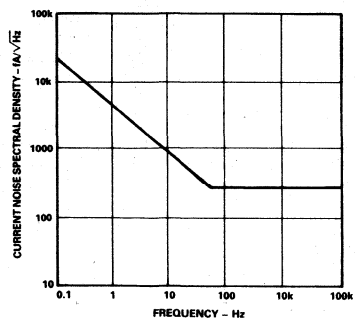


Figure 15. Input Current Noise

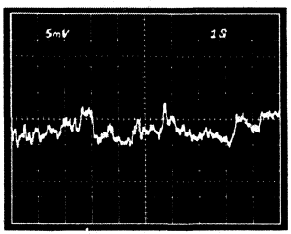


Figure 16. Low Frequency Voltage Noise – G = 1 (System Gain = 1000)

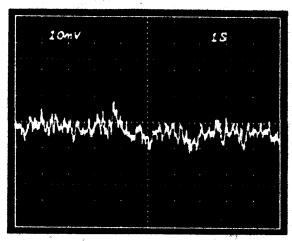


Figure 17. Low Frequency Voltage Noise – G = 1000 (System Gain = 100,000)

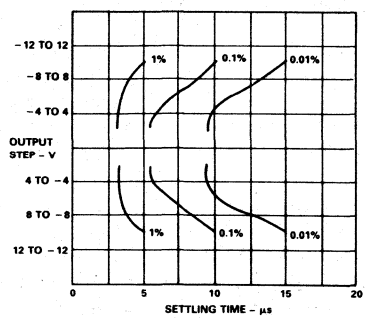


Figure 18. Settling Time Gain = 1

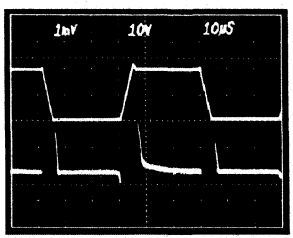


Figure 19. Large Signal Pulse Response and Settling Time – G = 1

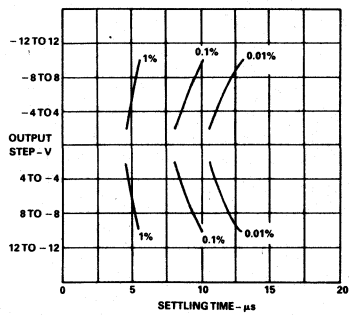


Figure 20. Settling Time Gain = 100

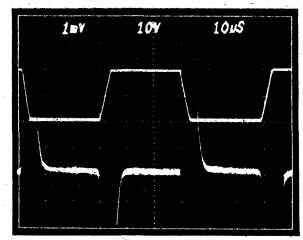


Figure 21. Large Signal Pulse Response and Settling Time G = 100

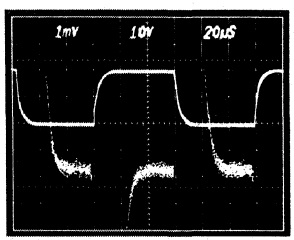


Figure 22. Range Signal Pulse Response and Settling Time G = 500

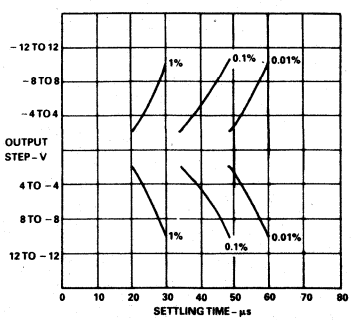


Figure 23. Settling Time Gain = 1000

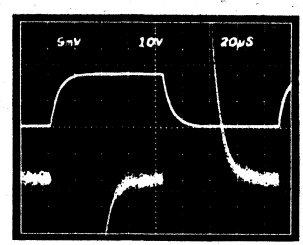


Figure 24. Large Signal Pulse Response and Settling Time G = 1000

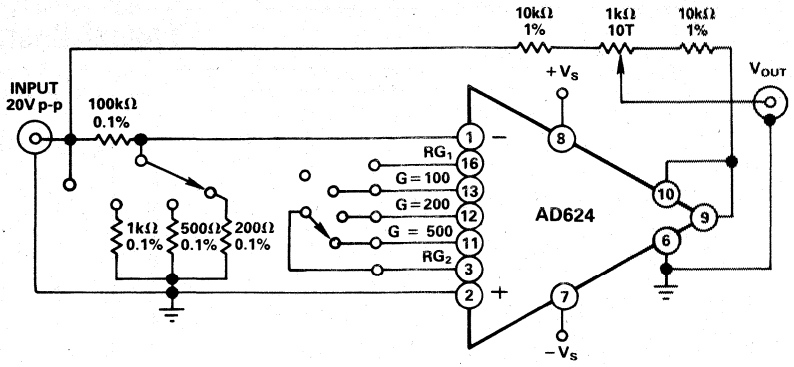


Figure 25. Settling Time Test Circuit

Theory of Operation

The AD624 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp instrumentation amplifier. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components and the high level of performance that this circuit architecture is capable of.

A preamp section (Q1–Q4) develops the programmed gain by the use of feedback concepts. Feedback from the outputs of A1 and A2 forces the collector currents of Q1–Q4 to be constant thereby impressing the input voltage across R_G.

The gain is set by choosing the value of R_G from the equation, $Gain = \frac{40k}{R_G} + 1$. The value of R_G also sets the transconductance of the input preamp stage increasing it asymptotically to the transconductance of the input transistors as R_G is reduced for larger gains. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 3ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $4nV/\sqrt{Hz}$ at G ≥ 500.

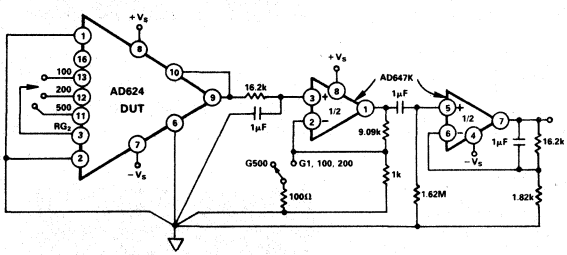


Figure 26. Noise Test Circuit

INPUT CONSIDERATIONS

Under input overload conditions the user will see $R_G + 100\Omega$ and two diode drops (~1.2V) between the plus and minus inputs, in either direction. If safe overload current under all conditions is assumed to be 10mA, the maximum overload voltage is ~ ±2.5V. While the AD624 can withstand this continuously, momentary overloads of ±10V will not harm the device. On the other hand the inputs should never exceed the supply voltage.

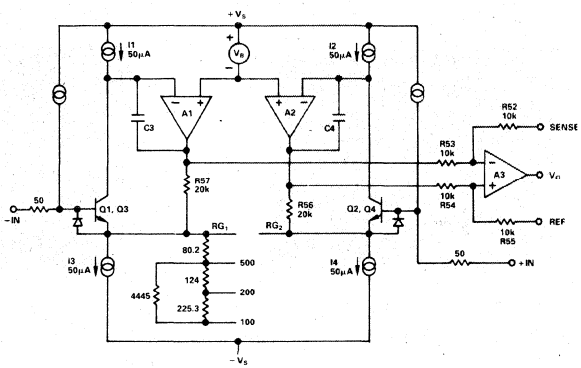


Figure 27. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit.

The AD524 should be considered in applications that require protection from severe input overload. If this is not possible, external protection resistors can be put in series with the inputs of the AD624 to augment the internal (50Ω) protection resistors. This will most seriously degrade the noise performance. For this reason the value of these resistors should be chosen to be as low as possible and still provide 10mA of current limiting under maximum continuous overload conditions. In selecting the value of these resistors, the internal gain setting resistor and the 1.2 volt drop need to be considered. For example, to protect the device from a continuous differential overload of 20V at a gain of 100, 1.9kΩ of resistance is required. The internal gain resistor is 404Ω; the internal protect resistor is 100Ω. There is a 1.2V drop across D1 or D2 and the base-emitter junction of either Q1 and Q3 or Q2 and Q4 as shown in Figure 27, 1400Ω of external resistance would be required (700Ω in series with each input). The RTI noise in this case would be $\sqrt{4KTR_{ext.} + (4nV/\sqrt{Hz})^2} = 6.2nV/\sqrt{Hz}$.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift each have two components; input and output. Input offset is that component of offset that is

directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD624 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD624 provides for both input and output offset adjustment. This optimizes nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD624 includes high accuracy pre-trimmed internal gain resistors. These allow for single connection programming of gains of 1, 100, 200 and 500. Additionally, a variety of gains including a pre-trimmed gain of 1000 can be achieved through series and parallel combinations of the internal resistors. Table I shows the available gains and the appropriate pin connections and gain temperature coefficients.

The gain values achieved via the combination of internal resistors are extremely useful. The temperature coefficient of the gain is dependent primarily on the mismatch of the temperature coefficients of the various internal resistors. Tracking of these resistors is extremely tight resulting in the low gain TC's shown in Table I.

If the desired value of gain is not attainable using the internal resistors, a single external resistor can be used to achieve any gain between 1 and 10,000. This resistor connected between

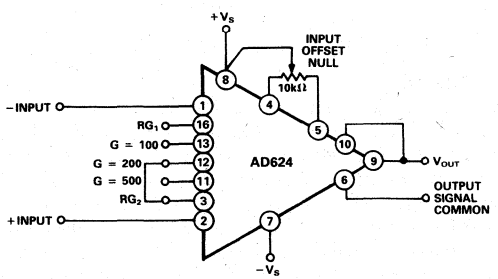


Figure 28. Operating Connections for G = 200

Gain (Nominal)	Temperature Coefficient (Nominal)	Pin 3 to Pin	Connect Pins
1	−1.5ppm/°C	–	–
100	−1.5ppm/°C	13	–
125	−5ppm/°C	13	11 to 16
137	−5.5ppm/°C	13	11 to 12
186.5	−6.5ppm/°C	13	11 to 12 to 16
200	−3.5ppm/°C	12	–
250	−5.5ppm/°C	12	11 to 13
333	−15ppm/°C	12	11 to 16
375	−0.5ppm/°C	12	13 to 16
500	−10ppm/°C	11	–
624	−5ppm/°C	11	13 to 16
688	−1.5ppm/°C	11	11 to 12; 13 to 16
831	+4ppm/°C	11	16 to 12
1000	0ppm/°C	11	16 to 12; 13 to 11

Table I.

pins 3 and 16 programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 29). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors R56 and R57. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−15ppm/°C typ), and the temperature coefficient of the internal interconnections.

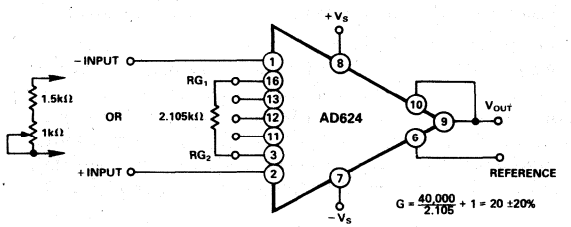


Figure 29. Operating Connections for G = 20

The AD624 may also be configured to provide gain in the output stage. Figure 30 shows an H pad attenuator connected to the reference and sense lines of the AD624. The values of R1, R2 and R3 should be selected to be as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

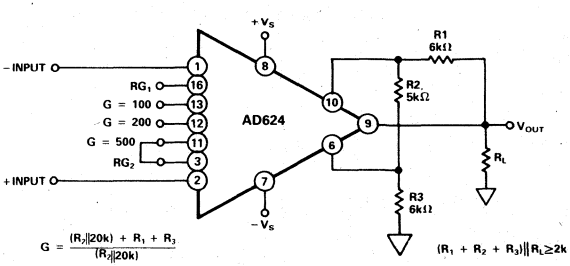


Figure 30. Gain of 2500

NOISE

The AD624 is designed to provide noise performance near the theoretical noise floor. This is an extremely important design criteria as the front end noise of an instrumentation amplifier is the ultimate limitation on the resolution of the data acquisition system it is being used in. There are two sources of noise in an instrument amplifier, the input noise, predominantly generated by the differential input stage, and the output noise, generated by the output amplifier. Both of these components are present at the input (and output) of the instrumentation amplifier. At the input, the input noise will appear unaltered; the output noise will be attenuated by the closed loop gain (at the output, the output noise will be unaltered; the input noise will be amplified by the closed loop gain). Those two noise sources must be root sum squared to determine the total noise level expected at the input (or output).

The low frequency (0.1 to 10Hz) voltage noise due to the output stage is 10μV p-p, the contribution of the input stage is 0.2μV p-p. At a gain of 10, the RTI voltage noise would be 1μV p-p, $\sqrt{\left(\frac{10}{G}\right)^2 + (0.2)^2}$. The RTO voltage noise would be 10.2μV p-p $\sqrt{10^2 + (0.2\ (G))^2}$. These calculations hold for applications using either internal or external gain resistors.

INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance imbalance appear as an additional offset voltage. (What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature.) Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source resistance.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground, (see Figure 31).

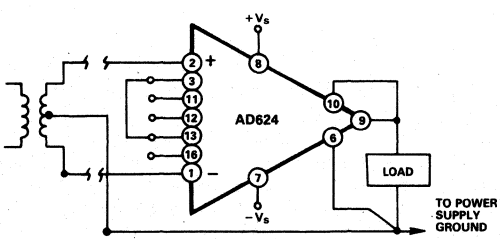


Figure 31a. Transformer Coupled

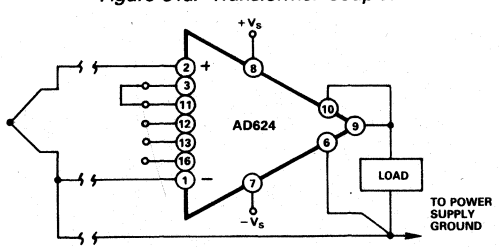


Figure 31b. Thermocouple

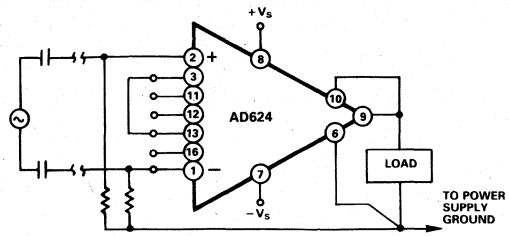


Figure 31c. AC Coupled

Figure 31. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

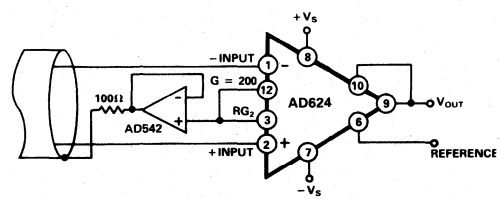


Figure 32. Shield Driver, G ≥ 100

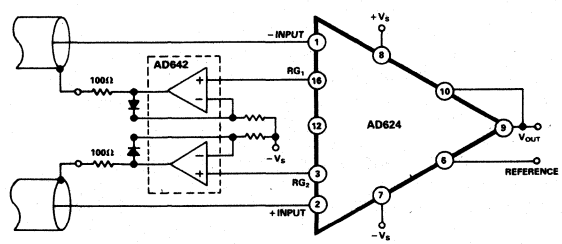


Figure 33. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to

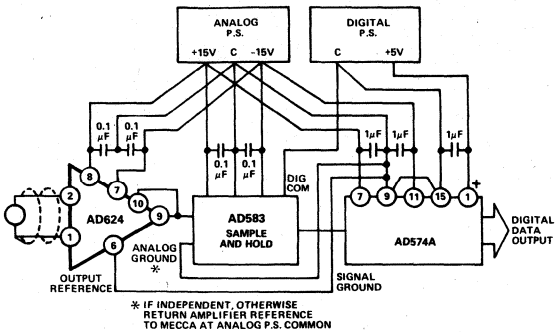


Figure 34. Basic Grounding Practice

minimize the current flow in the path from the most sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors (see Figure 34).

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

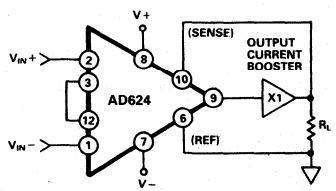


Figure 35. AD624 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ± 10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 35 shows how a current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current without significantly degrading overall performance. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ± 10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ± 10 volts, from ground, to be shared between signal and reference offset.

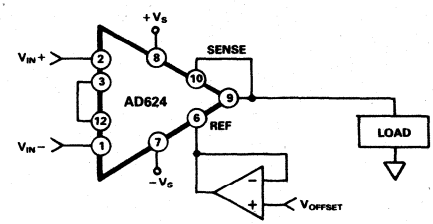


Figure 36. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance, including those caused by PC layouts or other connection techniques, which appears between the reference pin and ground will increase the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the IA. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD624 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega = 80dB$). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 36. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 37.

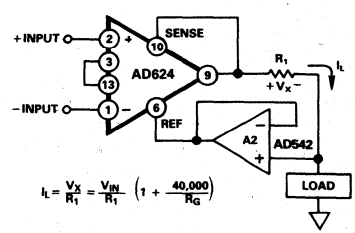


Figure 37. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 38 shows the AD624 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

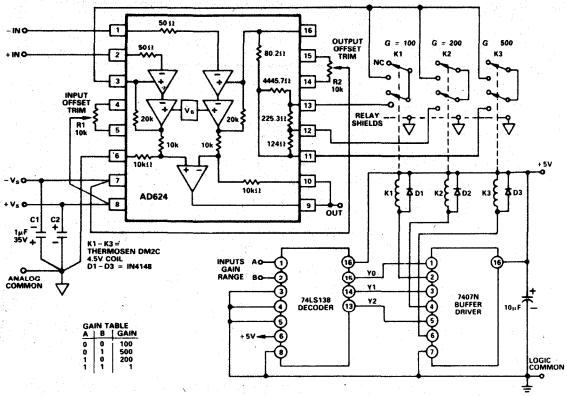


Figure 38. Gain Programmable Amplifier

A significant advantage in using the internal gain resistors in a programmable gain configuration is the minimization of thermocouple signals which are often present in multiplexed data acquisition systems.

If the full performance of the AD624 is to be achieved, the user must be extremely careful in designing and laying out his circuit to minimize the remaining thermocouple signals.

The AD624 can also be connected for gain in the output stage. Figure 39 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common-mode rejection ratio degradation.

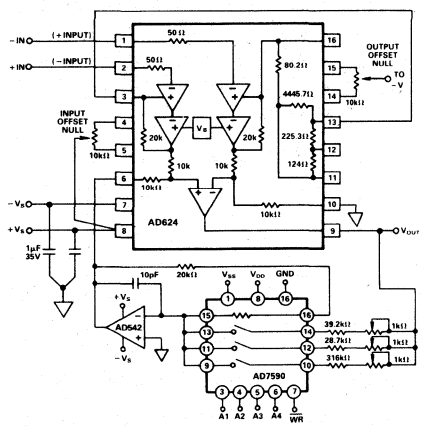


Figure 39. Programmable Output Gain

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

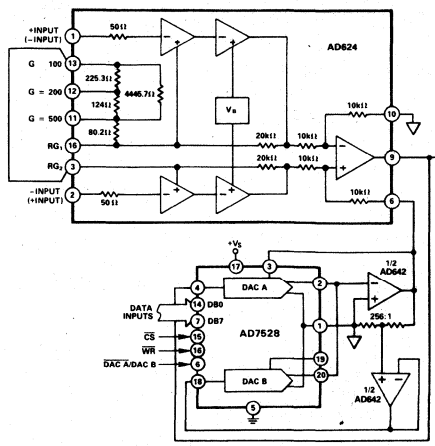


Figure 40. Programmable Output Gain Using a DAC

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 41 shows a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

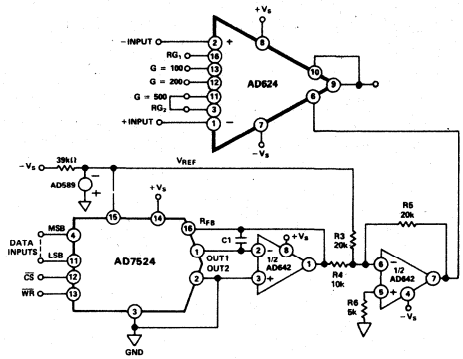


Figure 41. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For these applications Figure 42 provides a hardware solution.

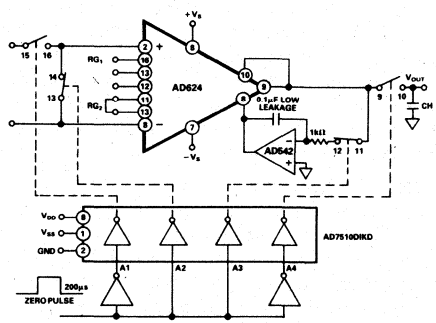


Figure 42. Auto-Zero Circuit

The microprocessor controlled data acquisition system shown in Figure 43 includes includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

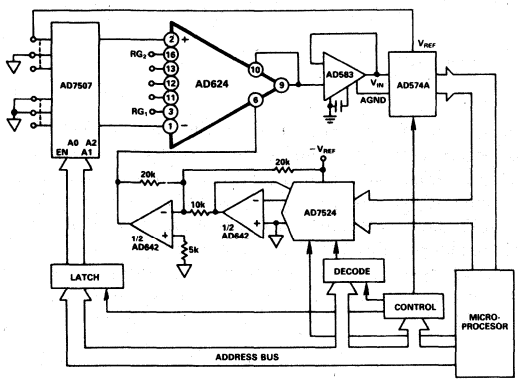


Figure 43. Microprocessor Controlled Data Acquisition System

WEIGH SCALE

Figure 44 shows an example of how an AD624 can be used to condition the differential output voltage from a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type particularly where it is desirable to measure small changes in weight as opposed to the absolute value. The addition of an auto gain/auto tare cycle will enable the system to remove offsets, gain errors, and drifts making possible true 14-bit performance.

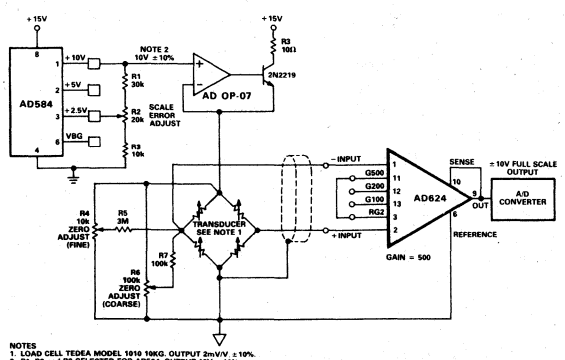


Figure 44. AD624 Weigh Scale Application

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 45 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 6.3mV change in the low pass filtered dc output, well above the RTO drifts and noise.

The AC-CMRR of the AD624 decreases with the frequency of the input signal. This is due mainly to the package-pin capacitance associated with the AD624's internal gain resistors. If AC-CMRR is not sufficient for a given application, it can be trimmed by using a variable capacitor connected to the amplifier's RG_2 pin as shown in Figure 45.

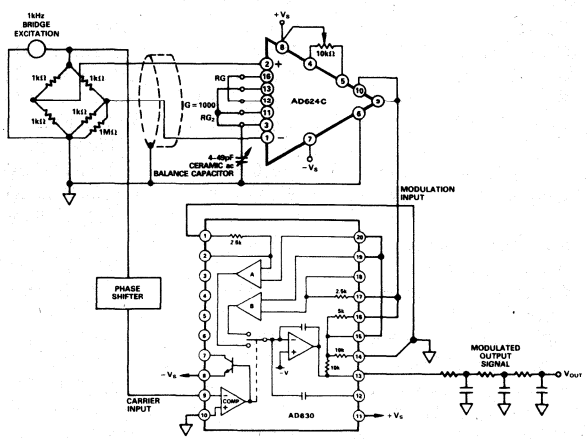


Figure 45. AC Bridge

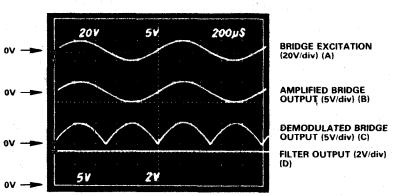


Figure 46. AC Bridge Waveforms

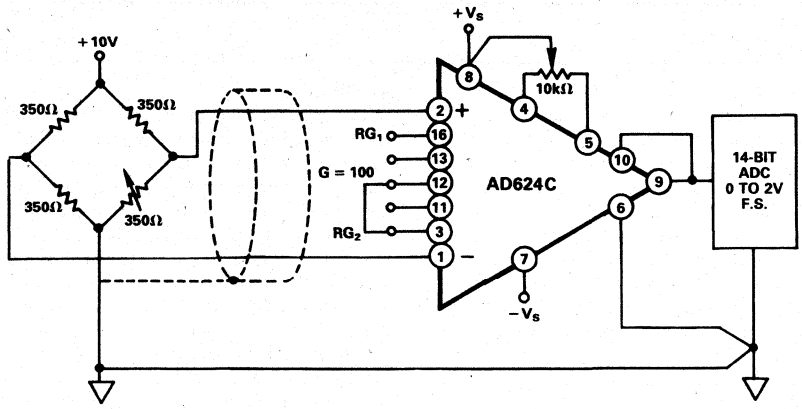


Figure 47. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer. Figure 47 shows a differential transducer, unbalanced by ≈5Ω, supplying a 0 to 20mV signal to an AD624C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (20ppm = 0.002%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.002%.

Error Source	AD624C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.1%	±0.1% = 1000ppm	1000ppm	1000ppm	–
Gain Instability	10ppm	(10ppm/°C)(60°C) = 600ppm	–	600ppm	–
Gain Nonlinearity	±0.001%	±0.001% = 10ppm	–	–	10ppm
Input Offset Voltage	±25μV, RTI	±25μV/20mV = ±1250ppm	1250ppm	1250ppm	–
Input Offset Voltage Drift	±0.25μV/°C	(±0.25μV/°C)(60°C) = 15μV 15μV/20mV = 750ppm	–	750ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±10μV/°C	(±10μV/°C)(60°C) = 600μV 600μV/20mV = 300ppm	–	300ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(5Ω) = 0.075μV 0.075μV/20mV = 3.75ppm	3.75ppm	3.75ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(5Ω) = 0.050μV 0.050μV/20mV = 2.5ppm	2.5ppm	2.5ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 9μV 9μV/20mV = 444ppm	450ppm	450ppm	–
Noise, RTI (0.1–10Hz)	0.22μV p-p	0.22μV p-p/20mV = 10ppm	–	–	10ppm
		Total Error	3793.75ppm	5493.75ppm	20ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD624CD in Bridge Application

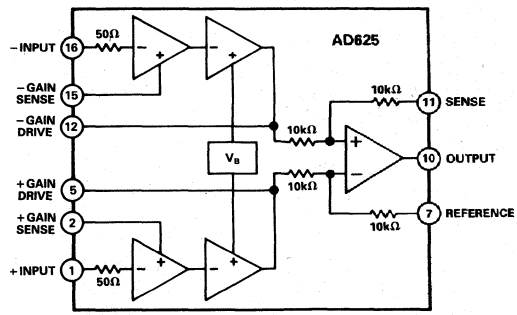
Programmable Gain Instrumentation Amplifier

AD625

FEATURES

Low Gain TC: 5ppm/°C max
Low Nonlinearity: 0.005% max
Low Noise 4nV/$\sqrt{Hz}$ (at 1kHz) RTI
Gain Bandwidth Product: 25MHz
User Programmed Gains 1 to 10,000

AD625 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier intended for use where flexible gain programmability is required. The performance of the AD625 enables its use in many applications which previously required tradeoffs between expensive external components and performance.

In resistor programmable gain applications (RPGA), as shown in Figure 2, the user can select any gain between 1 and 10,000. Gain programming is accomplished through the use of 3 external resistors. Gain accuracies and temperature coefficients are determined primarily by the match between the user provided gain setting resistors. Common-mode rejection (CMR) ranges from 70dB to 115dB minimum, for overall gains of 1 to 1000, and is independent of the feedback resistor matching.

A software programmable gain amplifier (SPGA) can be configured with the addition of a CMOS multiplexer (or other switch network), and a suitable resistor network (see Figure 3). The AD625 based SPGA can be programmed for any set of gains between 1 and 10,000, with completely user-selected gain steps.

The AD625 exhibits excellent ac performance; its 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD625 in high speed data acquisition applications.

PRODUCT HIGHLIGHTS

1. The AD625 allows user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
4. The gain accuracy and gain temperature coefficients of the amplifier circuit are primarily dependent on user selected external resistors.
5. The proprietary design of the AD625 provides the lowest input voltage noise of any resistor programmable instrumentation amplifier – 4nV/$\sqrt{Hz}$ at 1kHz.
6. The match of the two feedback resistors is not critical to maintain high common-mode rejection. This is possible because the gain sense current is insensitive to common-mode voltage.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD625A	AD625B	AD625C	AD625S
GAIN				
Gain Equation (External Resistor Gain Programming)	$2\frac{R_F}{R_G}+1$	*	*	*
Gain Range	1 to 10000	*	*	*
Gain Error, Max	±0.05%	±0.03%	±0.02%	*
Nonlinearity, max	±0.005%	±0.003%	±0.001%	*
Gain vs. Temperature, max	5ppm/°C	*	*	*
VOLTAGE OFFSET (May be Nulled)				
Input Offset Voltage, max	200μV	75μV	25μV	**
vs. Temperature, max	2μV/°C	0.5μV/°C	0.25μV/°C	2μV/°C
Output Offset Voltage, max	5mV	3mV	2mV	**
vs. Temperature, max	50μV/°C	25μV/°C	10μV/°C	50μV/°C
Offset Referred to the Input vs. Supply				
G = 1	70dB	75dB	80dB	**
G = 10	85dB	105dB	110dB	**
G = 100	95dB	105dB	110dB	**
G = 1000	100dB	110dB	115dB	**
INPUT CURRENT				
Input Bias Current, max	±50nA	±25nA	±15nA	*
vs. Temperature	±50pA/°C	*	*	*
Input Offset Current, max	±35nA	±15nA	±10nA	*
vs. Temperature	±20pA/°C	*	*	*
INPUT				
Input Voltage Range				
Max Differ. Input Linear (V_D)	±10V	*	*	*
Max Common Mode Linear (V_{CM})	$12V-\left(\frac{G}{2}\times V_D\right)$	*	*	*
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance, min				
G = 1	70dB	75dB	80dB	*
G = 10	90dB	105dB	110dB	*
G = 100	100dB	105dB	110dB	*
G = 1000	110dB	120dB	130dB	*
OUTPUT RATING	±10V @ 5mA	*	*	*
DYNAMIC RESPONSE				
Small Signal −3dB				
G = 1	650kHz	*	*	*
G = 10	400kHz	*	*	*
G = 100	100kHz	*	*	*
G = 1000	25kHz	*	*	*
Slew Rate	5.0V/μs	*	*	*
Settling Time to 0.01%, 20V Step				
G = 1 to 200	15μs	*	*	*
G = 500	35μs	*	*	*
G = 1000	75μs	*	*	*
NOISE				
Voltage Noise, 1kHz				
R.T.I.	$4nV/\sqrt{Hz}$	*	*	*
R.T.O.	$75nV/\sqrt{Hz}$	*	*	*
R.T.I., 0.1 to 10Hz				
G = 1	10μV p-p	*	*	*
G = 10	1.0μV p-p	*	*	*
G = 100	0.3μV p-p	*	*	*
G = 1000	0.2μV p-p	*	*	*
Current Noise				
0.1Hz to 10Hz	60pA p-p	*	*	*

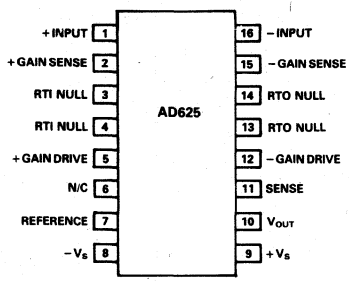
Model	AD625A	AD625B	AD625C	AD625S
TEMPERATURE RANGE				
Specified Performance	−25°C to +85°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
POWER SUPPLY				
Power Supply Range	±5V to ±18V	*	*	*
Quiescent Current	3.5mA (5mA max)	*	*	*
Gain Sense Current, max	500nA	250nA	100nA	*
Gain Sense Current vs. Temperature, max	25nA/°C	15nA/°C	10nA/°C	*
Gain Sense Offset Current	500nA	250nA	100nA	*
Gain Sense Offset Current vs. Temperature	20nA/°C	10nA/°C	5nA/°C	*
PACKAGE OPTION[1]	D16A AD625AD	D16A AD625BD	D16A AD625CD	D16A AD625SD

NOTES
*Specifications same as AD625A.
**Specifications same as AD625B.

[1]See Section 19 for package outline information.
Specifications subject to change without notice.

5

PIN CONFIGURATION



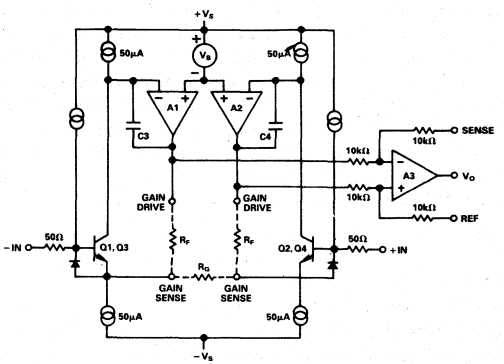


Figure 1. Simplified Circuit of Amplifier

Theory of Operation

The AD625 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture. A preamp section (Q1-Q4) provides additional gain to A1 and A2, which increases the overall transconductance of the input stage. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant thereby impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain $\left(\frac{2R_F}{R_G} + 1\right)$ times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_O, referred to the reference potential.

The value of R_G is the determining factor of the transconductance of the input preamp stage. As R_G is reduced for larger gains the transconductance increases. This has three important advantages. First, the approach allows the circuit to achieve a very high open-loop gain of 3×10^8 at programmed gains ≥ 500 thus reducing gain related errors. Second, the gain-bandwidth product, which is determined by C3, C4, and the input transconductance, increases with gain, thereby optimizing frequency response. Third, the input voltage noise is reduced to a value determined by the collector current of the input transistors resulting in an RTI noise of $4nV/\sqrt{Hz}$.

RESISTOR PROGRAMMABLE GAIN AMPLIFIER

In the resistor-programmed mode (see Figure 2) only three external resistors are needed to select any gain from 1 to 10,000. Depending on the application, discrete components or a pre-trimmed network can be used. The gain accuracy and gain TC are primarily determined by the external resistors since the AD625 typically contributes less than 0.02% to gain error and under 5ppm/°C gain TC. The gain sense current is insensitive to common-mode voltage, making the CMRR of the resistor programmed AD625 independent of the match of the two feedback resistors (R_F).

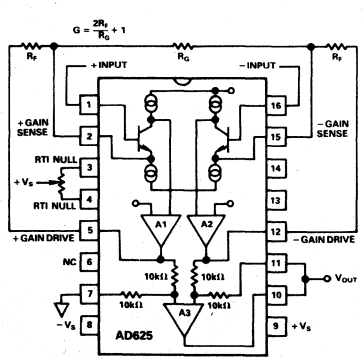


Figure 2. AD625 in Fixed Gain Configuration

Selecting Resistor Values

As previously stated each R_F provides feedback to the input stage and sets the unity gain transconductance. These feedback resistors are provided by the user. The AD625 is tested and specified with a value of 20kΩ for R_F. In the unity gain configuration R_F should be 20kΩ; for gains > 1 R_F can be in the range of 10kΩ to 30kΩ. The gain resistor (R_G) is determined by the formula $R_G = \frac{2R_S}{G-1}$

For single gain applications, only one offset null adjust is necessary; in these cases the RTI null should be used.

SOFTWARE PROGRAMMABLE GAIN AMPLIFIER

An SPGA provides the user the abiliy to externally program precision gains from digital inputs. To date, the problem in systems requiring electronic switching of gains has been the ON resistance (R_{ON}) of the multiplexer, which appears in series with the gain setting resistor R_G. This can result in substantial gain errors and gain drifts. The AD625 eliminates this problem by making the gain drive and gain sense pins available (Pins 2, 15, 5, 12; see Figure 4). Consequently the multiplexer's ON resistance is removed from the signal current path. This transforms the ON resistance error into a small nullable offset voltage error. To clarify this point, an error budget analysis has been performed in Table I. Figure 4 shows the AD625 based SPGA used for the analysis in Table I. The output of the AD625 feeds a 12-bit DAS with a 0-10V input voltage range. The gain used for the RTI calculations is set at 16; as the gain is changed, the ON resistance of the multiplexer and the feedback resistance will change, which will change the values in the table.

Figure 3 shows an SPGA at a gain of 16. To determine the gain, it is necessary to calculate R_G and R_F. R_G equals the resistance between the gain sense lines (Pins 2 and 15) of the AD625. In Figure 3, R_G equals the sum of the two 975Ω resistors and the 650Ω resistor, therefore, R_G equals 2600Ω. R_F equals the resistance between the gain sense and gain drive pins (Pins 12 and 15, or Pins 2 and 5). In Figure 3, R_F equals the 15.6kΩ resistor plus the 3.9kΩ resistor, or R_F equals 19.5kΩ. The gain equals:

$$\frac{2R_F}{R_G} + 1 = 2\frac{(19.5k\Omega)}{(2.6k\Omega)} + 1 = 16$$

As the switches of the differential multiplexer proceed synchronously, R_G and R_F change, resulting in the various programmed gain settings.

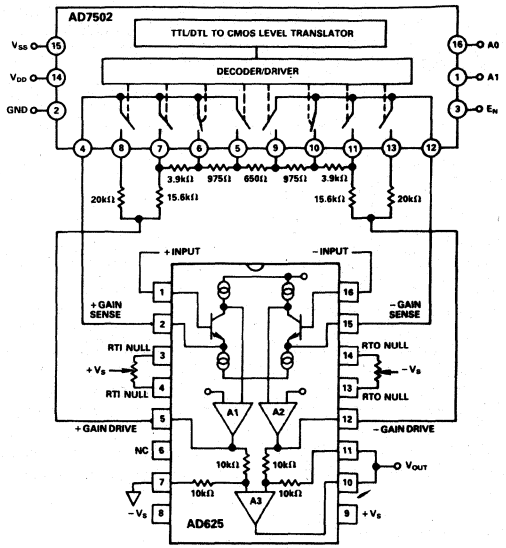


Figure 3. SPGA in a Gain of 16

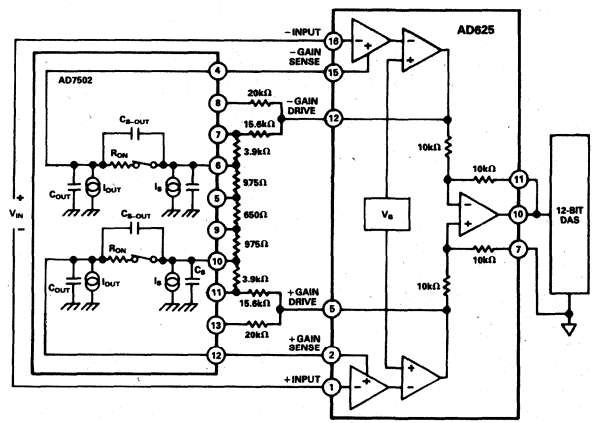


Figure 4. SPGA with Multiplexer Error Sources

Induced Error	Specification AD625	Specification AD7502	Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Offset Current 150nA	Switch Resistance 170Ω	150nA × 170Ω = 25.5μV	25.5μV
RTI Offset Voltage	Gain Sense Current 300nA	Differential Switch Resistance 6.8Ω	300nA × 6.8Ω = 2.04μV	2.04μV
RTO Offset Voltage	Feedback Resistance[1] 20kΩ	Differential Leakage Current (I_S)[2] +0.2nA −02nA	2(0.2nA × 20kΩ) = 8μV	0.5μV
RTO Offset Voltage	Feedback Resistance[1] 20kΩ	Differential Leakage Current (I_{OUT})[2] + 1nA − 1nA	2(1nA × 20kΩ) = 40μV	2.5μV

NOTES

[1]The resistor for this calculation is the user provided feedback resistance (R_F), 20kΩ is recommended (see resistor programmable gain amplifier section)

[2]The leakage currents (I_S and I_{OUT}) will induce an offset voltage, however, the offset will be determined by the difference between the leakages of each "half" of the differential multiplexer. The differential leakage current is multiplied by the feedback resistance (see Note 1), to determine offset voltage. Because differential leakage curent is not a parameter specified on multiplexer data sheets, the most extreme difference (one most positive and one most negative) was used for the calculation in Table I. Typical performance will be much better.

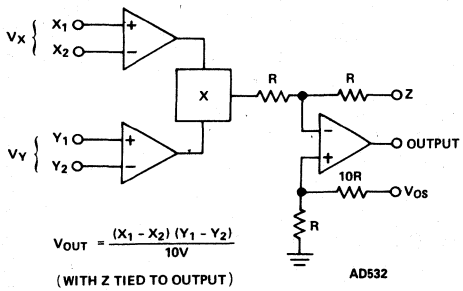
Table I. Errors Induced by Multiplexer to an SPGA

Analog Signal Processing Components

Contents

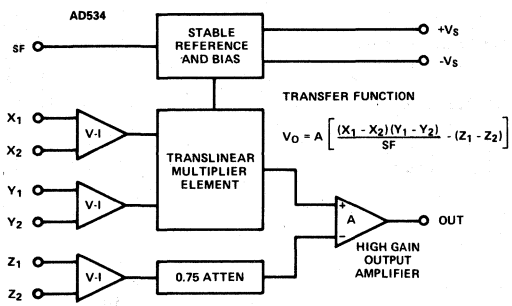
Selection Guide
Analog Signal Processing Components

Internally Trimmed Multipliers



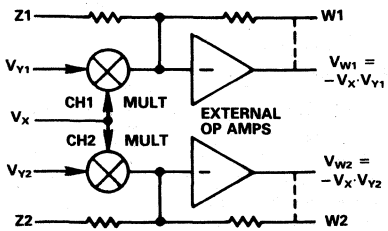
AD532

Pretrimmed to ±1.0% (AD532K)
No External Components Required
Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
Diff Inputs for $(X_1-X_2)(Y_1-Y_2)/10$ Transfer Function
Monolithic Construction



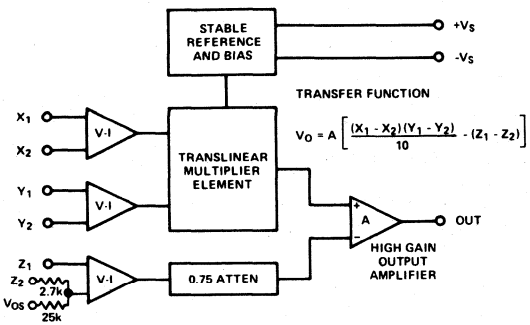
AD534

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V] + Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz–10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability



AD539

Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control-Bandwidth of 5MHz
Full-Calibrated, Monolithic Circuit

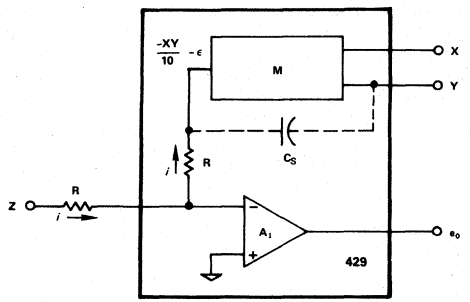


AD632

Pretrimmed to ±0.5% max 4-Quadrant Error
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1 - X_2)(Y_1 - Y_2)/10V] + Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X10 Gain
Low Noise Design: 90μV rms, 10Hz–10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

Selection Guide
Analog Signal Processing Components

Internally Trimmed Multipliers

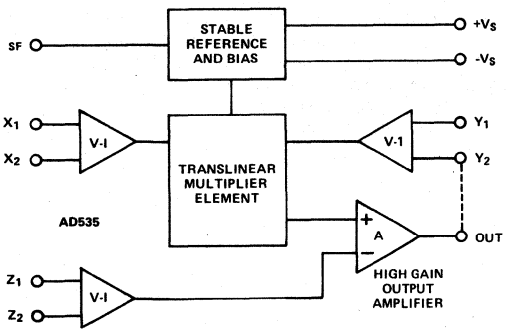


MODEL 429

Page

1.0%/0.5% Accuracy Without Trimming (429A/B) Vol. II
Low Drift to 1.0mV/°C max 6-9
Wideband – 10MHz
0.2% Nonlinearity max (429B)
External Amplifiers not Required
MTBF: 169, 268 Hours

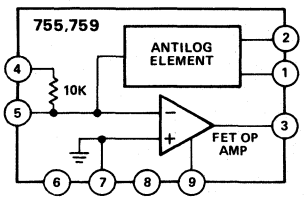
Internally Trimmed Dividers



AD535

Pretrimmed to ±0.5% max Error, 10:1 Denominator Range (AD535K) Vol. I
±2.0% max Error, 50:1 Denominator Range (AD535K) 6-37
All Inputs (X, Y and Z) Differential
Monolithic Construction

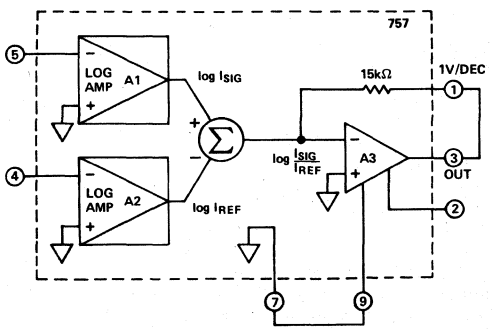
Log-Antilog Amplifiers



MODEL 755, MODEL 759

Vol. II 8-7

High Accuracy: Models 755N, 755P
Low Cost: Models 759N, 759P
Complete Log-Antilog Amplifiers: External Components not Required
Temperature-Compensated Internal Reference
6 Decades Current Operation: 1nA to 1mA
1% max Error: 1nA to 1mA (755)
20nA to 200μA (759)
4 Decades Current Operation: 1mV to 10V
1% max Error: 1mV to 10V (755)
1mV to 2V (759)



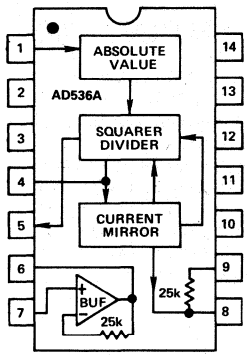
MODEL 757

Vol. II 8-11

6 Decade Operation – 1nA to 1mA
1/2% Log Conformity – 10nA to 100μA
Symmetrical FET Inputs
Voltage or Current Operation
Temperature Compensated
Complete Log Ratio Amplifier: External Components not Required

Selection Guide
Analog Signal Processing Components

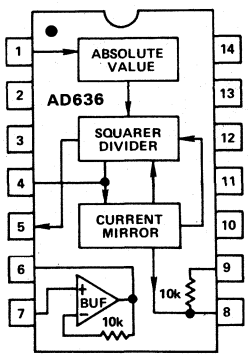
RMS-to-DC Converters



AD536A

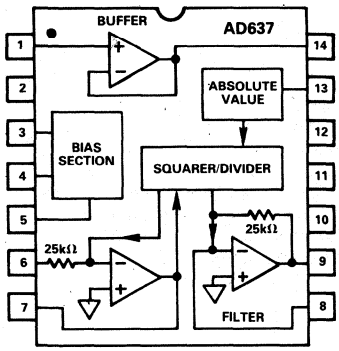
Page

- True rms-to-dc Conversion — Vol. I 6-43
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 300kHz Bandwidth: V_{rms}>100mV
  - 2MHz Bandwidth: V_{rms}>1V
  - Signal Crest Factor 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- −55°C to +125°C Operation (AD536AS)



AD636

- True rms-to-dc Conversion — Vol. I 6-71
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz −3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit



AD637

Page
Vol. I
6-77

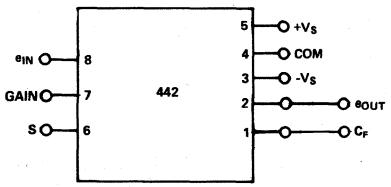
High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V rms Input**
- **0.10% Max Error to Crest Factor of 3**

Wide Bandwidth
- **8MHz at 2V rms Input**
- **600kHz at 100mV rms**

Computes:
- **True rms**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (−60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiescent Current Reduction from 2.2mA to 350μA**



MODEL 442

Vol. II
7-7

DC to 8MHz Response (−3dB)

High Accuracy:
- **With No Ext. Trim: ±2mV ±0.15% of Rdg., max**
- **With Ext. Trim: ±1mV ±0.05% of Rdg., max**

Low Drift: ±(35μV ±0.01% of Reading)/°C max, 442L

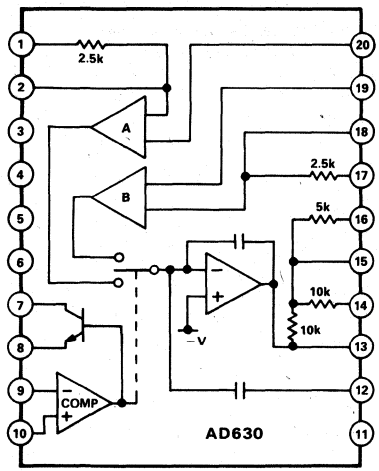
Fast Settling Time: 5ms to 1%

All Hermetically Sealed Semiconductors

No External Components Required to Meet Specifications

Selection Guide
Analog Signal Processing Components

Modulator/Demodulator



AD630

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth

Orientation
Analog Signal Processing Components

MULTIPLIERS/DIVIDERS

Multiplication For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_xV_y/E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If E_{ref} = 10V, E_{out} = 10V when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement, and mathematical operations in analog computing, curve fitting, and linearizing.

If the inputs may be of either positive or negative polarity, and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the 4 quadrants of the X-Y plane.

Squaring If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2/E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive, whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads, and mathematical operations.

Division For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If E_{ref} = 10V, E_{out} will be 10V or less for $V_z \leqslant V_x$. V_x is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios—such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements, and for mathematical operations in analog computing.

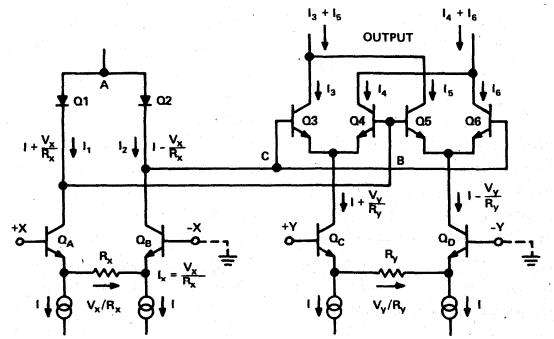
Square rooting For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref}V_{in}}$. A square-rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, etc.

A number of devices are listed here, differing in internal architecture, external functional configuration, device technology, and performance specifications. Some have essentially fixed references; others have an actively variable or programmable reference as a third input (*multifunction devices*), and one type (model 433) performs the one-quadrant operation, $E_o = V_z(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5. With one exception (model 436 precision 2-quadrant divider), all of the devices listed here can be used for any of the functions defined above.

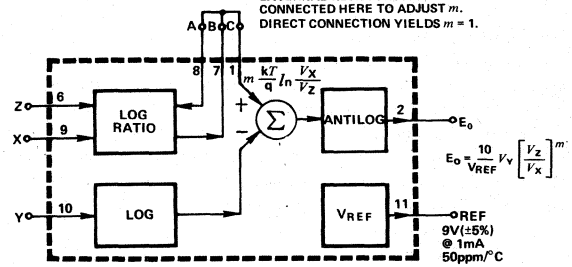
Considerable information on these functions, the nature of devices to perform them, and extensive discussions of their applications can be found in two publications available from Analog Devices.[1,2] A wealth of information is also to be found in the data sheets for the individual devices, published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture All of the devices in this selection rely on the logarithmic properties of silicon P-N junctions. With the exception of models 433 and 436, the circuit employed is basically like that of the "Gilbert cell" (its 4-quadrant-multiplying circuitry and performance are described in (1) and (2), with further references to original sources). The input voltages are converted to currents, the currents are multiplied together and divided by a reference, and the net output current, I_xI_y/I_{ref}, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division. In the AD531[3], the I_{ref} terminals are available for external programming or variation; thus, the AD531 is a 3-variable "multifunction" IC which can divide without external feedback. This versatile feature offers greater bandwidth as a divider.



Basic 4-Quadrant Variable-Transconductance Multiplier Circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2\,V_X\,V_Y}{I\,R_X\,R_Y}$$



Functional Block Diagram of Model 433

In multifunction devices like Model 433, the feedback currents of the input op amps are used to develop logarithmic

[1] *Multiplier Application Guide*, available upon request

[2] *Nonlinear Circuits Handbook*, D. H. Sheingold, ed., 1976, 536pp., $5.95, P.O. Box 796, Norwood MA 02062

[3] Data sheet available upon request.

voltages across transistor base-emitter junctions; these voltages are summed and differenced and produce an exponential current proportional to V_yV_z/V_x via another transistor junction in the input path of the output amplifier. Thus, the output voltage is proportional to V_yV_z/V_x; an internally generated reference voltage is available as a fixed reference for the odd input in two-variable operations. In the 433, the internal emitter-voltage difference proportional to log (V_z/V_x) can be amplified or attenuated by the appropriate connection of a resistive attenuator with an attenuation ratio, m; since the antilog of m(log V_z/V_x) is $(V_z/V_x)^m$, the output of the 433 is proportional to $V_y(V_z/V_x)^m$. In the model 436 divider, the inputs are scaled and linearly combined, before the log-antilog computation takes place; the result is that the numerator (of V_z/V_x) may have positive or negative values. The 436 circuit is optimized and trimmed for performance as a dedicated divider; it has a fixed reference. Its circuit principles are discussed in some detail on the data sheet.

External functional configuration As noted earlier, with the exception of the model 436 dedicated divider, all of the devices listed here can be used for multiplication, division, squaring, and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. As an example, the AD534 is shown connected for multiplication, and the AD535, which has similar architecture but is optimized for division, is shown connected for division and square-rooting. Performance of pretrimmed devices is optimized in specified modes of operation, usually multiplication. The data sheets show how devices are connected for the various modes of operation; where appropriate, the trim circuits and procedures for optimizing performance are provided.

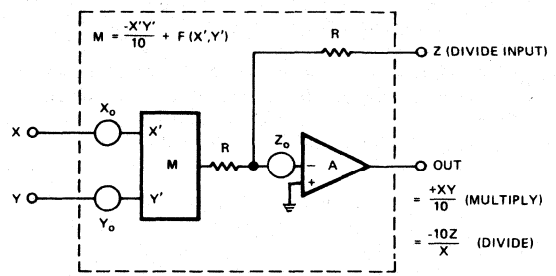
Some devices have differential inputs, which provide a great deal of flexibility. They permit polarity changes without external inversion, direct subtraction of inputs, insertion of bias voltages for additive constants, and direct multiplication of the results of differential measurements.

Technologies The devices described here are either monolithic integrated circuits or high-performance modules. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The modules provide the highest performance: speed (model 429), accuracy as a divider (436), and accuracy in multifunction applications (433). On the other hand, the IC's provide economy of cost and space, and the availability of "mil-temp" range (-55°C to +125°C) versions. The pretrimmed IC's (AD534, AD535 and AD532) use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors to 0.25%, and linearities as yet unmatched in the industry.

Performance Multiplier performance, specifications and test circuitry are described in great detail in the NONLINEAR CIRCUITS HANDBOOK. Here is a brief digest of the factors relating to low-frequency performance.

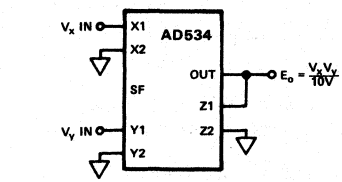
In theory, a multiplier has an output which is ideally the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities, which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practice (see the figure), the multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is the gain-conditioning op amp, A.

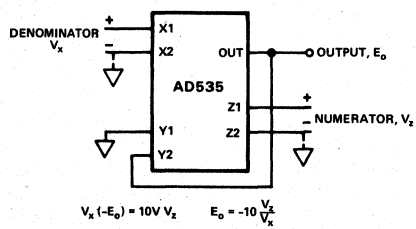


Functional Block Diagram of Typical Multiplier/Divider

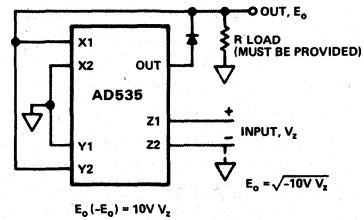
Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model used for considering errors. X_o and Y_o are input offset voltages, Z_o is the offset-referred-to-the-input of the output amplifier, and $F(X', Y')$ is the nonlinearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form



Multiplier



Divider



Square Rooter

$$E_o = \frac{XY}{10B} \pm \left[\frac{X_o Y}{10B} \pm \frac{XY_o}{10B} \pm Z_o + f(X,Y)\right]$$

Product: X_{offset} Y_{offset} — Output offset — Nonlinearity and feedthrough

Linear "Y" — Feedthrough "X"

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by applying external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x|\,\epsilon_x + |V_y|\,\epsilon_y$$

were ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_y are the input signals.

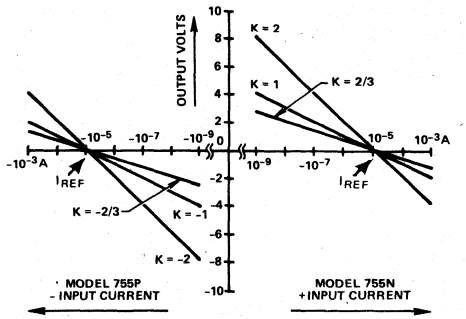
When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (e.g., 10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of X.

LOGS AND LOG RATIOS

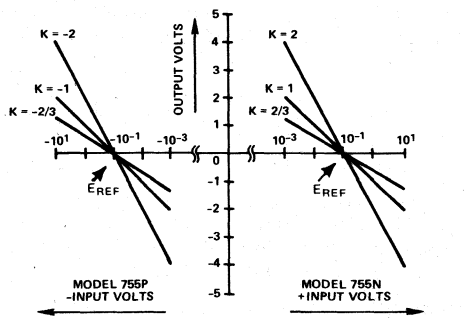
In the *logarithmic* mode, the ideal output equation is

$$E_o = -K \log_{10}\left(\frac{I_{in}}{I_{ref}}\right)$$

E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin-programmable to be either 1V, 2V, or 2/3V, or externally adjustable to any value ≥ 2/3V; in the model 757 log-



Log of Current



Log of Voltage

Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

ratio amplifier, K may be either a preset value of 1V, or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted; but model 757 is a *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive*; "P" indicates that

*A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1000 (3 decades), the output would change by 6V.

only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 755N, with K = +1V, would produce an output voltage, E_o = -1V log (100) = -2V; on the other hand, -10V applied to model 755P, with K = 1V, would produce an output voltage, E_o = -(-1V) log (100) = +2V. The figure shows, in condensed form, the outputs of P and N log-amps, with differing K values, for voltage and current inputs.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs, and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

$$E_o = E_{ref} \exp_{10} (-E_{in}/K)$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = -2V, if E_{in} = +4V, and E_{ref} = -0.1V, then

$E_o = -0.1V \cdot 10^{-4/-2}$, or -10V; if E_{in} = -4V, then

$E_o = -0.1V \cdot 10^{-(-4)/-2} = -1mV$. The figure below shows, in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

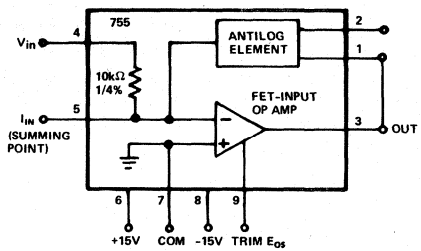
Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.

LOG-ANTILOG AMPLIFIER PERFORMANCE

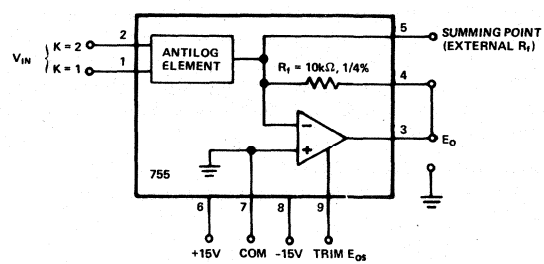
Considerable information regarding log- and antilog-amplifier circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK[1]. Several salient points will be covered here, and specifications will be defined.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

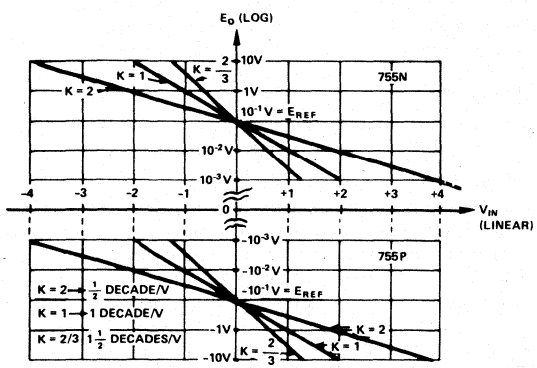
In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)



b) Log/Antilog Amplifier Connected in the Exponential Mode



Antilog Operator Response Curves, Semilog Scale
$E_o = E_{REF}\ 10^{V_{IN}/-K}$

[1] *Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood MA 02062

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

$$I = I_o(\epsilon^{qV/kT} - 1) \cong I_o\epsilon^{qV/kT}$$

and $V = (kT/q) \ln (I/I_o)$

where I is the collector current, I_o is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11605° K/V) is the ratio of charge of an electron to Boltzmann's constant, and T is junction temperature kelvin. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_o's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q) \ln (I_{in}/I_o) - (kT/q) \ln (I_{ref}/I_o) \\ &= (kT/q) (\ln I_{in} - \ln I_{ref}) + (kT/q) (\ln I_o - \ln I_o) \\ &= (kT/q) \ln (I_{in}/I_{ref})\end{aligned}$$

The temperature-dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade (kT/q) ln10 at room temperature) to 1V/decade.

Errors are introduced by the offset current of the amplifier, and the offset voltage, for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog paper. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at whatever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output} \\ &= 1V \cdot \log (1.01\ I/I_{ref}) - 1V \cdot \log (I/I_{ref}) \\ &= 1V \cdot \log 1.01 = 0.0043V = 4.3mV\end{aligned}$$

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17.	5.7
3.0	13.	26.	8.6
4.0	17.	34.	11.
5.0	21.	42.	14.
10.0	41.	83.	28.

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction — step changes in the direction of increasing current are responded to more quickly than step decreases of current.

RMS-TO-DC CONVERTERS

The accurate calculation of the root-mean-square of an ac waveform has long been a stumbling block to designers of ac measurement and control instrumentation. Historically, this problem has been addressed by various, each method tailored to the specific application. The rms of ac signals is important because it is a measure of the power in that signal.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of (i.e., full-wave or half-wave rectifying) a signal, filtering it, and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform and will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

Examples of applications include noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True-rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

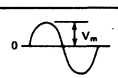
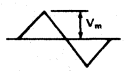
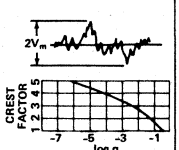
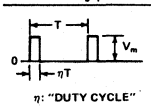
True-rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise, and acoustical noise. The electrical signals produced by these mechanical actions are often noisy, non-periodic, nonsinusoidal, and superimposed on dc levels, and require true-rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms is to take the absolute value, square it, and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_o = \text{Avg.}\left[\frac{V_{in}^2}{E_o}\right] \cong \sqrt{\text{Avg.}\,(V_{in}^2)}$$

is valid if the averaging time-constant is sufficiently long compared with the periods of the lowest-frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter, using an external filtering capacitance. Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, the data sheets show how an additional stage of 2-pole filtering is useful. The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{ext}.

WAVEFORM		RMS	MAD	RMS / MAD	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0.707 V_m	$\frac{2}{\pi} V_m$ 0.637 V_m	$\frac{\pi}{2\sqrt{2}}$ = 1.111	$\sqrt{2}$ = 1.414
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}}$ = 1.155	$\sqrt{3}$ = 1.732
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2x10⁻⁹
	PULSE TRAIN η: "DUTY CYCLE"	$V_m\sqrt{\eta}$	$V_m\eta$	$\frac{1}{\sqrt{\eta}}$	$\frac{1}{\sqrt{\eta}}$

η	MARK/SPACE	RMS	MAD	RMS / MAD	CREST FACTOR
1	∞	V_m	V_m	1	1
0.25	0.3333	$0.5V_m$	$0.25V_m$	2	2
0.0625	0.0667	$0.25V_m$	$0.0625V_m$	4	4
0.0156	0.0159	$0.125V_m$	$0.0156V_m$	8	8
0.01	0.0101	$0.1V_m$	$0.01V_m$	10	10

MODULATION/DEMODULATION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecutre with accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication.

Often in physical processes, it is necessary to determine the amplitude of a very small signal whose phase and frequency is known. In addition, the signal may be masked by broadband noise or dc interference. Some specific instances where this type of signal detection is required include sonar reception, LVDT demodulation, inductive or capacitive bridges, chopped photodetectors, and resistive bridges where a large amount of dc interference exists. The AD630 can extract these tiny signals from the background noise by switching between positive and negative gain each half cycle. This synchronous gain switching rectifies the signal of interest and produces a dc output proportional to the signal amplitude. Other signal components that are of a different frequency (including dc offset) are chopped to an ac frequency that can be filtered out with a simple low pass filter.

DEFINITIONS OF SPECIFICATIONS

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Crest Factor (a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case – rectangular pulse – input signal.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error,* and *settling time.*

Full-power response is the maximum frequency at which the multiplier can produce full-scale voltage into its rated load without noticeable distortion.

Settling time. for the product of a ±10V step and 10Vdc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Slew(ing) rate is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

Small-signal amplitude error is defined in relation to the frequency at which the amplitude response, or scale factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Small-signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

Vector error is the most-sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.

Filter Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for ±3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal 30% of reading. It is a function of amplitude.

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

Log-Conformity Error When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the multiplier may improve small-signal resolution significantly.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Power Supply: Power-supply range for specified performance, power-supply range for operation, and quiescent current drain. Note that the AD536 can be operated from single or dual supplies.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements ($T_H - 25^\circ C$), ($25^\circ C - T_L$), when measured.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

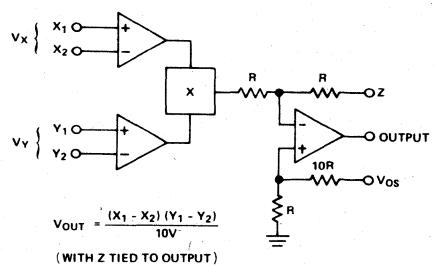
Internally Trimmed Integrated Circuit Multiplier

AD532

FEATURES
- Pretrimmed To ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs For (X_1-X_2) $(Y_1-Y_2)/10V$ Transfer Function
- Monolithic Construction, Low Cost

APPLICATIONS
- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications

AD532 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

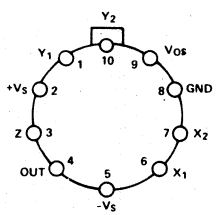
FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10V$, divides in two quadrants with a $10VZ/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10VZ}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as $XY/10V$, $(X^2-Y^2)/10V$, $\pm X^2/10V$, and $10VZ/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

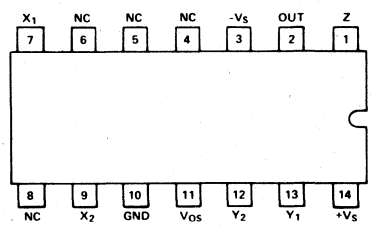
The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of −55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP.

AD532H



TO-100
TOP VIEW

AD532D



TO-116
TOP VIEW

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, $R \geq 2k\Omega$, V_{OS} Grounded)

Model	AD532J Min	AD532J Typ	AD532J Max	AD532K Min	AD532K Typ	AD532K Max	AD532S Min	AD532S Typ	AD532S Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$		
Total Error ($-10V \leq X, Y \leq +10V$)		±1.5	**±2.0**		±0.7	**±1.0**		±0.5	**±1.0**	%
T_A = min to max		±2.5			±1.5				**±4.0**	%
Total Error vs Temperature		±0.04			±0.03			±0.01	±0.04	%/°C
Supply Rejection (±15V ±10)		±0.05			±0.05			±0.05		%/%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.8			±0.5			±0.5		%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.3			±0.2			±0.2		%
Feedthrough, X (Y Nulled, X = 20V pk-pk 50Hz)		50	**200**		30	**100**		30	**100**	mV
Feedthrough, Y (X Nulled, Y = 20V pk-pk 50Hz)		30	**15**		25	**80**		25	**80**	mV
Feedthrough vs. Temp.		2.0			1.0			1.0		mV p-p/°C
Feedthrough vs. Power Supply		±0.25			±0.25			±0.25		mV/%
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error		75			75			75		kHz
Slew Rate (V_{OUT} 20 pk-pk)		45			45			45		V/µs
Settling Time (to 2%, ΔV_{OUT} = 20V)		1			1			1		µs
NOISE										
Wideband Noise f = 5Hz to 10kHz		0.6			0.6			0.6		mV (rms)
f = 5Hz to 5MHz		3.0			3.0			3.0		mV (rms)
OUTPUT										
Output Voltage Swing	±10	±13		±10	±13		±10	±13		V
Output Impedance (f≤1kHz)		1			1			1		Ω
Output Offset Voltage		±40				**±30**			**±30**	mV
Output Offset Voltage vs. Temp.		0.7			0.7				**2.0**	mV/°C
Output Offset Voltage vs. Supply		±2.5			±2.5			±2.5		mV/%
INPUT AMPLIFIERS (X, Y and Z)										
Signal Voltage Range (Diff. or CM Operating Diff)		±10			±10			±10		V
CMRR	**40**			**50**			**50**			dB
Input Bias Current										
X, Y Inputs		3			1.5	**4**		1.5	**4**	µA
X, Y Inputs T_{min} to T_{max}		10			8			8		µA
Z Input		±10			±5	**±15**		±5	**±15**	µA
Z Input T_{min} to T_{max}		±30			±25			±25		µA
Offset Current		±0.3			±0.1			±0.1		µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\ Z/(X_1-X_2)$			$10V\ Z/(X_1-X_2)$			$10V\ Z/(X_1-X_2)$		
Total Error										
($V_X = -10V$, $-10V \leq V_Z \leq +10V$)		±2			±1			±1		%
($V_X = -1V$, $-10V \leq V_Z \leq +10V$)		±4			±3			±3		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$		
Total Error		±0.8			±0.4			±0.4		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function		$(X_1-X_2)^2/10V$			$(X_1-X_2)^2/10V$			$(X_1-X_2)^2/10V$		
Total Error ($0V \leq V_Z \leq 10V$)		±1.5			±1.0			±1.0		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	**±10**		**±18**	**±10**		**±18**	**±10**		**±22**	V
Suply Current										
Quiescent		**4**	**6**		**4**	**6**		**4**	**6**	mA

NOTE

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown on the first page, and the complete schematic in Figure 1. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1-X_2)(Y_1-Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{os} in critical applications . . . . otherwise the V_{os} pin should be grounded.

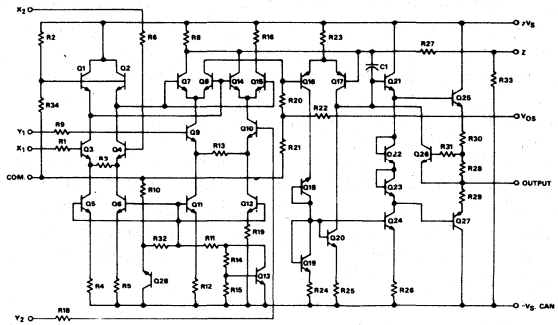


Figure 1. AD532 Schematic Diagram

6

ORDERING GUIDE

Model	Package Option[1]	Max Mult Error	Temperature Range
AD532JH	TO–100	±2.0%	0 to +70°C
AD532JD	TO–116 Style (D14A)	±2.0%	0 to +70°C
AD532KH	TO–100	±1.0%	0 to +70°C
AD532KD	TO–116 Style (D14A)	±1.0%	0 to +70°C
AD532SH	TO–100	±1.0%	-55°C to +125°C
AD532SD	TO–116 Style (D14A)	±1.0%	-55°C to +125°C

[1] See Section 19 for package outline information.

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output amp as shown in Figure 12. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwdith and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10V/X_1-X_2)$ where ϵ_m represents multiplier full scale error and drift, and (X_1-X_2) is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 2 and 3 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 3 the sine wave amplitude is 20V (p-p).

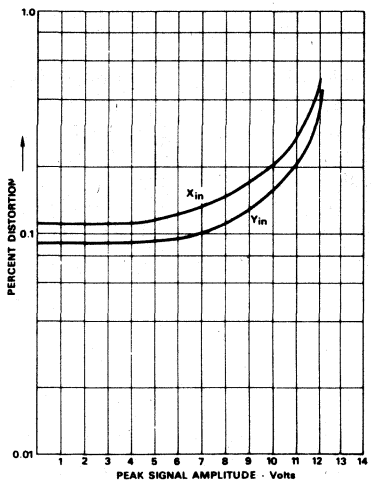


Figure 2. Percent Distortion vs. Input Signal

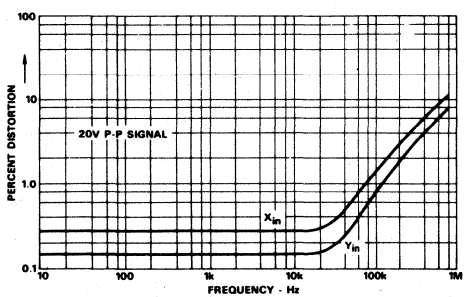


Figure 3. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 4. It is measured for the condition $V_X = 0$, $V_y = 20V(p\text{-}p)$ and $V_y = 0$, $V_X = 20V(p\text{-}p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

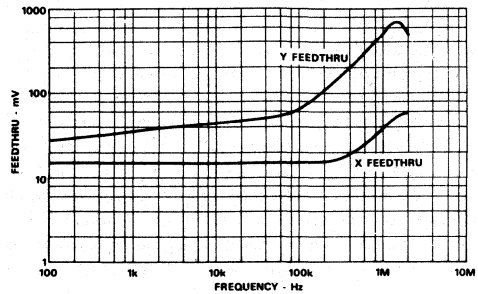


Figure 4. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 5. It is measured with $X_1 = X_2 = 20V$ (p-p), $(Y_1-Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p\text{-}p)$, $(X_1-X_2) = \pm 10V$ dc.

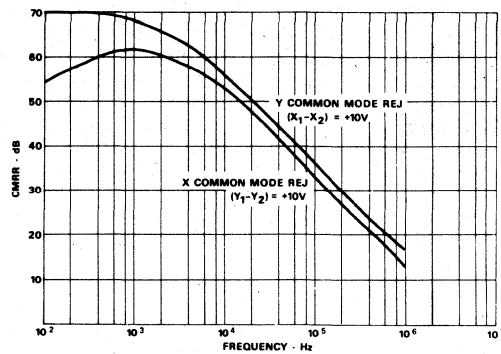


Figure 5. CMRR vs. Frequency

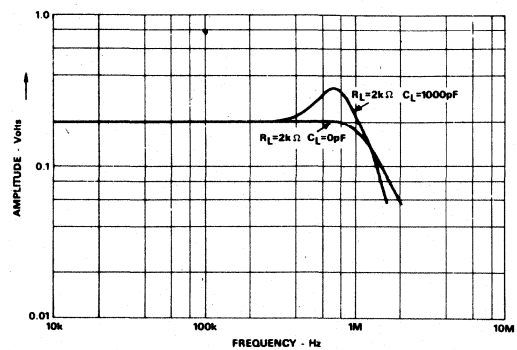


Figure 6. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 6. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 7.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

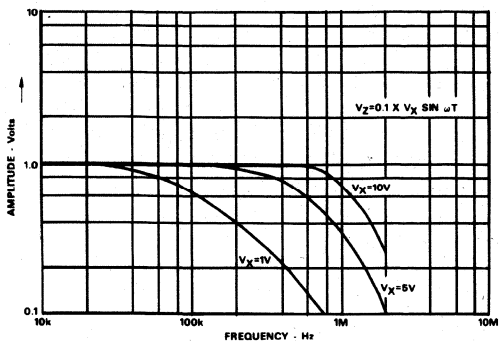


Figure 7. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 8. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

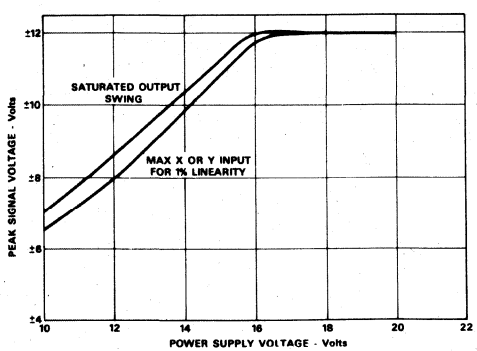


Figure 8. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 9.

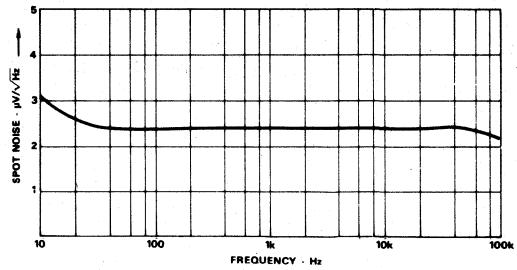


Figure 9. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

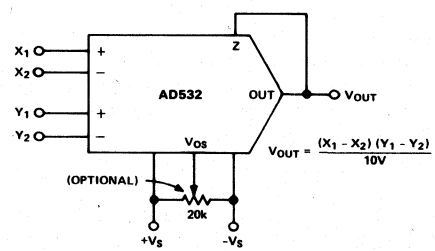


Figure 10. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 10. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see first page). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

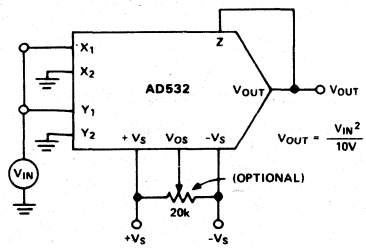


Figure 11. Squarer Connection

The squaring circuit in Figure 11 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

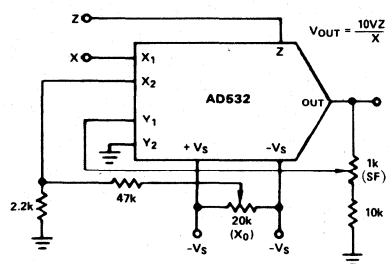


Figure 12. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 12. It should be noted, however, that the output error is given approximately by $10V\epsilon_m/(X_1-X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1-X_2)/10V$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to -10V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $500mV \leq |(X_1-X_2)| \leq 10V$. The voltage offset adjust (V_{os}), if used, is trimmed with Z at zero and (X_1-X_2) at full scale.

SQUARE ROOT

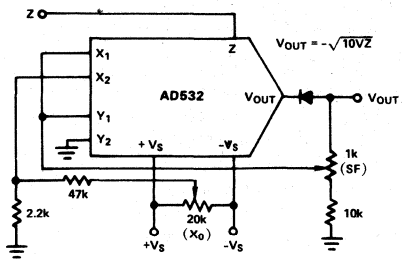


Figure 13. Square Rooter Connection

The connections for square root mode are shown in Figure 13. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{os} to obtain -1.0V dc in the output, $V_{out} = -\sqrt{10VZ}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

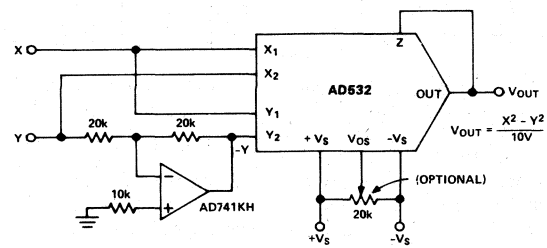


Figure 14. Differential of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2-Y^2/10V$. As shown in Figure 14, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	+10V	±10V	+10V	−10V
X_o (Offset)	−1V	+0.1V	±10V	+0.1V	−1V

Repeat if required.

ANALOG DEVICES

Low Cost IC Multiplier,Divider,Squarer,Square Rooter

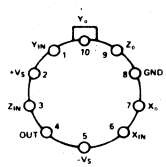
AD533

FEATURES

- **Simplicity of Operation: Only Four External Adjustments**
- **Max 4-Quadrant Error Below 0.5% (AD533L)**
- **Low Temperature Drift: 0.01%/°C (AD533L)**
- **Multiplies, Divides, Squares, Square Roots**

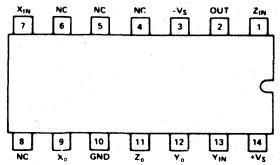
AD533 PIN CONFIGURATIONS

AD533H



TO-100
TOP VIEW

AD533D



TO-116
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD533 is a low cost integrated circuit multiplier comprised of a transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. Specified accuracy is easily achieved by the straight-forward adjustment of feedthrough, output zero, and gain trim pots. The AD533 multiplies in four quadrants with a transfer function of XY/10V, divides in two quadrants with a 10VZ/X transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10VZ}$. Several levels of accuracy are provided: the AD533J, AD533K, and AD533L, for 0 to +70°C operation, are specified for maximum multiplying errors of 2%, 1%, and 0.5% respectively at +25°C. The AD533S, for operation from -55°C to +125°C, is guaranteed for a maximum 1% multiplying error at +25°C. The maximum error specification is a true measure of overall accuracy since it includes the effects of offset voltage, feedthrough, scale factor, and nonlinearity in all four quadrants.

The low drift design of the AD533 insures that high accuracy is maintained with variations in temperature. The op amp output provides ±10 volts at 5mA, and is fully protected against short circuits to ground or either supply voltage: all inputs are fully protected against over-voltage transients with internal series resistors. The devices provide excellent ac performance, with typical small signal bandwidth of 1.0MHz, full power bandwidth of 750kHz, and slew rate of 45V/μs.

The low cost and simplicity of operation of the AD533 make it especially well suited for use in such widespread applications as modulation and demodulation, automatic gain control and phase detection. Other applications include frequency discrimination, rms computation, peak detection, voltage controlled oscillators and filters, function generation, and power measurements.

All models are available in the hermetically sealed TO-100 metal can and TO-116 ceramic DIP packages.

SPECIFICATIONS (typical @ +25°C, externally trimmed and V_S = ±15V dc unless otherwise specified)

PARAMETER	CONDITIONS	AD533J	AD533K	AD533L	AD533S
ABSOLUTE MAX RATINGS					
Internal Power Dissipation		500mW	*	*	*
Input Voltage[1]					
X_{in}, Y_{in}, Z_{in}, X_O, Y_O, Z_O		$\pm V_S$	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	−55°C to +125°C
Storage Temp Range		−65°C to +150°C	*	*	*
Output Short Circuit	To Ground	Indefinite	*	*	*
MULTIPLIER SPECIFICATIONS					
Transfer Function		XY/10V	*	*	*
	Untrimmed	XY/6V max [XY/10V min]	*	*	*
Total Error (of full scale)		±2.0% max	±1.0% max	±0.5% max	±1.0% max
	T_A = min to max	±3.0%	±2.0%	±1.0%	±1.5%
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.01%/°C
Nonlinearity					
X Input	$V_X = V_O$ = 20V(p-p)	±0.8%	±0.5%	**	**
Y Input	$V_Y = V_O$ = 20V(p-p)	±0.3%	±0.2%	**	**
Feedthrough					
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	200mV (p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	200mV(p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
DIVIDER SPECIFICATIONS					
Transfer Function		10VZ/X	*	*	*
	Untrimmed	10VZ/X max [6VZ/X min]	*	*	*
Total Error (of full scale)	V_x = −10V dc, V_z = ±10V dc	±1.0%	±0.5%	±0.2%	±0.5%
	V_x = −1V dc, V_z = ±10V dc	±3.0%	±2.0%	±1.5%	±2.0%
SQUARER SPECIFICATIONS					
Transfer Function		$X^2/10V$	*	*	*
	Untrimmed	$X^2/6V$ max [$X^2/10V$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
SQUARE ROOTER SPECIFICATIONS					
Transfer Function		$-\sqrt{10VZ}$	*	*	*
	Untrimmed	$-\sqrt{10VZ}$ max [$-\sqrt{6VZ}$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
INPUT SPECIFICATIONS					
Input Resistance					
X Input		10MΩ	*	*	*
Y Input		6MΩ	*	*	*
Z Input		36kΩ	*	*	*
Input Bias Current					
X, Y Inputs		3μA	7.5μA max	5μA max	7.5μA max
Z Input		±25μA	*	*	*
X, Y Inputs	T_A = min to max	12μA	10μA	7μA	7μA
Z Input	T_A = min to max	±35μA	*	*	*
Input Voltage	T_A = min to max				
V_X, V_Y, V_Z	For Rated Accuracy	±10V	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μs	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Sm Sig 1% Vector Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μs to 2%	*	*	*
Overload Recovery		2μs to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance		100Ω	*	*	*
Output Voltage Swing	T_A = min to max				
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		Trimmable To Zero	*	*	*
vs. Temperature	T_A = min to max	0.7mV/°C	*	*	*
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	Rated Performance	±15V	*	*	*
	Operating	±15V to ±18V	±10V to ±18V	±10V to ±18V	±10V to ±22V
Supply Current	Quiescent	±6mA max	*	*	*
Power Supply Variation	*Includes* Effects of Recommended Null Pots				
Multiplier Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor		±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

NOTES

[1] Max input voltage is zero when supplies are turned off.

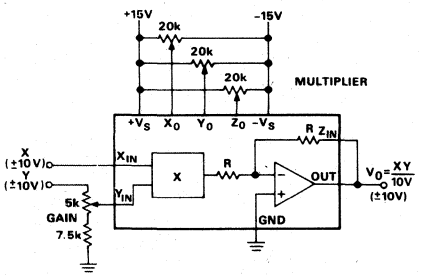
*Specifications same as AD533J.

**Specifications same as AD533K.

Specifications subject to change without notice.

MULTIPLIER

Multiplier operation is accomplished by closing the loop around the internal op amp with the Z input connected to the output. The X_O null pot balances the X input channel to minimize Y feedthrough and similarly the Y_O pot minimizes the X feedthrough. The Z_O pot nulls the output op amp offset voltage and the gain pot sets the full scale output level.



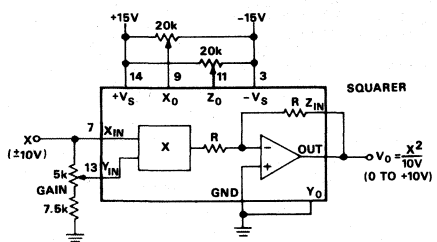
TRIM PROCEDURES

1. With X = Y = 0 volts, adjust Z_O for 0V dc output.
2. With Y = 20 volts p-p (at f = 50Hz) and X = 0V, adjust X_O for minimum ac output.
3. With X = 20 volts p-p (at f = 50Hz) and Y = 0V, adjust Y_O for minimum ac output.
4. Readjust Z_O for 0V dc output.
5. With X = +10V dc and Y = 20 volts p-p (at f = 50Hz), adjust gain for output = Y_{in}.

NOTE: For best accuracy over limited voltage ranges (e.g., ±5V), gain and feedthrough adjustments should be optimized with the inputs in the desired range, as linearity is considerably better over smaller ranges of input.

SQUARER

Squarer operation is a special case of multiplier operation where the X and Y inputs are connected together and two quadrant operation results since the output is always positive. When the X and Y inputs are connected together, a composite offset results which is the algebraic sum of the individual offsets which can be nulled using the X_O pot alone.

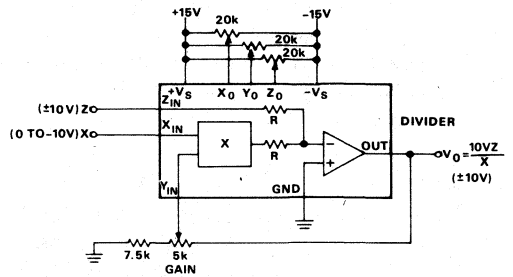


TRIM PROCEDURES

1. With X = 0 volts, adjust Z_O for 0V dc output.
2. With X = +10V dc, adjust gain for +10V dc output.
3. Reverse polarity of X input and adjust X_O to reduce the output error to ½ its original value; readjust the gain to take out the remaining error.
4. Check the output offset with input grounded. If nonzero, repeat the above procedure until no errors remain.

DIVIDER

The divide mode utilizes the multiplier in a fed-back configuration where the Y input now controls the feedback factor. With X = full scale, the gain (V_O/Z) becomes unity after trimming. Reducing the X input reduces the feedback around the op amp by a like amount, thereby increasing the gain. This reciprocal relationship forms the basis of the divide mode. Accuracy and bandwidth decrease as the denominator decreases.

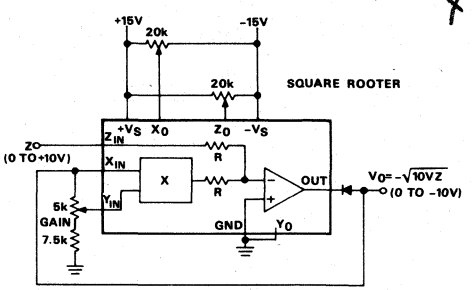


TRIM PROCEDURES

1. Set all pots at mid-scale.
2. With Z = 0V, trim Z_O to hold the output constant, as X is varied from -10V dc through -1V dc.
3. With Z = 0V, X = -10V dc, trim Y_O for 0V dc.
4. With Z = X or -X, trim X_O for the minimum worst-case variations as X is varied from -10V dc to -1V dc.
5. Repeat steps 2 and 3 if step 4 required a large initial adjustment.
6. With Z = X or -X, trim the gain for the closest average approach to ±10V dc output as X is varied from -10V dc to -3V dc.

SQUARE ROOTER

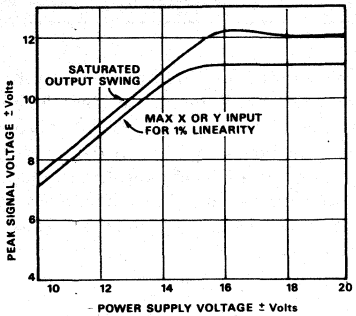
This mode is also a fed-back configuration with both the X and Y inputs tied to the op amp output through an external diode to prevent latchup. Accuracy, noise and frequency response are proportional to $\sqrt{Z}$, which implies a wider usable dynamic range than the divide mode.



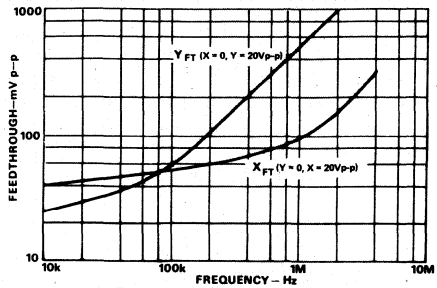
TRIM PROCEDURES

1. With Z = +0.1V dc, adjust Z_O for Output = -1.0V dc.
2. With Z = +10.0V dc, adjust gain for Output = -10.0V dc.
3. With Z = +2.0V dc, adjust X_O for Output = -4.47 ±0.1V dc.
4. Repeat steps 2 and 3, if necessary. Repeat step 1.

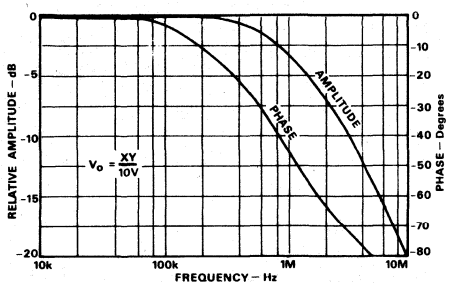
TYPICAL PERFORMANCE CHARACTERISTICS



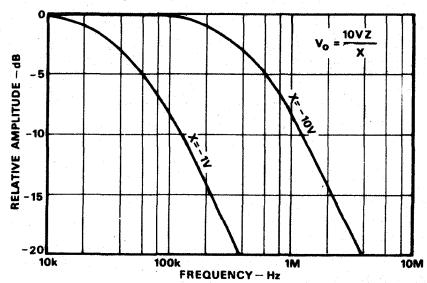
Allowable Signal Swing vs. Supply Voltage



Feedthrough vs. Frequency



Closed Loop Frequency and Phase Response



Divide Mode Frequency Response

ORDERING GUIDE

MODEL	MULT. ERROR (Max @ +25°C)	TEMP. RANGE	ORDER NUMBER	PACKAGE OPTIONS[1]
AD533J	±2.0%	0 to +70°C	AD533JH	TO-100
			AD533JD	TO-116 Style (D14A)
AD533K	±1.0%	0 to +70°C	AD533KH	TO-100
			AD533KD	TO-116 Style (D14A)
AD533L	±0.5%	0 to +70°C	AD533LH	TO-100
			AD533LD	TO-116 Style (D14A)
AD533S	±1.0%	-55°C to +125°C	AD533SH	TO-100
			AD533SD	TO-116 Style (D14A)

[1] See Section 19 for package outline information.

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD534

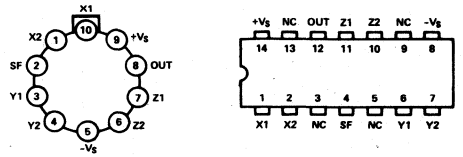
FEATURES

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters

AD534 PIN CONFIGURATIONS



TO-100 **TO-116**

TOP VIEW

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00V; by means of an external resistor, this can be reduced to values as low as 3V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, -55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS ($T_A = +25°C$, $\pm V_S = 15V$, $R \geq 2k\Omega$)

Model	AD534J			AD534K			AD534L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] ($-10V \leq X, Y \leq +10V$)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling-Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.01			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**		±0.003	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		µV/°C
DYNAMICS										
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2		µs
NOISE										
Noise Spectral-Density SF = 10V		0.8			0.8			0.8		µV/√Hz
SF = 3V[4]		0.4			0.4			0.4		µV/√Hz
Wideband Noise f = 10Hz to 5MHz		1			1			1		mV/rms
f = 10Hz to 10kHz		90			90			90		µV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		µV/°C
CMRR	**60**	80		**70**	90		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.05	**0.2**	µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, $-10V \leq Z \leq +10V$)		±0.75			±0.35			±0.2		%
($X - 1V$, $-1V \leq Z \leq +1V$)		±2.0			±1.0			±0.8		%
($0.1V \leq X \leq 10V$, $-10V \leq Z \leq 10V$)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{100}+Z_2$			$\frac{(X_1-X_2)^2}{100}+Z_2$			$\frac{(X_1-X_2)^2}{100}+Z_2$		
Total Error ($-10V \leq X \leq 10V$)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2-Z_1)}+Y_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] ($1V \leq Z \leq 10V$)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	**±8**		**±18**	**±8**		**±18**	**±8**		**±18**	V
Supply Current										
Quiescent		4	**6**		4	6		4	**6**	mA
PACKAGE OPTIONS[6]										
H: TO-100 Package	**AD534JH**			**AD534KH**			**AD534LH**			
D: TO-116 Package (D14A)	**AD534JD**			**AD534KD**			**AD534LD**			

NOTES
[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
[6]See Section 19 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD534S			AD534T			Units
	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			±1.0			±0.5	%
T_A = min to max			±2.0			±1.0	%
Total Error vs Temperature			±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1		%
Temperature-Coefficient of Scaling-Voltage		±0.02				±0.005	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	±0.3	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.01			±0.1	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	±0.3	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	±0.1	%
Output Offset Voltage		±5	±30		±2	±15	mV
Output Offset Voltage Drift			500			300	µV/°C
DYNAMICS							
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10V		0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1.0			1.0		mV/rms
f = 10Hz to 10kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	±11			±11			V
Output Impedance (f≤1kHz)		0.1			0.1		Ω
Output Short Circuit Current R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM		±10			±10		V
Operating Diff.)		±12			±12		V
Offset Voltage X, Y		±5	±20		±2	±10	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	±30		±2	±15	mV
Offset Voltage Drift Z			500			300	µV/°C
CMRR	60	80		70	90		dB
Bias Current		0.8	2.0		0.8	2.0	µA
Offset Current		0.1	2.0		0.1	2.0	µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, −10V≤Z≤+10V)		±0.75			±0.75		%
(X = 1V, −1V≤Z≤+1V)		±2.0			±2.0		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2.5			±1.0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)^2+Z_2}{10V}$			$\frac{(X_1-X_2)^2+Z_2}{10V}$		
Total Error (−10V≤X≤10V)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	±8		±22	±8		±22	V
Supply Current							
Quiescent		4	6		4	6	mA
PACKAGE OPTIONS[6]							
H: TO-100 Package		AD534SH			AD534TH		
D: TO-116 Package (D14A)		AD534SD			AD534TD		

NOTES
[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

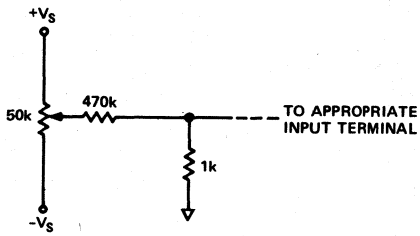
Using the AD534

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.05% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

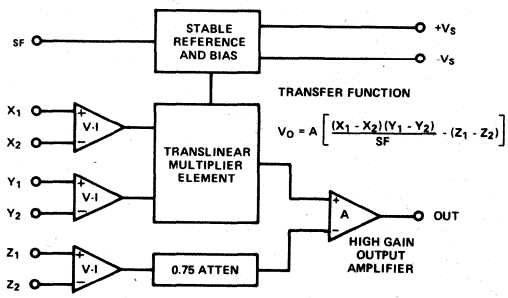


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite, and SF will be 10V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10V(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

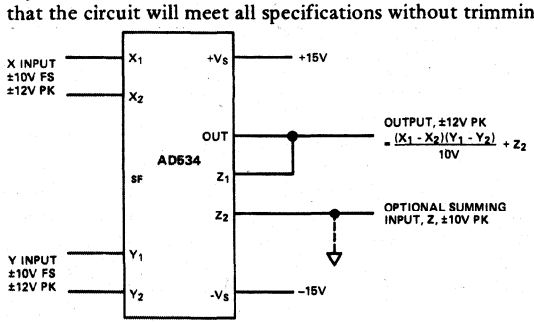


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input (see Optional Trimming Configuration). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

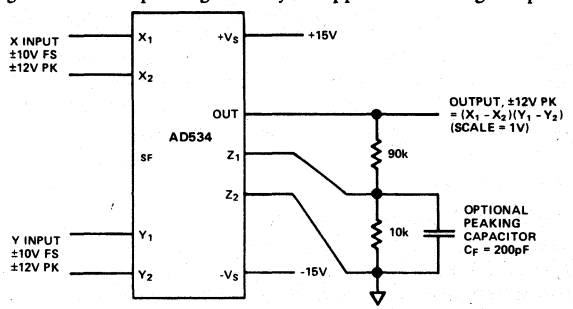


Figure 3. Connections for Scale-Factor of Unity

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

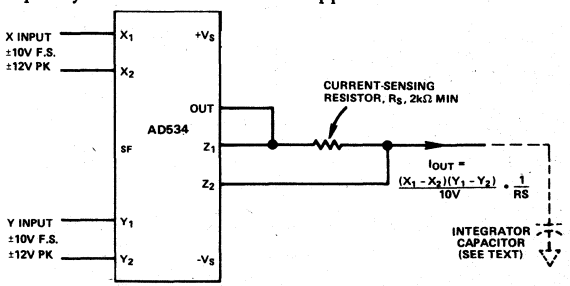


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

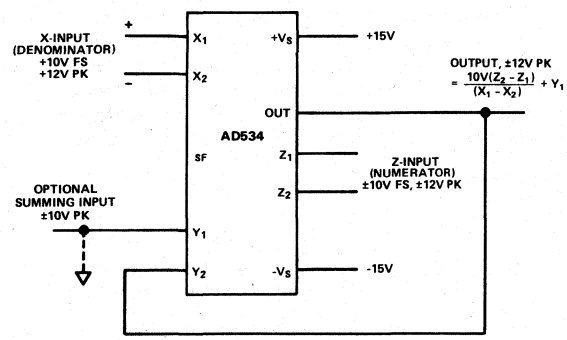


Figure 5. Basic Divider Connection

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input (see Optional Trimming Configuration). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

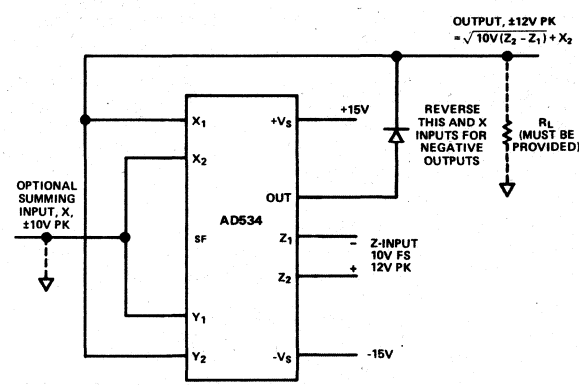


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1V.

*See the AD535 Data Sheet for more details.

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few. These applications along with many other such "idea stimulators" are described in detail in the *Multiplier Application Guide*, available upon request from Analog Devices.

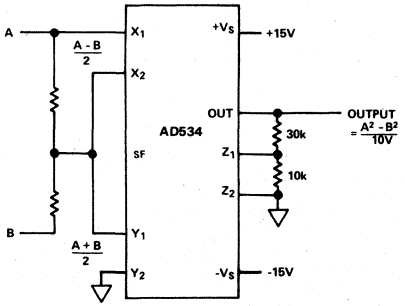
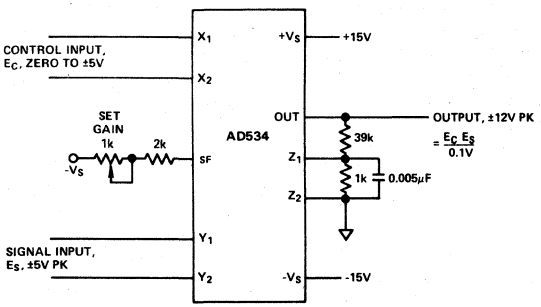
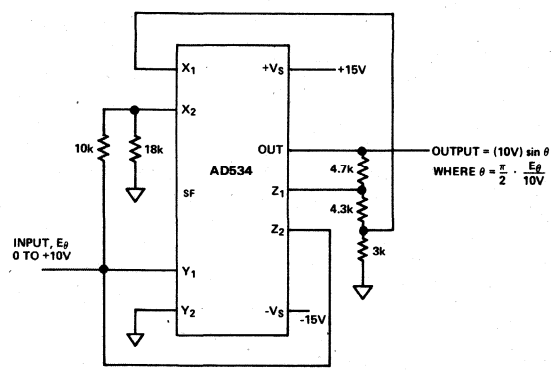


Figure 7. Difference-of-Squares



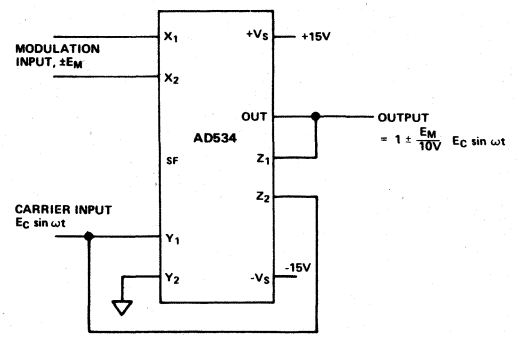
NOTES:
1) GAIN IS X10 PER VOLT OF E_C, ZERO TO X50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F.S. S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60µV RMS, TYP
4) BANDWIDTH IS DC TO 20kHz, -3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



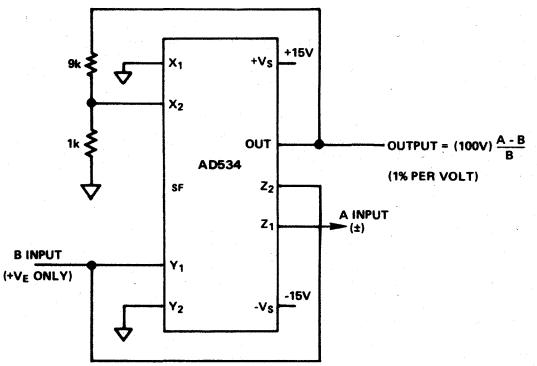
USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator



THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION. OPERATION FROM A SINGLE SUPPLY IS POSSIBLE; BIAS Y_2 TO $V_S/2$.

Figure 10. Linear AM Modulator



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 11. Percentage Computer

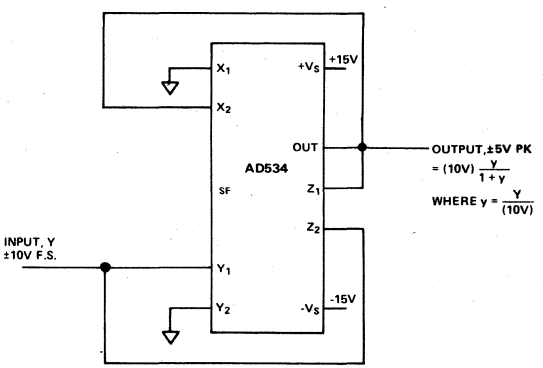
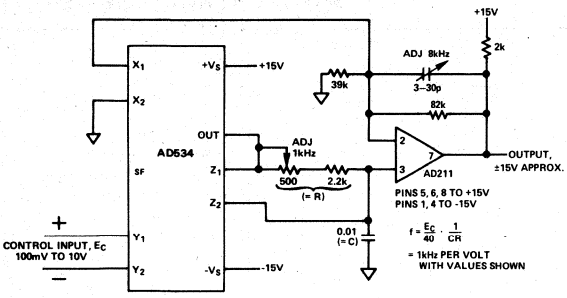


Figure 12. Bridge-Linearization Function



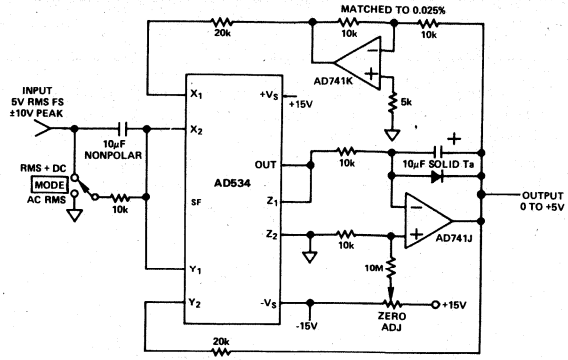
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1,000kHz. WITH E_C = 8.0V, ADJUST TRIMMER CAPACITOR TO SET f = 8,000kHz. LINEARITY WILL TYPICALLY BE WITHIN ±0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE TO FREQUENCY CONVERTER IS RECOMMENDED.

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01μF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED FROM 60Hz to 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE).

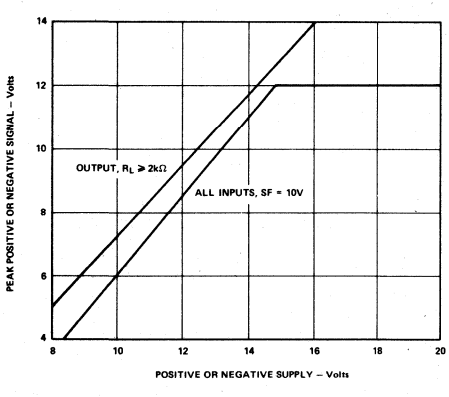
PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

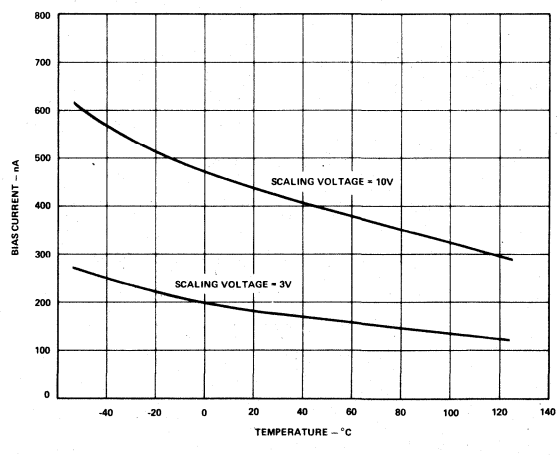
FOR GUARANTEED SPECIFICATIONS THE AD536A AND AD636 IS OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER.

Figure 14. Wideband, High-Crest Factor, RMS-to-DC Converter

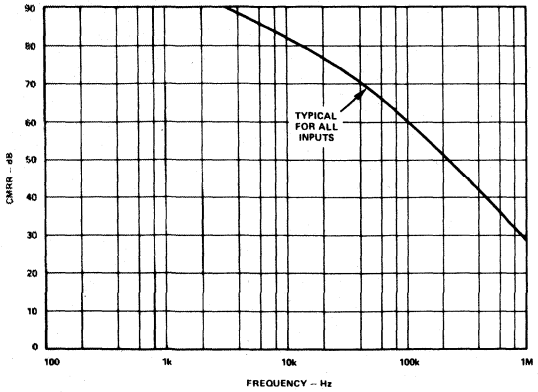
Typical Performance Curves (typical at +25°C, with V_S = ±15V dc, unless otherwise stated)



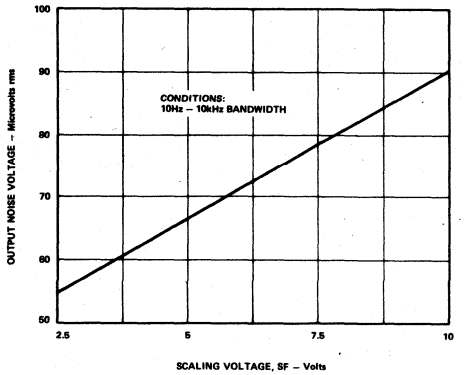
Curve 1. Input/Output Signal Range Vs. Supply Voltages



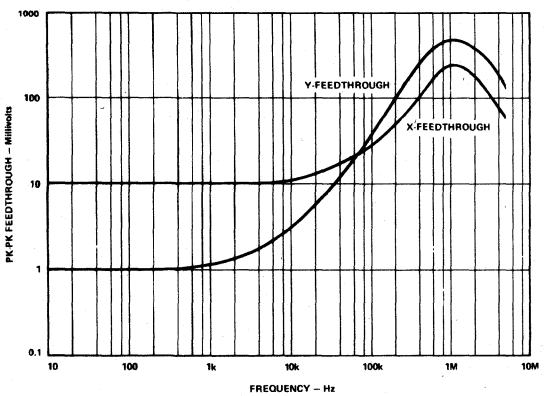
Curve 2. Bias Currents Vs. Temperature (X, Y or Z inputs)



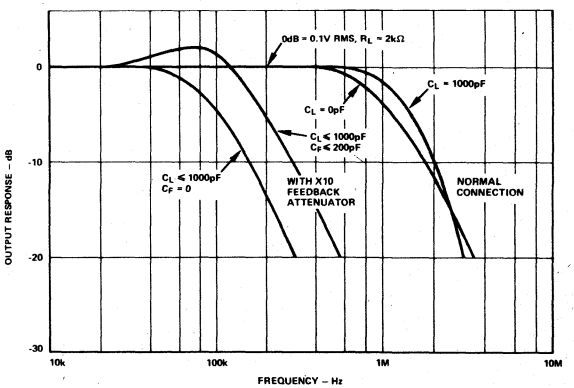
Curve 3. Common-Mode-Rejection-Ratio Vs. Frequency



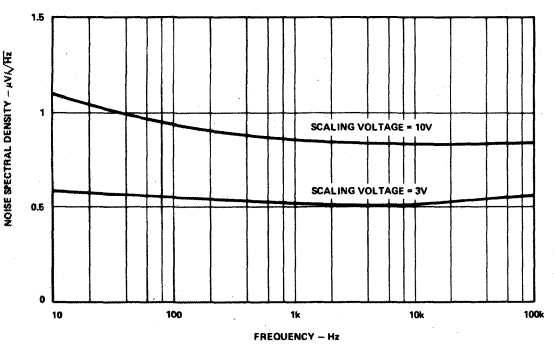
Curve 6. Wideband Noise Vs. Scaling Voltage



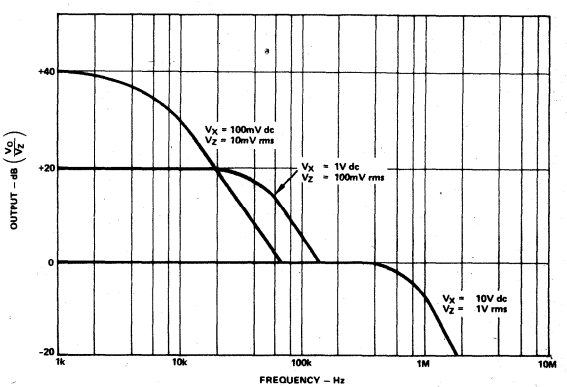
Curve 4. AC Feedthrough Vs. Frequency



Curve 7. Frequency Response as a Multiplier



Curve 5. Noise Spectral Density Vs. Frequency



Curve 8. Frequency Response Vs. Divider Denominator Input Voltage

ANALOG DEVICES

Internally Trimmed Integrated Circuit Divider

AD535

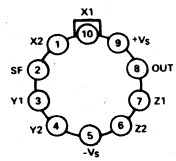
FEATURES

Pretrimmed to ±0.5% max Error, 10:1 Denominator Range (AD535K)
±2.0% max Error, 50:1 Denominator Range (AD535K)
All Inputs (X, Y and Z) Differential

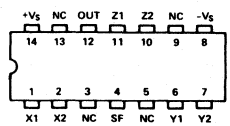
APPLICATIONS

General Analog Signal Processing
Differential Ratio and Percentage Computations
Precision AGC Loops
Square-Rooting

AD535 PIN CONFIGURATIONS



TO-100
(TOP VIEW)



TO-116
(TOP VIEW)

PRODUCT DESCRIPTION

The AD535 is a monolithic laser-trimmed two-quadrant divider having performance specifications previously found only in expensive hybrid or modular products. A maximum divider error of ±0.5% is guaranteed for the AD535K without any external trimming over a denominator range of 10:1; ±2.0% max error over a range of 50:1. A maximum error of ±1% over the 50:1 denominator range is guaranteed with the addition of two external trims. The AD535 is the first divider to offer fully differential, high impedance operation on all inputs, including the z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced by any amount down to 3.

The extraordinary versatility and performance of the AD535 recommend it as the first choice in many divider and computational applications. Typical uses include square-rooting, ratio computation, "pin-cushion" correction and AGC loops. The device is packaged in a hermetically sealed, 10-pin TO-100 can or 14-pin TO-116 DIP and made available in a ±1% max error version (J) and a ±0.5% max error version (K). Both versions are specified for operation over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. Laser trimming at the wafer stage enables the AD535 to provide high accuracies without the addition of external trims (±0.5% max error over a 10:1 denominator range for the AD535K).
2. Improved accuracies over a wider denominator range are possible with only two external trims (±0.5% max error over a 20:1 denominator range for the AD535K).
3. Differential inputs on the X, Y and Z input terminals enhance the AD535's versatility as a generalized analog computational circuit.
4. Monolithic construction permits low cost and, at the same time, increased reliability.

SPECIFICATIONS (V_S = ±15V, R_L > 2kΩ, T_A = +25°C unless otherwise stated)

PARAMETER	CONDITIONS	AD535J	AD535K
TRANSFER FUNCTION	Figure 2	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*
TOTAL ERROR[1]	No External Trims, Figure 2		
	1V≤X≤10V, Z≤|X|	1.0% max	0.5% max
	0.2V≤X≤10V, Z≤|X|	5.0% max	2.0% max
	With External Trims, Figure 5		
	0.5V≤X≤10V, Z≤|X|	1.0% max	0.5% max
	0.2V≤X≤10V, Z≤|X|	2.0% max	1.0% max
TEMPERATURE COEFFICIENT	1V≤X≤10V, Z≤|X|	0.01%/°C typ	*
	0.5V≤X≤10V, Z≤|X|	0.02%/°C typ	*
	0.2V≤X≤10V, Z≤|X|	0.05%/°C typ	*
SUPPLY RELATED	1V≤X≤10V	0.1%/V typ	*
Error	0.5V≤X≤10V	0.2%/V typ	*
V_S = ±14V to ±16V	0.2V≤X≤10V	0.5%/V typ	*
SQUARE ROOTER	No External Trims, Figure 11		
TOTAL ERROR[1]	1V≤Z≤10V	0.4% typ	*
	0.2V≤Z≤10V	0.7% typ	*
NOISE[2]	X = 0.2V, f = 10Hz to 10kHz	4.5mV rms typ	*
BANDWIDTH	X = 0.2V	20kHz typ	*
INPUT AMPLIFIERS[3]			
CMRR	f = 50Hz, 20V p-p	60dB min	*
Bias Current		2.0μA max	*
Offset Current		0.1μA typ	*
Differential Resistance		10MΩ typ	*
OUTPUT AMPLIFIER[3]			
Open-Loop Gain	f = 50Hz	70dB typ	*
Small Signal Gain-Bandwidth	V_{OUT} = 0.1V rms	1MHz typ	*
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz typ	*
Output Voltage Swing	T_{min} to T_{max}	±11V min	*
Slew Rate	V_{OUT} = 20V p-p	20V/μs typ	*
Settling Time	V_{OUT} = 20V ±1%	2μs typ	*
Output Impedance	Unity Gain, f≤1kHz	0.1Ω typ	*
Wide-band Noise	f = 10Hz to 5MHz	1mV rms typ	*
	f = 10Hz to 10kHz	90μV rms typ	*
OUTPUT SHORT CURRENT	T_{min} to T_{max}, R_1 = 0	30mA	*
POWER SUPPLIES			
Rated Performance		±15V	*
Operating		±8V min, ±18V max	*
Supply Current	Quiescent	6mA max	*
PACKAGE OPTIONS[4]			
H: TO-100		AD535JH	AD535KH
D: TO-116 Style (D14A)		AD535JD	AD535KD

NOTES
*Specifications same as AD535J.
[1] Figures are given as a percent of full scale (i.e. 1.0% = 100mV).
[2] Noise may be reduced as shown in Figure 14.
[3] See Figure 1 for definition of section.
[4] See Section 19 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltages, X_1, X_2, Y_1, Y_2, Z_1, Z_2	$\pm V_S$
Rated Operating Temp Range	0 to +70°C
Storage Temp Range	−65°C to +150°C
Lead Temp, 60s soldering	+300°C

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD535. Inputs are converted to differential currents by three identical voltage to current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique with an internal scaling voltage.

The difference between XY/SF and Z is applied to the high gain output amplifier. The transfer function can then be expressed...

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - V_{OUT})}{SF} - (Z_1 - Z_2)\right]$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite and SF will be 10V. Dividing both sides of the equation by A and solving the V_{OUT}, we get...

$$V_{OUT} = 10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$$

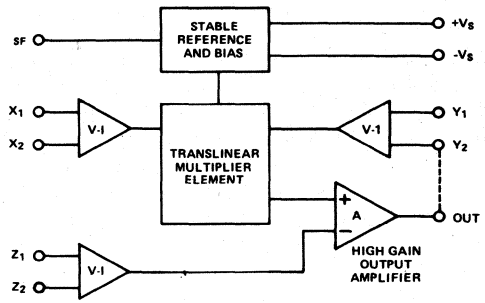


Figure 1. AD535 Functional Block Diagram

SOURCES OF ERROR

Divider error is specified as a percent of full scale (i.e. 10.00V) and consists primarily of the effects of X, Y and Z offsets and scale factor (which are trimmable) as shown in the generalized equation....

$$V_{OUT} = (SF + \Delta SF)\left[\frac{(Z_2 - Z_1) + Z_{OS}}{(X_1 - X_2) + X_{OS}}\right] + Y_1 + Y_{OS}$$

Note especially that divider error is inversely proportional to X, that is, the error increases rapidly with decreasing denominator values. Hence, the AD535 divider error is specified over several denominator ranges on previous page. (See also Figure 12, AD535 Total Error as a function of denominator values.)

Overall accuracy of the AD535 can be significantly improved by nulling out X and Z offset as described in the applications sections. Figure 13 illustrates a factor of 2 improvement in accuracy with the addition of these external trims. The remaining errors stem primarily from scale factor error and Y offsets which can be trimmed out as shown in Figure 6.

Figure 14 illustrates the bandwidth and noise relationships versus denominator voltage. Whereas noise increases with decreasing denominator, bandwidth decreases, the net result given by the expression...

$$En_{OUT}\ (\text{wideband}) = \frac{1.26}{\sqrt{\left(\frac{X}{10}\right)}}\ \text{mV rms}$$

External filtering can be added to limit output voltage noise even further. In this case...

$$En_{OUT}\ (\text{B.W. externally limited}) = \frac{0.9\sqrt{f}}{\left(\frac{X}{10}\right)}\ \text{mV rms}$$

where f = bandwidth in MHz of an external filter whose bandwidth is less than the noise bandwidth of the AD535. Table I provides calculated values of the typical output voltage noise, both filtered and unfiltered for several denominator values.

X	Noise 10Hz to 5MHz	Noise Limited by External Filtering 10Hz to 10kHz
0.2V	8.9mV rms	4.5mV rms
0.5V	5.6mV rms	1.8mV rms
1V	4.0mV rms	0.9mV rms
10V	1.3mV rms	0.09mV rms

Table I. AD535 Calculated Voltage Noise

APPLICATIONS

Figure 2 shows the standard divider connection without external trims. The denominator X, is restricted to positive values in this configuration. X, Y and Z inputs are differential with high (80dB typical) CMRR permitting the application of differential signals on X and Z (see Figure 3).

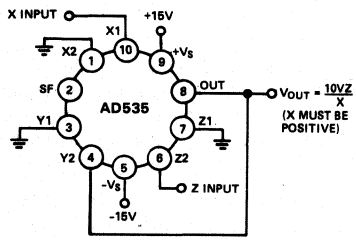


Figure 2. Divider Without External Trims

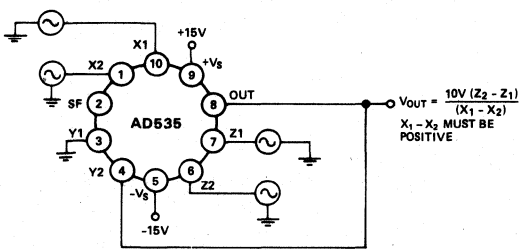


Figure 3. Differential Divider Connection

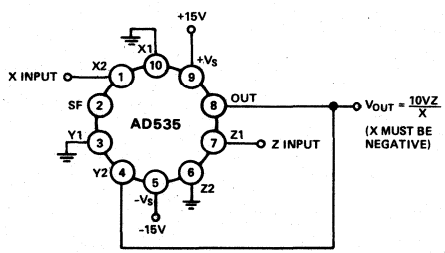


Figure 4. Divider Connection for Negative X Inputs

Negative denominator inputs are handled as shown in Figure 4. Note that in either configuration, operation is limited to two quadrants (i.e. Z is bipolar, X is unipolar).

A factor of two improvements in accuracy is possible by trimming the X and Z offsets as illustrated in Figure 5. To trim, set X to the smallest denominator value for which accurate computation is required (i.e., X = 0.2V). With Z = 0, adjust the Z_O trim for V_{OUT} = 0. Next, adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V). Finally, readjust Z_O for the best compromise at Z = +X, Z = -X and Z = O. The remaining error (Figure 13) consists primarily of scale factor error, output offset and an irreducible nonlinearity component.

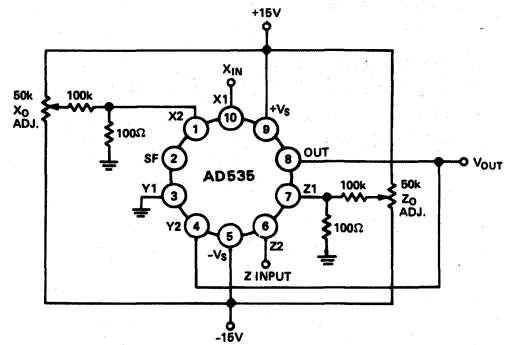


Figure 5. Precision Divider Using Two Trims

In certain applications, the user may elect to adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} ±25% using the potentiometer. Note that the peak signal is always limited to 1.25 SF (i.e. ±5V for SF = 4).

The scale factor may also be adjusted using a feedback attenuator between V_{OUT} and Y2 as indicated in Figure 6. The input signal range is unaffected using this scheme.

Scale factor and output offset error can be minimized utilizing the four trim circuit of Figure 6. Adjustment is as follows:

1. Apply X = +0.2V (or the smallest required denominator value), Z = 0 and adjust Z_O for V_{OUT} = 0.
2. Apply X = 0.2V. Then adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V.)
3. Apply X = +10V, Z = 0 and adjust Y_O for V_{OUT} = 0.
4. Apply X = +10V. Then adjust the scale factor (SF) trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V).
5. Repeat steps 1 and 2.
6. Apply X = 0.2V. Then adjust the Z trim for the best compromise when Z = X (V_{OUT} = +10V), Z = 0 (V_{OUT} = 0) and Z = -X (V_{OUT} = -10V).

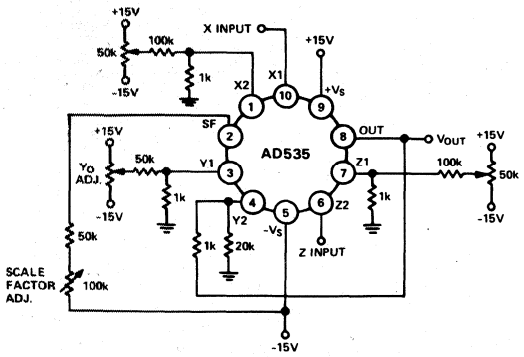


Figure 6. Precision Divider with Four External Adjustments

These trim adjustments can be made either by using two calibrated voltage sources and a DVM, or by using a differential scope, a low frequency generator, a voltage source and a precision attenuator. As shown in Figure 7, the differential scope subtracts the expected ideal output and thus displays only errors. Set the attenuation to $\frac{X}{10V}$.

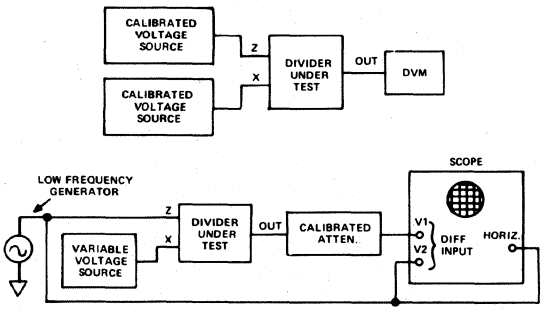


Figure 7. Alternate Trim Adjustment Set-Up

PIN-CUSHION CORRECTION

A pin-cushion corrector eliminates the distortion caused by flat screen CRT tubes. The correction equations are:

$$V_{OH} = \frac{V_{IH}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

and

$$V_{OV} = \frac{V_{IV}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

where: V_{OH} and V_{OV} are the horizontal and vertical output signals, respectively.

V_{IH} and V_{IV} are the horizontal and vertical input signals, respectively.

L is the length of the CRT tube.

In typical applications L (expressed in voltage) is roughly equal to full scale V_{IH} or V_{IV}. The result is that the expression, $\sqrt{(V_{IH}^2 + V_{IV}^2 + L^2)}$, varies less than 2:1 over the full range of values of V_{IH} and V_{IV}.

Major sources of divider error associated with small denominator values can thereby the minimized.

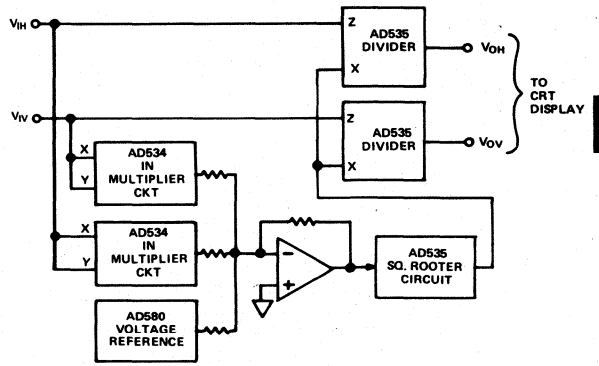


Figure 8. Pin-Cushion Corrector

Figure 9 shows an AGC loop using an AD535 divider. The AD535 lends itself naturally in this application since it is configured to provide gain rather than loss. Overall gain varies from 1 to ∞ as the denominator is servoed to maintain V_{OUT} at a constant level.

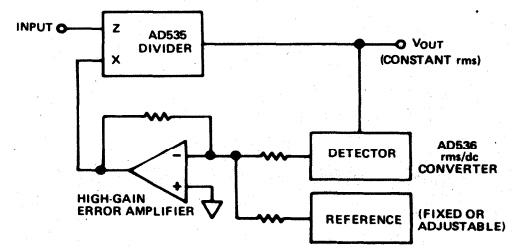


Figure 9. AGC Loop Using the AD536 rms/dc Converter as a Detector

Figure 10 shows a method for obtaining the time average as defined by:

$$\overline{X} = \frac{1}{T}\int_0^T X\,dt$$

where T is the time interval over which the average is to be taken. Conventional techniques typically provide only a crude approximation to the true time average, and furthermore, require a fixed time interval before the average can be taken. In Figure 10, the AD535 is used to divide the integrator output by the ramp generator output. Since the ramp is proportional to time, the integrator is divided by the time interval, thus allowing continuous, true time processing of signals over intervals varying by as much as 50:1.

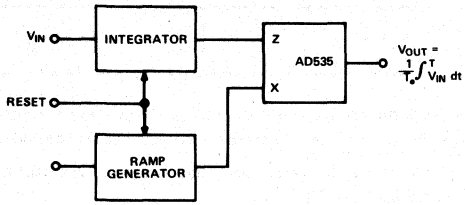


Figure 10. Time Average Computation Circuit

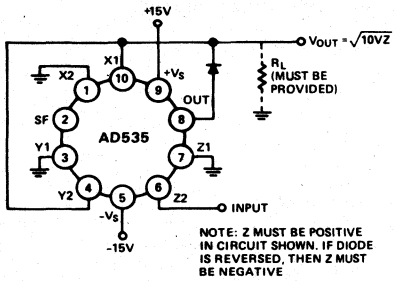


Figure 11. Square Rooter

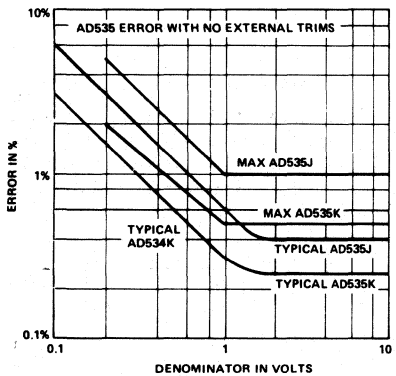


Figure 12. AD535 Error with No External Trims

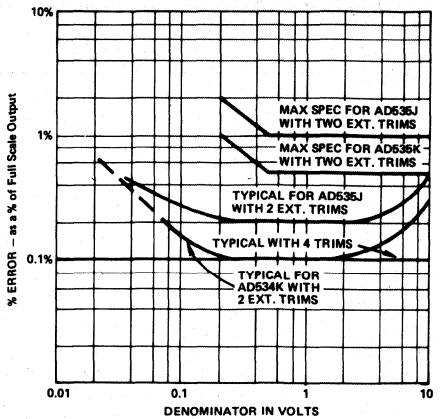


Figure 13. Errors with External Trims at 25°C

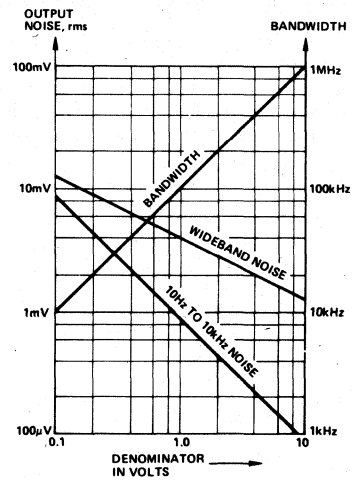


Figure 14. -3dB Bandwidth and Noise vs. Denominator

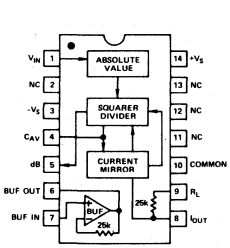
Integrated Circuit True rms-to-dc Converter

AD536A

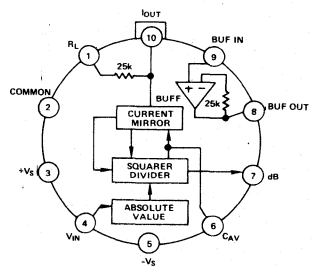
FEATURES

- True rms-to-dc Conversion
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 300kHz Bandwidth: $V_{rms} > 100mV$
  - 2MHz Bandwidth: $V_{rms} > 1V$
  - Signal Crest Factor of 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- -55°C to +125°C Operation (AD536AS)
- Low Cost

AD536A FUNCTIONAL BLOCK DIAGRAMS



TO-116
TOP VIEW



TO-100
TOP VIEW

PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the -55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536, and provides improved bandwidth and temperature drift specifications.

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD536AJ			AD536AK			AD536AS			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig. 1)			**±5 ±0.5**			**±2 ±0.2**			**±5 ±0.5**	mV ± % of Reading
vs. Temperature, T_{min} to +70°C			±0.1 ±0.01			±0.05 ±0.005			**±0.1 ±0.005**	mV ± % of Reading
+70°C to +125°C									**±0.3 ±0.005**	mV ± % of Reading
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading
vs. Reversal Error		±0.2			±0.1			±0.2		% of Reading
Total Error, External Trim[1] (Fig. 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR vs CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.1			−0.1			−0.1		% of Reading
Crest Factor = 7		−1.0			−1.0			−1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% additional error (0.09dB)										
10mV<V_{IN}≤100mV		6			6			6		kHz
100mV<V_{IN}≤1V		40			40			40		kHz
1V<V_{IN}≤7V		100			100			100		kHz
±3dB Bandwidth										
10mV<V_{IN}≤100mV		50			50			50		kHz
100mV<V_{IN}≤1V		300			300			300		kHz
1V<V_{IN}≤7V		2			2			2		MHz
AVERAGING TIME CONSTANT (Fig. 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15V Supply		±20			±20			±20		V Peak
Signal Range, ±5V Supply		±5			±5			±5		V Peak
Safe Input, All Supply Voltages		±25			±25			±25		V
Input Resistance	13.33	16.7	20.87	13.33	16.7	20.87	13.33	16.7	20.87	kΩ
Input Offset Voltage			±2			±1			±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage		±1	±2		±0.5	±1			±2	mV
vs. Temperature		±0.1			±0.1				±0.2	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ±15V Supplies	**±11**			**±11**			**±11**			V
±5V Supply	±2			±2			±2			V
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)			V
Short Circuit Current		20			20			20		mA
Resistance			0.5			0.5			0.5	Ω
dB OUTPUT (Fig. 13)										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.4	±0.6		±0.2	±0.3		±0.5		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC (Uncompensated, see Fig. 13 for Temperature Compensation)		−0.3			−0.3			−0.35		% of Reading
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	μA
I_{REF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±20			±20			±20		%
Output Resistance		10^8			10^8			10^8		Ω
Voltance Compliance		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5)			$-V_S$ to ($+V_S$ −2.5V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$		$+V_S$ −2.5V	$-V_S$		$+V_S$ −2.5V	$-V_S$		$+V_S$ −2.5V	V
Input Offset Voltage, R_S = 25k			**±4**			**±4**			**±4**	mV
Input Current		60	300		60	300		60	300	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)			V
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance										
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S 5V to 36V, T_{min} to T_{max}		1.2	**2**		1.2	**2**		1.2	**2**	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−55		+150	−55		+150	−55		+150	°C
PACKAGE OPTIONS[5]										
Ceramic DIP (D14A)		AD536AJD			AD536AKD			AD536ASD		
Metal Can (TO-100)		AD536AJH			AD536AKH			AD536ASH		

NOTES

[1]Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.

[2]Error vs. crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.

[3]Input voltages are expressed in volts rms, and error is percent of reading.

[4]With 2k external pulldown resistor.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 14. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input, positive out.

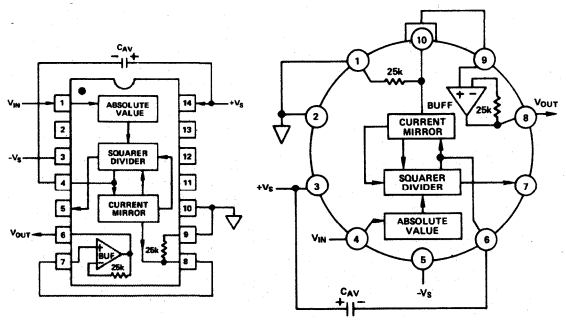


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 249Ω in series with the internal 25kΩ resistor. This will cause a 1% increase in scale factor, which is trimmed out by using R_1 as shown.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range.

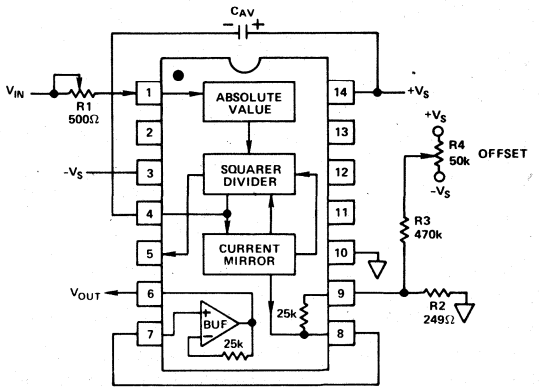


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into pin 10 (pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 14. The load resistor, R_L, is necessary to provide output sink current.

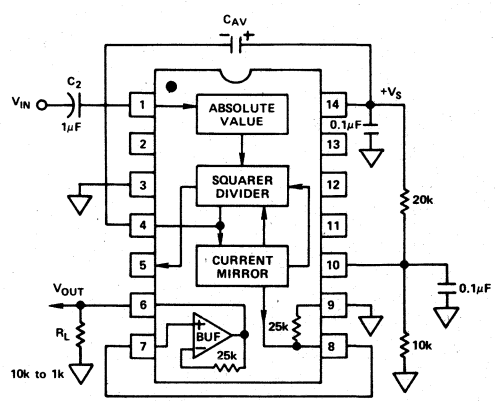


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by an average (or dc) error and some amount of ripple, as demonstrated in Figure 4.

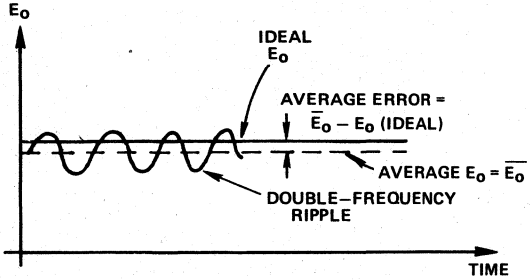


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% dc error above a given frequency. For example, if a 60Hz waveform is to be measured with a dc error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

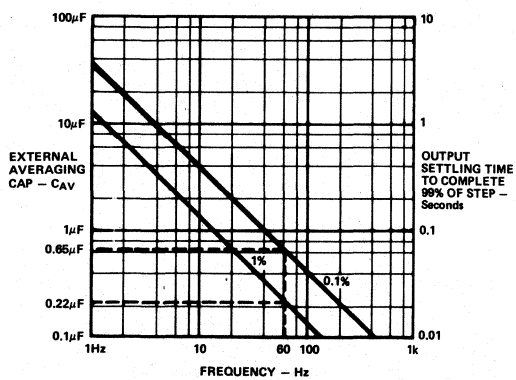


Figure 5. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

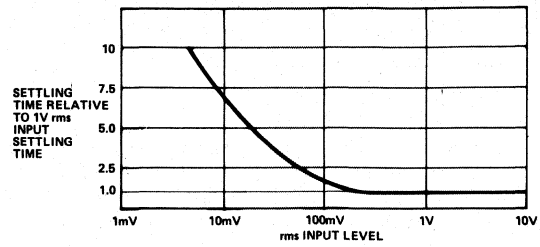


Figure 6. Settling Time vs Input Level

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 2.2μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

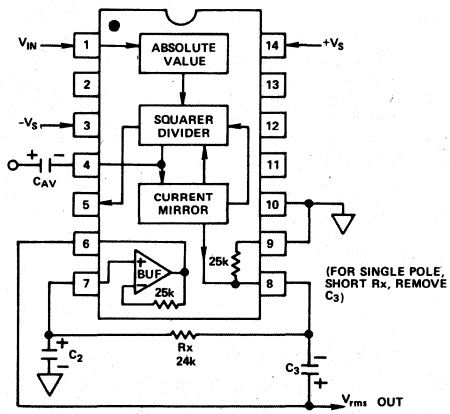


Figure 7. 2 Pole "Post" Filter

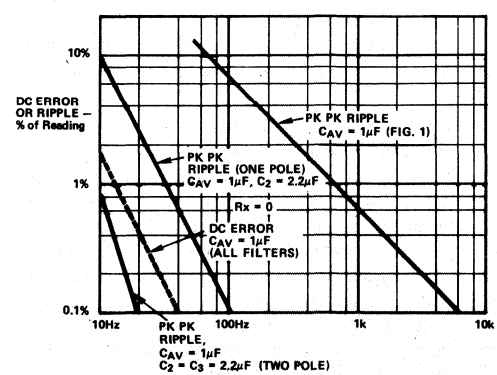


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.}\ [I_1^2/I_4] = I_1\ \text{rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to $-\log V_{IN}$. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

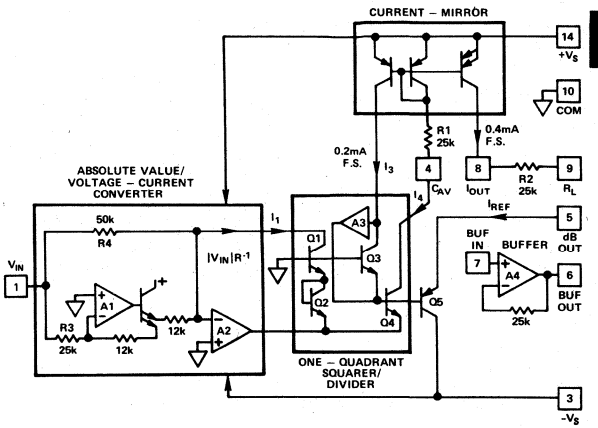


Figure 9. Simplified Schematic

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A, which is not available in any other computing rms circuit, is the logarithmic or decibel output. The internal circuit which computes dB is very accurate and works well over a 60dB range. The connection for dB measurements is shown in Figure 10. The user selects the 0dB level by setting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor, R_3, is available from Tel Labs, Londonderry, NH, type number Q-81. The linear rms output is available at pin 8 with an output impedance of 25kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc
4. Adjust R_2 for dB out = -2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_2 for the proper gain automatically gives the correct temperature compensation.

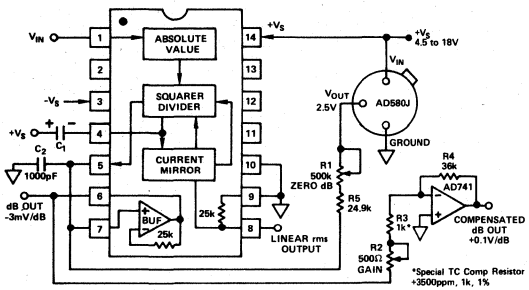


Figure 10. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 100kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to only 6kHz.

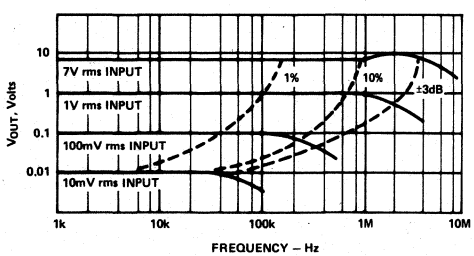


Figure 11. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 12 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 10. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

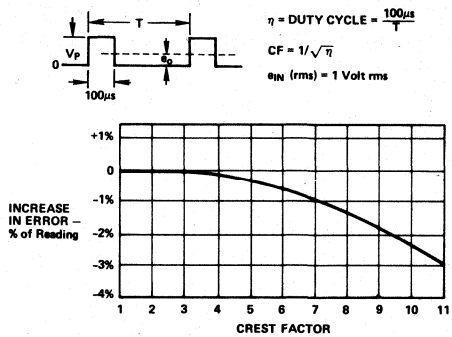


Figure 12. Error vs. Crest Factor

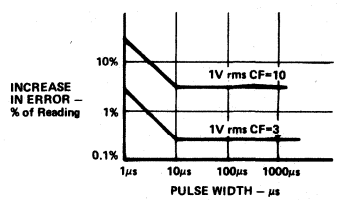


Figure 13. AD536A Error vs. Pulse Width Rectangular Pulse

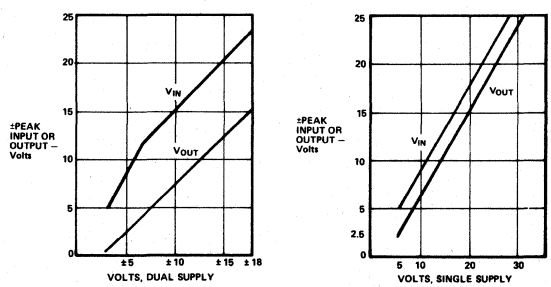


Figure 14. AD536A Input and Output Voltage Ranges vs. Supply

ANALOG DEVICES

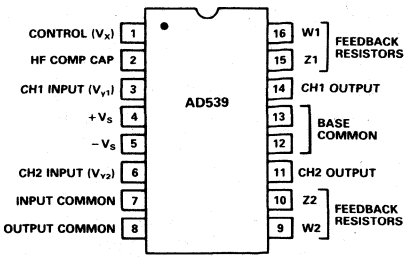
Wideband Dual-Channel Linear Multiplier/Divider

AD539

FEATURES
- Two Quadrant Multiplication/Division
- Two Independent Signal Channels
- Signal Bandwidth of 60MHz (I_{OUT})
- Linear Control-Bandwidth of 5MHz
- Fully-Calibrated, Monolithic Circuit

APPLICATIONS
- Precise AGC and VCA Systems
- Voltage-Controlled Filters
- Video-Signal Processing
- High-Speed Analog Division
- Automatic Signal-Leveling
- Square-Law Gain/Loss Control

AD539 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps in conjunction with the on-chip scaling resistors, accurate multiplication and large output voltages can be achieved, but with a reduction in bandwidth typically to 25MHz.

The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. All versions are packaged in 16-pin DIPs.

DUAL SIGNAL CHANNELS

The signal voltages inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2V with a peak range to ±4.2V (using a negative supply of 7.5V or greater). For video applications where differential phase is critical a reduced input range of ±1 volt is recommended, resulting in a phase variation of typically ±0.2° at 3.579MHz for full gain. The input impedance is typically 400kΩ shunted by 3pF. Signal channel distortion is typically well under 0.1% at 10kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 to +3V FS, +3.2V peak. The input resistance is 500Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3nF allows a bandwidth at mid-gain of about 5MHz. Larger compensation capacitors slow the control channel but improve the high-frequency performance of the signal channels.

FLEXIBLE SCALING

Using either one or two external op amps in conjunction with the on-chip 6kΩ scaling resistors, the output currents (nominally ±1mA FS, ±2.25mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$ or $V_W = -2V_X V_Y$ (where inputs V_X and V_Y and output V_W are expressed in volts), with corresponding full-scale outputs of ±3V, ±6V and ±12V. Alternatively, low-impedance grounded loads can be used to achieve the full signal bandwidth of 60MHz, in which mode the scaling is less accurate.

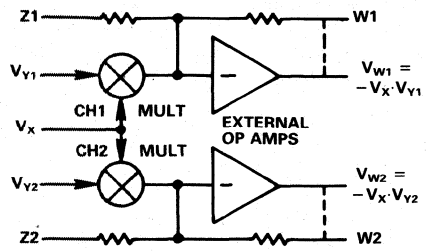
SPECIFICATIONS ($@ T_A = 25°C, V_S = \pm 5V$, unless otherwise specified)

Parameter	Conditions	AD539J			AD539K			AD539S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SIGNAL-CHANNEL DYNAMICS	Reference Figure 6a										
Minimal Configuration											
Bandwidth, −3dB	$R_L = 50\Omega, C_C = 0.01\mu F$	30	60		30	60		30	60		MHz
Maximum Output	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		−10			−10			210		dBm
Feedthrough, f<1MHz	$V_X = 0, V_{Yac} = 1.5V$ rms		−75			−75			−75		dBm
f = 20MHz			−55			−55			−55		dBm
Differential Phase Linearity											
$-1V < V_Ydc < +1V$	f = 3.58MHz, $V_X = +3V$,		±0.2			±0.2			±0.2		Degrees
$-2V < V_Ydc < +2V$	$V_{Yac} = 100mV$		±0.5			±0.5			±0.5		Degrees
Group Delay	Reference Figure 2										
Bandwidth, −3dB (AD509)	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		6			6			6		MHz
Maximum Output	$V_X = +3V, V_{Yac} = 1.5V$ rms		4.5			4.5			4.5		V
Feedthrough, f<100kHz	$V_X = 0, V_{Yac} = 1.5V$ rms		1			1			1		mV rms
Crosstalk (CH1 to CH2)	$V_{Y1} = 1V$ rms, $V_{Y2} = 0$										
	$V_X = +3V$, f<100kHz		−40			−40			−40		dB
Noise, 10Hz to 1MHz	$V_X = +1.5V, V_Y = 0$, Figure 2		200			200			200		$nV/\sqrt{Hz}$
THD + Noise, $V_X = +1V$,	f = 10kHz, $V_{Yac} = 1V$ rms		0.02			0.02			0.02		%
$V_Y = +3V$	f = 10kHz, $V_{Yac} = 1V$ rms		0.04			0.04			0.04		%
Wide Band Two-Channel Multiplier	Figure 2										
Bandwidth, −3dB (LH0032)	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		25			25			25		MHz
Maximum Output Feedthrough, $V_X = +3V$	$V_{Yac} = 1.5V$ rms, f = 3MHz		2.25			2.25			2.25		V rms
$V_X = +0$	$V_{Yac} = 1.0V$ rms, f = 3MHz		14			14			14		mV rms
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3dB	$C_C = 3000pF, V_Xdc = +1.5V$, $V_Xac = 100mV$ rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} & V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	$-V_S > 7V$	±4.2			±4.2			±4.2			V
Input Resistance			400			400			400		kΩ
Bias Current			10	**30**		10	**20**		10	**30**	μA
Offset Voltage	$V_X = +3V, V_Y = 0$		5	**20**		5	**10**		5	**20**	mV
(T_{min} to T_{max})			10		5				15	35	mV
Power Supply Sensitivity	$V_X = +3V, V_Y = 0$		2			2			2		mV/V
CONTROL INPUT, V_X											
Nominal Full-Scale Input			+3.0			+3.0			+3.0		V
Operational Range, Degraded Performance		+3.2			+3.2			+3.2			V
Input Resistance[1]			500			500			500		Ω
Offset Voltage			1	4		1	2		1	4	mV
(T_{min} to T_{max})			3			2			2	5	mV
Power Supply Sensitivity			30			30			30		μV/V
Decibel Gain	(Figure 2)		20			20			20		$\log_{10}(V_X)$
Absolute Gain Error	$V_X = +0.1V$ to $+3.0V$		0.2	**0.4**		0.1	**0.2**		0.2	**0.4**	dB
(T_{min} to T_{max})			0.3			0.15			0.25	0.5	dB
CURRENT OUTPUT[1]											
Full-Scale Output Current	$V_X = +3V, V_Y = \pm 2V$		±1			±1			±1		mA
Peak Output Current	$V_X = +3.3V, V_Y = \pm 5V$	±2	±2.8		±2	±2.8		±2	±2.8		mA
Output Offset Current	$V_X = 0, V_Y = 0$		0.2	2		0.2	2		0.2	2	μA
Output Resistance[1]			1.2			1.2			1.2		kΩ
Scaling Resistors											
CH1	Z1, W1 to CH1		6			6			6		kΩ
CH2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[2]	(Figure 2)										
Multiplier Transfer Function,											
Either Channel			$V_W = -V_X \cdot V_Y / V_Q$			$V_W = -V_X \cdot V_Y / V_Q$			$V_W = -V_X \cdot V_Y / V_Q$		
Multiplier Scaling Voltage, V_Q			1.0			1.0			1.0		V
Accuracy			0.5	**2**		0.5	**1**		0.5	**2**	%
(T_{min} to T_{max})			1			0.5			1.0	3	%
Power Supply Sensitivity			0.03%			0.03			0.03		%/V
Total Multiplication Error[3]	$V_X <= +3V, -2V < V_Y < 2V$		0.6	**2.5**		0.6	**1.5**		2.5	**4**	% FSR
T_{min} to T_{max}			2			1			1		%
Control Feedthrough	$V_X = 0$ to $+3V, V_Y = 0$		15	**60**		15	**30**		15	**60**	mV
T_{min} to T_{max}			30			15			60	120	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°
POWER SUPPLIES											
Operational Range		±4.5		±16.5	±4.5		±16.5	±4.5		±16.5	V
Current Consumption											
$+V_S$			8.5	**10.2**		8.5	**10.2**		8.5	**10.2**	mA
$-V_S$			18.5	**22.2**		18.5	**22.2**		18.5	**22.2**	mA
PACKAGE OPTION[4]											
Ceramic DIP: (D16A)			AD539JD			AD539KD			AD539SD		

NOTES
[1]Resistance value and absolute current outputs subject to 20% tolerance.
[2]Spec assumes the external op amp is trimmed for negligible input offset.
[3]Includes all errors.
[4]See Section 19 for package outline information
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AD539 FUNCTIONAL BLOCK DIAGRAM



CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Q1-Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is 3 times larger than Q2; Q4, Q5 are each 3 times larger than Q3, Q6, and these transistors are twice as large as Q1, Q2. A stable reference current I_{REF} = 1.375mA is produced by a band-gap reference circuit and applied to the common emitter node of a *controlled-cascode* formed by Q1 and Q2. When V_X = 0, all of I_{REF} flows in Q1, due to the action of the high-gain control amplifier which lowers the voltage on the base of Q2. As V_X is raised the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5k. At the full-scale value of V_X (+3V) this fraction is 0.873. Since the bases of Q1, Q4 and Q5 are at ground potential and the bases of Q2, Q3 and Q6 are commoned, all three controlled-cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

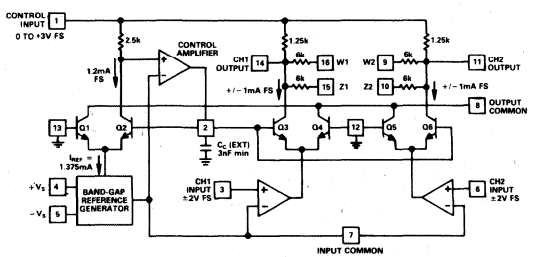


Figure 1. Simplified Schematic of AD539 Multiplier

The signal voltages V_{Y1} and V_{Y2} (generically referred to as V_Y) are first converted to currents by voltage-to-current converters with a g_m of 575μmhos; thus, thc full-scale input of ±2V becomes a current of ±1.15mA, which is superimposed on a bias of 2.75mA, and applied to the common emitter node of controlled cascode Q3-Q4 or Q5-Q6. As just explained, the proportion of this current steered to the output node is linearly dependent on V_X. Thus for full-scale V_X and V_Y inputs, a signal of ±1mA (0.873 × ±1.15mA) and a bias component of 2.4mA (0.873 × 2.75mA) appear at the ouput. The bias component absorbed by the 1.25k resistors also connected to V_X, and resulting the signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board or mounted in a low-profile socket. In the figures used here an open triangle denotes a *direct, short* connection to this ground plane; pins 12 and 13 are especially prone to unwanted signal pick-up. Power supply decoupling capacitors of 0.1μF to 1μF should be connected from pins 4 and 5 to the ground plane. In applications using external high-speed op amps, separate supply decoupling should be used. It is good practice to insert small (10Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3nF. Unless maximum control bandwidth is esssential it is advisable to use a larger value of 0.01μF to 0.1μF to improve the signal channel phase response, high-frequency crosstalk and high-frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2MHz for C_C = 0.01μF, V_X = 1.7V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between pins 1 and 2. Optimum transient response will result when the rise/fall time of V_X are commensurate with the control-channel response time.

V_X should not exceed the specified range of 0 to +3V. The ac gain is zero for V_x<0 but there remains a feedforward path (see Figure 1) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small-signal Schottky diode with its cathode connected to pin 2 and its anode grounded. This constrains the voltage swing on C_C. Above V_X = +3.2V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5V above $+V_S$; the minimum value is 2.5V above $-V_S$. To accommodate the peak specified inputs of ±4.2V the supplies should be nominally +5V and −7.5V. While there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5V can be as high as 535mW and some form of heat-sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider careful attention must be paid to the matter of *scaling*, particularly in computational applications. To be *dimensionally consistent* a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (Figure 2) is

$$V_W = -V_X V_Y / V_Q$$

where the inputs V_X and V_Y, the output V_W and the scaling voltage V_Q are expressed in a consistent unit, usually volts. In this case, V_Q is fixed by the design to be 1V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that *all signals must be expressed in volts*, that is, they are rendered dimensionless by division by (1V).

The accuracy specifications for V_Q allow the use of either of the two feedback resistors supplied with each channel, since these are very closely matched, or they may be used in parallel to half the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y/2.$$

When an external load resistor, R_L, is used the scaling is no longer exact since the internal thin-film resistors, while trimmed to high *ratiometric* accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y/V_Q'$$

where the effective scaling voltage, V_Q' can be calculated for each channel using the formula $V_Q' = V_Q\,(5R_L + 6.25)/R_L$, where R_L is expressed in kilohms. For example, when R_L = 100Ω, V_Q' = 67.5V. Table II provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (output pin 11 or 14 open-circuit), when V_Q' is quite accurately 5V.

BASIC MULTIPLIER CONNECTIONS

Figure 2 shows the connections for the standard two-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where inputs and outputs are expressed in volts (see TRANSFER FUNCTION). At the nominal full-scale inputs of V_X = +3V, V_Y = ±2V the full-scale outputs are ±6V. Depending on the choice of op amp, their supply voltages usually need to be about 2V more than the peak output. Thus, supplies of at least ±8V are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of +3.2V and ±4.2V respectively, when the peak output is ±13.4V. This requires operating the op amps at supplies of ±15V. Under these conditions it is advisable to reduce the supplies to the AD539 to ±7.5V to limit its power dissipation; however, with some form of heat sinking it is permissible to operate the AD539 directly from ±15V supplies.

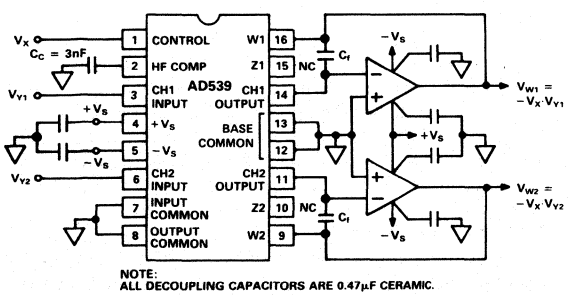


Figure 2. Standard Dual-Channel Multiplier

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10dB at V_X = +3.162V, 0dB at V_X = +1V, −20dB at V_X = +0.1V, and so on. In many ac applications the output offset voltage (for V_X = 0 or V_Y = 0) will not be of major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with V_X = V_Y = 0.

At small values of V_X the offset voltage of the control channel will degrade the gain/loss accuracy. For example, a ±1mV offset uncertainty will cause the nominal 40dB attenuation at V_X = +0.01V to range from 39.2dB to 40.9dB. Figure 3a shows the maximum gain error boundaries based on the guaranteed control-channel offset voltages of ±2mV for the AD539K and ±4mV for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2; alternatively, Z1 and Z2).

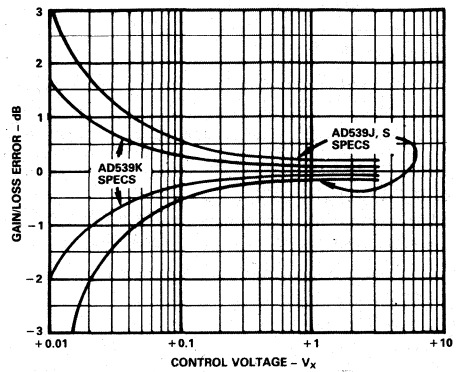


Figure 3a. Maximum ac Gain Error Boundaries

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice the op amp will generate most of the distortion at frequencies above 100kHz. Figure 3b shows typical results at f = 10kHz as a function of V_X with V_Y = 0.5 and 1.5V rms.

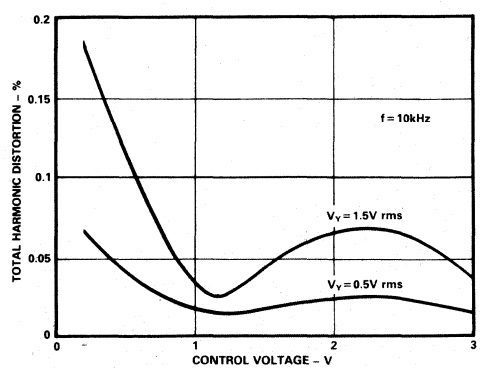


Figure 3b. Total Harmonic Distortion vs. Control Voltage

In some cases it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 1) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at ±3V FS (±6.75V pk), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is ±12V. Another option is to insert a resistor in series with the control-channel input, permitting the use of a large (for example, 0 to +10V) control voltage. A disadvantage of this scheme is the need to

adjust this resistor to accommodate the tolerance of the nominal 500Ω input resistance at pin 1. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal-Channel ac and Transient Response

The HF response is dependent almost entirely on the op amp. The AD509 is a good choice for many applications since it is inexpensive, has good slewing properties and can provide about 6MHz of bandwidth in conjunction with the AD539. Note that the "noise gain" for the op amp in Figure 2 is determined by the value of the feedback resistor (6kΩ) and the 1.25kΩ control-bias resistors (Figure 1). Op amps with provision for external frequency compensation (such as the AD301 and AD518) should be compensated for a closed-loop gain of 6.

Figure 4a shows the response of the configuration of Figure 2 using AD509 op amps, with the small capacitor C_F adjusted for 1dB peaking at $V_X = +1V$. The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see GENERAL RECOMMENDATIONS). For these curves, V_Y is 1V rms; other conditions are listed in Table I. The −3dB bandwidth is essentially constant at 6MHz for $V_X = +0.01V$ to $V_X = +1V$. At $V_X = +3.162V$ (chosen to result in 10dB gain) the apparent slight loss of bandwidth is due to the onset of slew-rate limitations

	AD544	AD509	ADLH0032
Op Amp Supply Voltages	±15V	±10V	±10V
Op Amp Compensation Cap.	None	None	1-5pF (Pins 2, 3)
Feedback Capacitor, C_F	None	2-5pF	1-4pF
−3dB Bandwidth, $V_X = +1V$	400kHz	6MHz	25MHz
Load Capacitance	<1nF	<100pF	<100pF
HF Feedthrough,			
$V_X = -0.01V$, f = 5MHz	–	−75dB	−70dB
rms Output Noise,			
$V_X = +1V$, BW 10Hz-10kHz	50μV	50μV	30μV
$V_X = +1V$, BW 10Hz-5MHz	220μV	550μV	500μV

In all cases, 0.47μF ceramic supply-decoupling capacitors were used at each IC pin, the AD539 supplies were ±5V and the control-compensation capacitor C_C was 3nF.

Table I. Summary of Operating Conditions and Performance for Standard Multiplier Connections

(peak output is then ±4.5V). The corresponding pulse response is shown in Figure 4b for a signal input V_Y of ±1V and two values of V_X (+0.1V and +3V).

For wide-band applications a hybrid op amp can be used. Figure 5a shows the HF response using the ADLH0032, with V_Y = 1V rms and other conditions as shown in Table I. C_F was adjusted for 1dB peaking at $V_X = +1V$; the −3dB bandwidth exceeds 25MHz. The effect of signal feedthrough on the response becomes apparent at $V_X = +0.01V$. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control-channel offset is exceeded and the dc gain is reliably

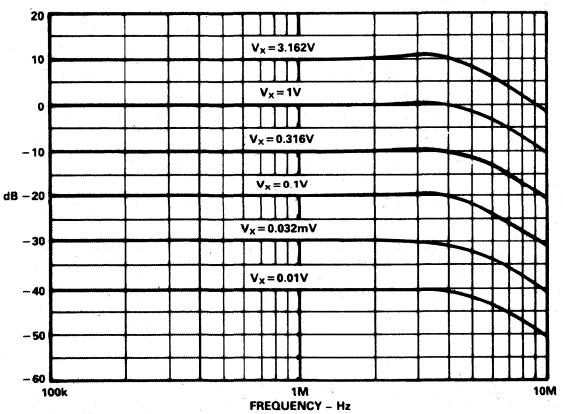


Figure 4a. Response in Standard Configuration Using AD509 Output Op Amp

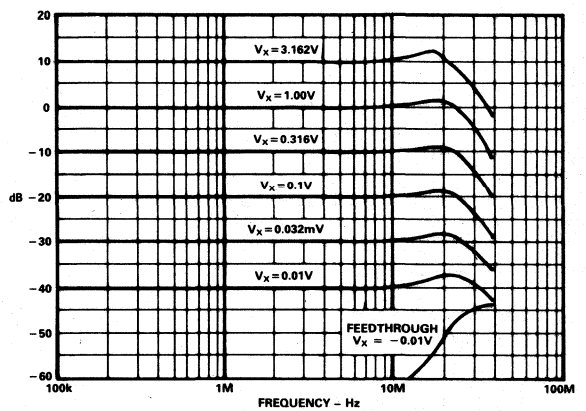
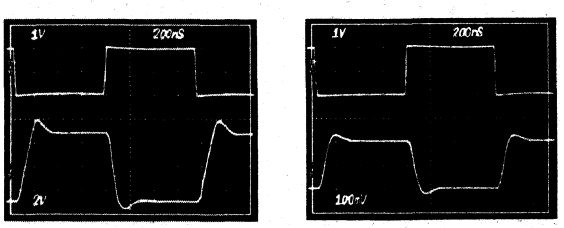
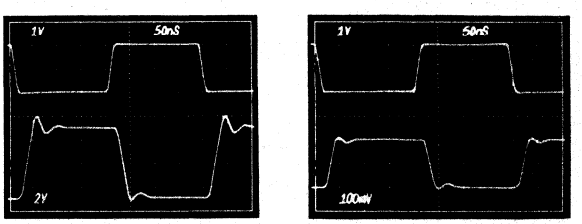


Figure 5a. Multiplier HF Response Using ADLH0032 Op Amps



$V_X = +3V$ $V_X = +0.1V$

Figure 4b. Multiplier Pulse Response Using AD509 Op Amps



$V_X = +3V$ $V_X = +0.1V$

Figure 5b. Multiplier Pulse Response Using ADLH0032 Op Amps

zero. Measurements show that the feedthrough can be held to −90dB relative to full output at low frequencies and to −60dB up to 20MHz with careful in board layout. The corresponding pulse response is shown in Figure 5b for a signal input of V_Y of ±1V and two values of V_X (+3V and +0.1V).

Minimal Wide-Band Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1mA FS, ±2.25mA pk, into short-circuit loads) are shunted by their source resistance of 1.25kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10MHz the gains are typically within ±0.025dB (measured using precision 50Ω load resistors) and the phase difference within ±0.1°.

For a given load resistance the output power can be quadrupled by using both channels in parallel, as shown in Figure 6a. The small-signal silicon diode D connected between ground and pins 12 and 13 provides extra voltage compliance at the output nodes in the negative direction (to −1V at 25°C); it is not required if the output swing does not exceed −300mV. Table II compares performance for various load resistances, using this configuration.

Figure 6b shows the HF response in this configuration with the AD539 in a carefully-shielded 50Ω test-environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response. In many applications *phase linearity* over frequency is important. Figure 6c shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10MHz, for V_X = +3V; the peak deviation is slightly more than 1°. *Differential phase linearity* (the stability of phase over the signal window at a fixed frequency) is shown in Figure 6d for f = 3.579MHz and various values of V_X. The most rapid variation occurs for V_Y above +1V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

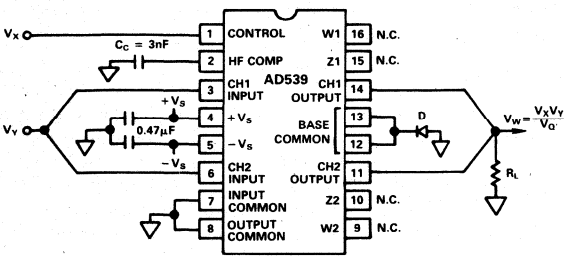


Figure 6a. Minimal Single-Channel Multiplier

Load Resistance	50Ω	75Ω	100Ω	150Ω	600Ω	O/C
FS Output Voltage	±92.6mV	±134mV	±172mV	±242mV	±612mV	±1V
	65.5mV rms	94.7mV rms	122mV rms	171mV rms	433mV rms	*
FS Output-Power in Load	0.086mW	0.12mW	0.15mW	0.195mW	0.312mW	–
	−10.5dBm	−9.2dBm	−8.3dBm	−7.1dBm	−5.05dBm	–
Pk Output Voltage	±210mV	±300mV	±388mV	±544mV	±1V	±1V
	148mV rms	212mV rms	274mV rms	385mV rms	*	*
Pk Output-Power in Load	0.44mW	0.6mW	0.75mW	1mW	±1V	±1V
	−7dBm	−4.4dBm	−2.5dBm	0dBm	*	*
Effective Scaling Voltage, V_Q'	67.5V	46.7V	36.3V	25.8V	10.2V	5V

*Peak negative voltage swing limited by output compliance.

Table II. Summary of Performance for Minimal Configuration

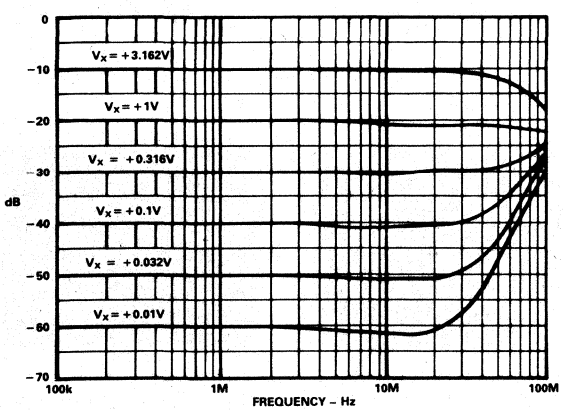


Figure 6b. HF Response in Minimal Configuration

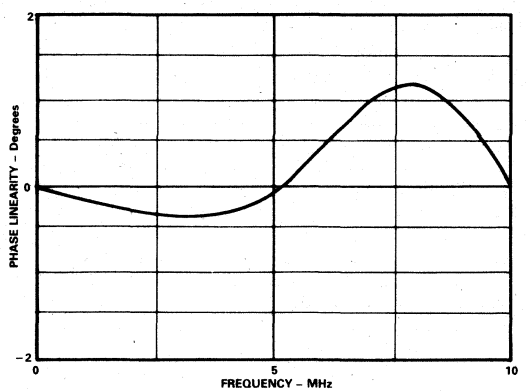


Figure 6c. Phase Linearity Error in Minimal Configuration

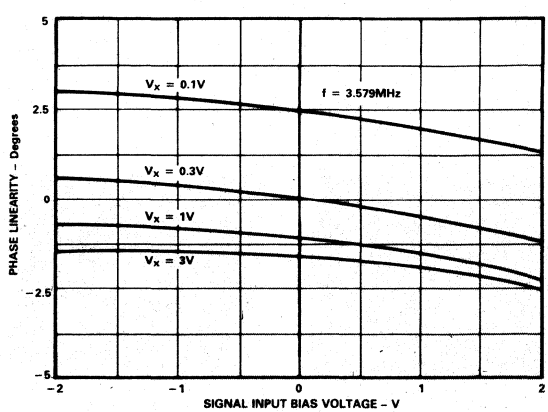


Figure 6d. Differential Phase Linearity in Minimal Configuration for a Typical Device

Differential Configurations

When only one signal channel must be handled it is often advantageous to use the channels differentially. By subtracting the CH1 and CH2 outputs any residual transient control feedthrough

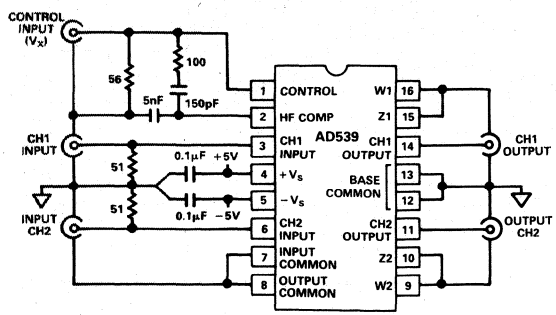


Figure 7a. High-Speed Differential Configuration

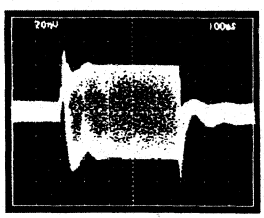


Figure 7b. Control Feedthrough One Channel of Figure 7a

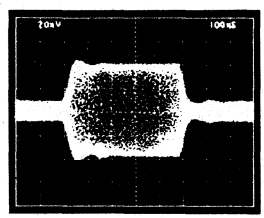


Figure 7c. Control Feedthrough Differential Mode, Figure 7a

is virtually eliminated. Figure 7a shows a minimal configuration where it is assumed that the host system uses differential signals and a 50Ω environment throughout. This figure also shows a recommended control-feedforward network to improve large-signal response time. The control feedthrough glitch is shown in Figure 7b, where the input was applied to CH1 and only the output of CH1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 7c. The envelope rise-time is of the order of 40ns.

Lower distortion results when CH1 and CH2 are driven by *complementary* inputs and the outputs are utilized differentially, using a circuit such as Figure 8a. Resistors R1 and R2 should have a value in the range 100 to 1000Ω. They minimize a secondary distortion mechanism caused by a collector-modulation effect in the controlled cascodes (see CIRCUIT DESCRIPTION) by keeping the voltage-swing at the outputs to an acceptable level. Figure 8b shows the improvement in distortion over the standard configuration (compare Figure 3b). Note that the Z nodes (pins

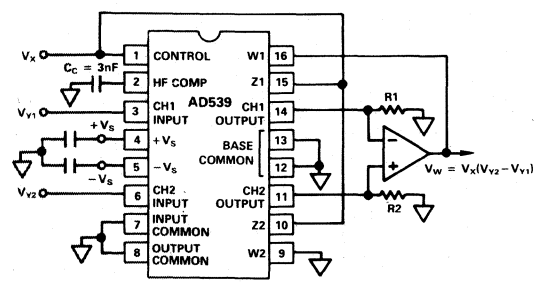


Figure 8a. Low-Distortion Differential Configuration

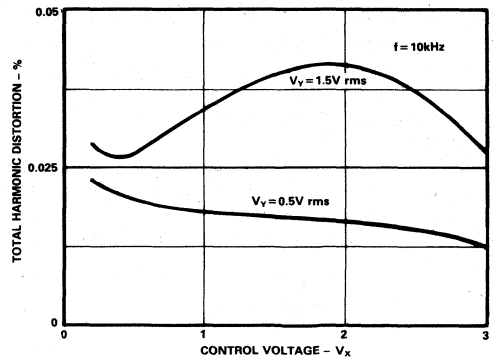


Figure 8b. Distortion in Differential Mode Using ADLH0032

10 and 15) are returned to the control input; this prevents the early onset of output-transistor saturation.

Even lower distortion (0.01%, or −80dB) has been measured using two output op amps connected as virtual-ground current-summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the CH1 op amp to the Z node of CH2. In this way, the net input to the CH2 op amp is the difference signal, and the low-distortion resultant appears as its output.

Square-Law Voltage Controlled Amplifier

The signal channels of the AD539 can be cascaded to achieve a

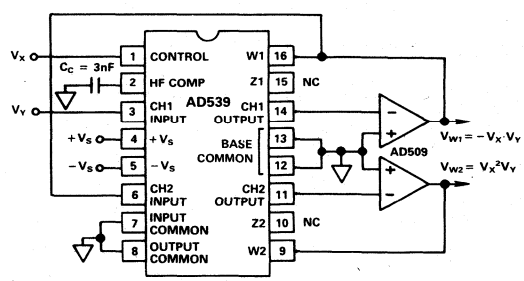


Figure 9a. Square-Law, Voltage-Controlled Amplifier

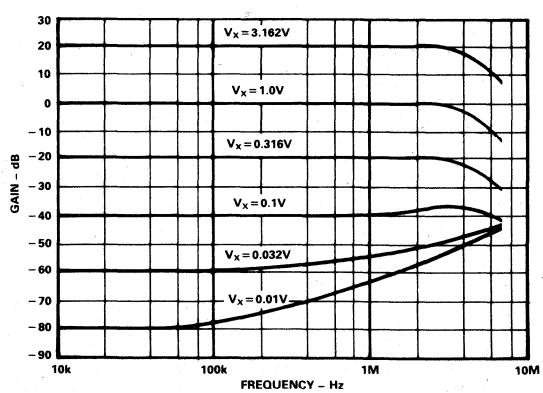


Figure 9b. HF Response of Square-Law Amplifier

much wider gain range with a square-law control characteristic. Figure 9a shows the connections and Figure 9b is the measured HF response using AD509 op amps with no additional HF compensation. Note that the gain varies from −80dB for V_X = +0.01V to +20dB at V_X = +3.162V, which is a 100dB control range. Since V_X is never very small, the gain or loss is well-defined over the entire range.

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wide-band wide gain-range applications, with the advantage of dual-channel operation. Figure 10a shows the simplest connections for division with a transfer function of

$$V_Y = -V_Q V_W / V_X$$

Recalling that the nominal value of V_Q is 1V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for V_X = +1V and a gain of 40dB when V_X =

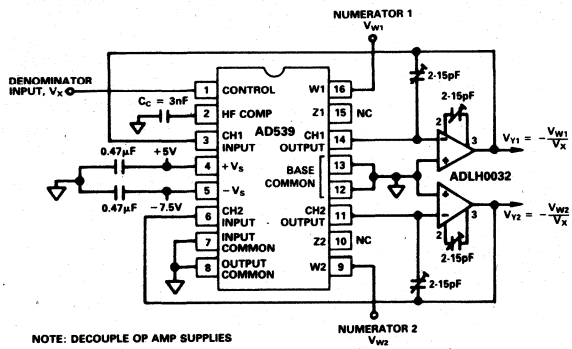


Figure 10a. Two-Channel Divider with 1V Scaling

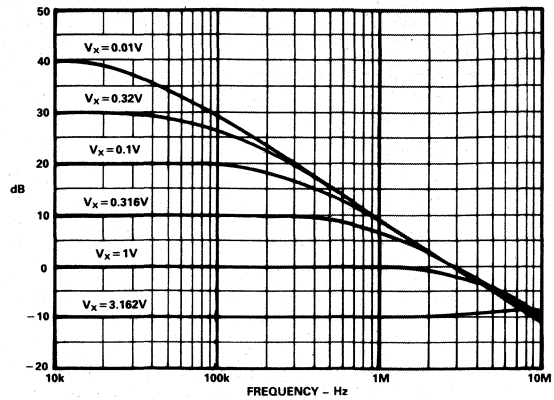


Figure 10b. HF Response of Figure 10a Divider

+0.01V. The output swing is limited to ±2V nominal full-scale and ±4.2V peak (using a $-V_S$ supply of at least 7.5V for the AD539). Since the maximum *loss* is 10dB (at V_X = 3.162V), it follows that the maximum input to V_W should be ±6.3V (4.4V rms) for low distortion applications, and no more than ±13.4V (9.5V rms) to avoid clipping. Note that offset adjustment will be needed for the op amps to maintain accurate dc levels at the output in high gain applications: the "noise gain" is $6V/V_X$ or 600 at V_X = +0.01V.

The gain-magnitude response for this configuration using the ADLH0032 op amps with nominally 12pF compensation (pins 2 to 3) and C_F = 7pF is shown in Figure 10b. Since there is some manufacturing variation in the HF response of the op amps, and load conditions will also affect the response, these capacitors should be adjustable: 5-15pF is recommended for both positions. The bandwidth in this configuration is nominally 17MHz at V_X = +3.162V, 4.5MHz at V_X = +1V, 350kHz at V_X = +0.1V and 35kHz at V_X = +0.01V. The general recommendations regarding the use of a good ground plane and power-supply decoupling should be carefully observed.

ANALOG DEVICES

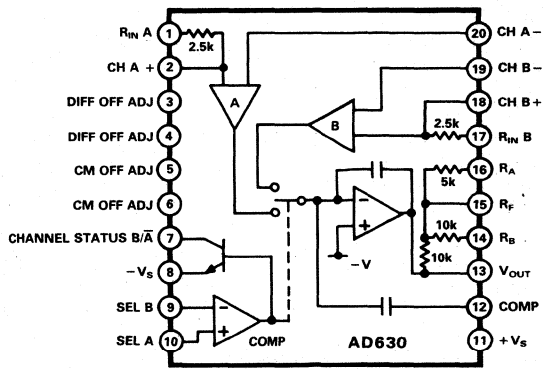
Balanced Modulator/Demodulator

AD630

FEATURES

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth

AD630 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

SPECIFICATIONS (@ +25°C and $\pm V_S$ = ±15V unless otherwise specified)

Model	AD630J Min	AD630J Typ	AD630J Max	AD630K Min	AD630K Typ	AD630K Max	Units
GAIN							
Open Loop Gain	**90**	110		**100**	120		dB
±1, ±2 Closed Loop Gain Error		0.1				**0.05**	%
Closed Loop Gain Match		0.1				**0.05**	%
Closed Loop Gain Drift		2			2		ppm°C
CHANNEL INPUTS							
V_{IN} Operational Limit[1]		$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$		Volts
Input Offset Voltage			**500**			**100**	μV
Input Offset Voltage							
T_{min} to T_{max}			**800**			**160**	μV
Input Bias Current		100	**300**		100	**300**	nA
Input Offset Current		10	**50**		10	**50**	nA
Channel Separation @ 10kHz		100			100		dB
COMPARATOR							
V_{IN} Operational Limit[1]		$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$		Volts
Switching Window			**±1.5**			**±1.5**	mV
Switching Window							
T_{min} to T_{max}			**±2.0**			**±2.0**	mV
Input Bias Current		100	**300**		100	**300**	nA
Response Time (−5mV to +5mV step)		200			200		ns
Channel Status							
I_{SINK} @ $V_{OL} = -V_S + 0.4V$[2]	**1.6**			**1.6**			mA
Pull-Up Voltage			$(-V_S + 33V)$			$(-V_S + 33V)$	Volts
DYNAMIC PERFORMANCE							
Unity Gain Bandwidth		2			2		MHz
Slew Rate[3]		45			45		V/μs
Settling Time to 0.1% (20V step)		3			3		μs
OPERATING CHARACTERISTICS							
Common-Mode Rejection	**85**	105		**90**	110		dB
Power Supply Rejection	**90**	110		**90**	110		dB
Supply Voltage Range	**±5**		±16.5	**±5**		±16.5	Volts
Supply Current		4	5		4	5	mA
OUTPUT VOLTAGE, @ $R_L = 2k\Omega$							
T_{min} to T_{max}	**±10**			**±10**			Volts
Output Short Circuit Current		25			25		mA
TEMPERATURE RANGES							
Rated Performance – N Package	0		+70	0		+70	°C
D Package		N/A			N/A		°C
PACKAGE OPTIONS[4]							
Plastic DIP – (N20A)		AD630JN			AD630KN		
Ceramic DIP – (D20A)		–			–		

NOTES

[1] If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2] I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.

[3] Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/μs.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

SPECIFICATIONS (@ +25°C and $\pm V_S$ = ±15V unless otherwise specified)

Model	AD630A			AD630B			AD630S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Open Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed Loop Gain Error		0.1				0.05		0.1		%
Closed Loop Gain Match		0.1				0.05		0.1		%
Closed Loop Gain Drift		2			2			2		ppm°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			Volts
Input Offset Voltage			500			100			500	µV
Input Offset Voltage T_{min} to T_{max}			800			160			1000	µV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation @ 10kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.3V)$			Volts
Switching Window			±1.5			±1.5			±1.5	mV
Switching Window T_{min} to T_{max}			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (−5mV to +5mV step)		200			200			200		ns
Channel Status										
I_{SINK} @ $V_{OL} = -V_S + 0.4V$[2]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[3]		45			45			45		V/µs
Settling Time to 0.1% (20V step)		3			3			3		µs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ R_L = 2kΩ										
T_{min} to T_{max}	±10			±10			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance – N Package		N/A			N/A			N/A		°C
D Package	−25		+85	−25		+85	−55		+125	°C
PACKAGE OPTIONS[4]										
Plastic DIP – (N20A)		–			–			–		
Ceramic DIP – (D20A)		AD630AD			AD630BD			AD630SD		

NOTES

[1] If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2] I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.

[3] Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/µs.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	600mW
Output Short Circuit to Ground	Indefinite
Storage Temperature, Ceramic Package	−65°C to +150°C
Storage Temperature, Plastic Package	−55°C to +125°C
Lead Temperature, 10 sec. Soldering	+300°C
Max Junction Temperature	+150°C

Typical Performance Characteristics

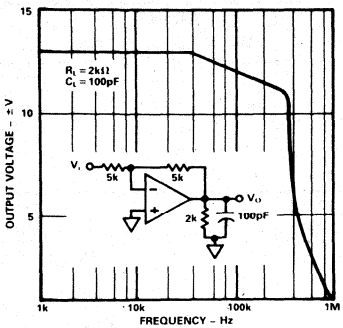


Figure 1. Output Voltage vs. Frequency

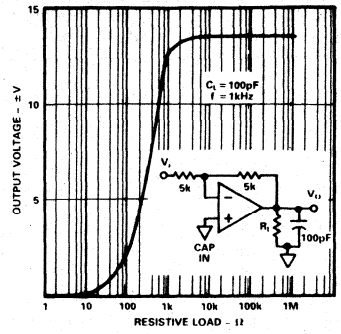


Figure 2. Output Voltage vs. Resistive Load

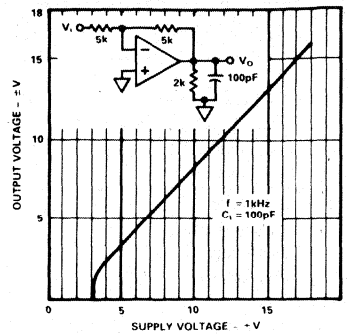


Figure 3. Output Voltage Swing vs. Supply Voltage

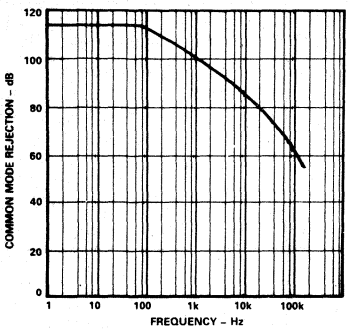


Figure 4. Common Mode Rejection vs. Frequency

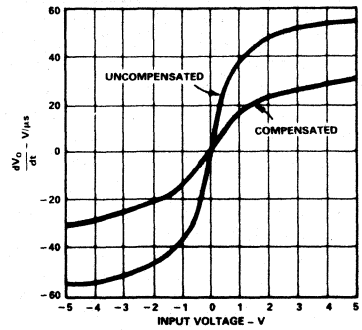


Figure 5. $\frac{dV_O}{dt}$ vs. Input Voltage

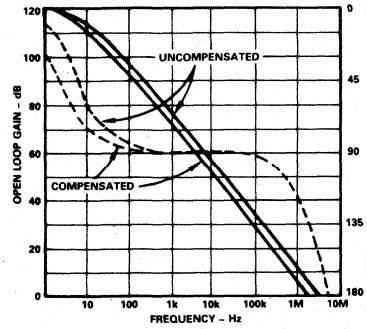


Figure 6. Gain and Phase vs. Frequency

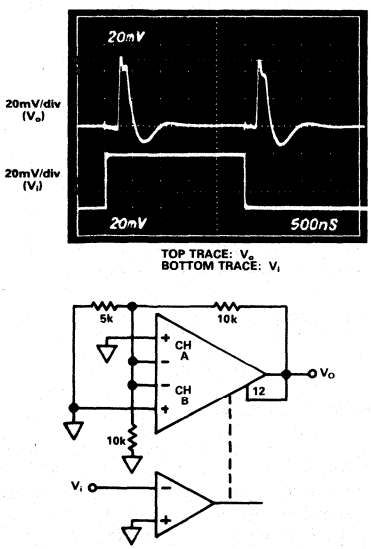


Figure 7. Channel-to-Channel Switch-Settling Characteristic

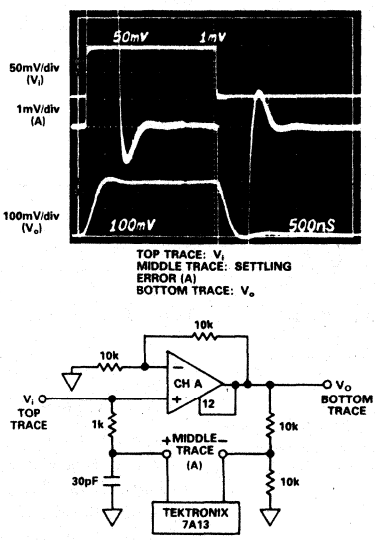


Figure 8. Small Signal Noninverting Step Response

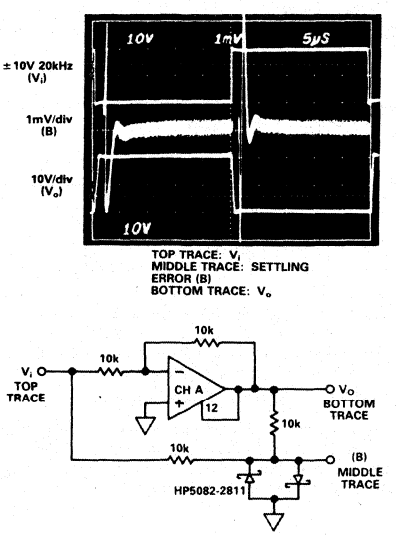


Figure 9. Large Signal Inverting Step Response

TWO WAYS TO LOOK AT THE AD630

Figure 10 is a functional block diagram of the AD630 which also shows the pin connections of the internal functions. An alternative architectural diagram is shown in Figure 11. In this diagram, the individual A and B channel pre-amps, the switch, and the integrator-output amplifier are combined in a single op amp. This amplifier has two differential input channels, only one of which is active at a time.

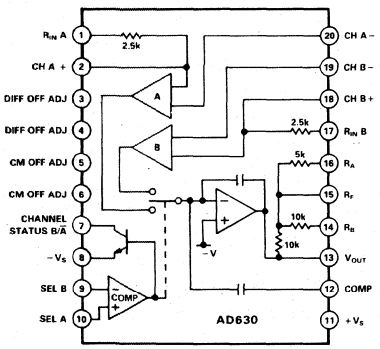


Figure 10. Functional Block Diagram

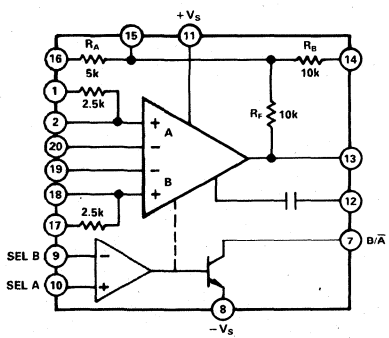


Figure 11. Architectural Block Diagram

HOW THE AD630 WORKS

The basic mode of operation of the AD630 may be more easy to recognize as two fixed gain stages which may be inserted into the signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic modulation/demodulation function. The AD630 is unique in that it includes Laser-Wafer-Trimmed thin-film feedback resistors on the monolithic chip. The configuration shown below yields a gain of ± 2 and can be easily changed to ± 1 by shifting R_B from its ground connection to the output.

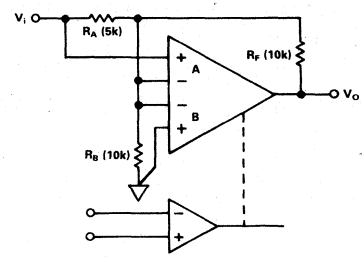


Figure 12. AD630 Symmetric Gain (± 2)

The comparator selects one of the two input stages to complete an operational feedback connection around the AD630. The de-selected input is off and has negligible effect on the operation.

When channel B is selected, the resistors R_A and R_F are connected for inverting feedback as shown in the inverting gain configuration diagram in Figure 13. The amplifier has sufficient loop gain to minimize the loading effect of R_B at the virtual ground produced by the feedback connection. When the sign of the comparator input is reversed, input B will be de-selected and A will be selected. The new equivalent circuit will be the noninverting gain configuration shown below. In this case R_A will appear across the op-amp input terminals, but since the amplifier drives this difference voltage to zero the closed loop gain is unaffected.

The two closed loop gain magnitudes will be equal when $R_F/R_A = 1 + R_F/R_B$, which will result from making R_A equal to $R_F R_B/(R_F + R_B)$ the parallel equivalent resistance of R_F and R_B.

The 5k and the two 10k resistors on the AD630 chip can be used to make a gain of two as shown here. By paralleling the 10k resistors to make R_F equal 5k and omitting R_B the circuit can be programmed for a gain of ± 1 (as shown in Figure 19a). These and other configurations using the on chip resistors present the inverting inputs with a 2.5k source impedance. The more complete AD630 diagrams show 2.5k resistors available at the noninverting inputs which can be conveniently used to minimize errors resulting from input bias currents.

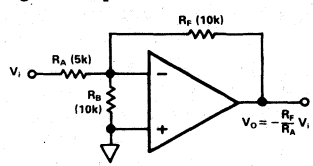


Figure 13. Inverting Gain Configuration

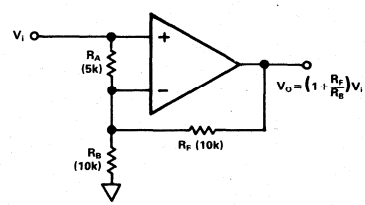


Figure 14. Noninverting Gain Configuration

CIRCUIT DESCRIPTION

The simplified schematic of the AD630 is shown in Figure 15. It has been subdivided into three major sections, the comparator, the two input stages and the output integrator. The comparator consists of a front end made up of Q52 and Q53, a flip-flop load formed by Q3 and Q4, and two current steering switching cells Q28, Q29 and Q30, Q31. This structure is designed so that a differential input voltage greater than 1.5mV in magnitude

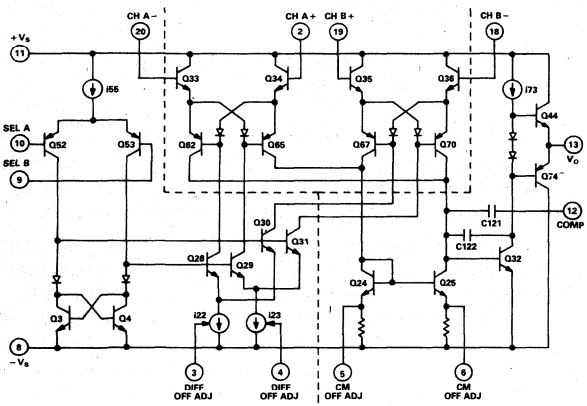


Figure 15. AD630 Simplified Schematic

applied to the comparator inputs will completely select one of the switching cells. The sign of this input voltage determines which of the two switching cells is selected.

The collectors of each switching cell connect to an input transconductance stage. The selected cell conveys bias currents i_{22} and i_{23} to the input stage it controls causing it to become active. The deselected cell blocks the bias to its input stage which, as a consequence, remains off.

The structure of the transconductance stages is such that they present a high impedance at their input terminals and draw no bias current when deselected. The deselected input does not interfere with the operation of the selected input insuring maximum channel separation.

Another feature of the input structure is that it enhances the slew rate of the circuit. The current output of the active stage follows a quasi-hyperbolic-sine relationship to the differential input voltage. This means that the greater the input voltage, the harder this stage will drive the output integrator, and hence, the faster the output signal will move. This feature helps insure rapid, symmetric settling when switching between inverting and noninverting closed loop configurations.

The output section of the AD630 includes a current mirror-load (Q24 and Q25), an integrator-voltage gain stage (Q32), and a complementary output buffer (Q44 and Q74). The outputs of both transconductance stages are connected in parallel to the current mirror. Since the deselected input stage produces no output current and presents a high impedance at its outputs, there is no conflict. The current mirror translates the differential output current from the active input transconductance amplifier into single ended form for the output integrator. The complementary output driver then buffers the integrator output to produce a low impedance output.

OTHER GAIN CONFIGURATIONS

Many applications require switched gains other than the ±1 and ±2 which the self-contained applications resistors provide. The AD630 can be readily programmed with 3 external resistors over a wide range of positive and negative gain by selecting R_B and R_F to give the noninverting gain $1 + R_F/R_B$ and subsequently R_A to give the desired inverting gain. Note that when the inverting magnitude equals the noninverting magnitude, the value of R_A is found to be $R_B R_F/(R_B + R_F)$. That is, R_A should equal the parallel combination of R_B and R_F to match positive and negative gain.

The feedback synthesis of the AD630 may also include reactive impedance. The gain magnitudes will match at all frequencies if the A impedance is made to equal the parallel combination of the B and F impedances. Essentially the same considerations apply to the AD630 as to conventional op-amp feedback circuits. Virtually any function which can be realized with simple non-inverting "L network" feedback can be used with the AD630. A common arrangement is shown in Figure 16. The low frequency gain of this circuit is 10. The response will have a pole (−3dB) at a frequency $f \simeq 1/(2\pi 100k\Omega C)$ and a zero (3dB from the high frequency asymptote) at about 10 times this frequency. The 2k resistor in series with each capacitor mitigates the loading effect on circuitry driving this circuit, eliminates stability problems, and has a minor effect on the pole-zero locations.

As a result of the reactive feedback, the high frequency components of the switched input signal will be transmitted at unity gain

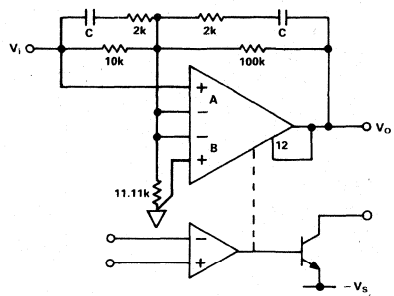


Figure 16. AD630 with External Feedback

while the low frequency components will be amplified. This arrangement is useful in demodulators and lock-in amplifiers. It increases the circuit dynamic range when the modulation or interference is substantially larger than the desired signal amplitude. The output signal will contain the desired signal multiplied by the low frequency gain (which may be several hundred for large feedback ratios) with the switching signal and interference superimposed at unity gain.

SWITCHED INPUT IMPEDANCE

The noninverting mode of operation is a high input impedance configuration while the inverting mode is a low input impedance configuration. This means that the input impedance of the circuit undergoes an abrupt change as the gain is switched under control of the comparator. If gain is switched when the input signal is not zero, as it is in many practical cases, a transient will be delivered to the circuitry driving the AD630. In most applications, this will require the AD630 circuit to be driven by a low impedance source which remains "stiff " at high frequencies. Generally this will be a wideband buffer amplifier.

FREQUENCY COMPENSATION

The AD630 combines the convenience of internal frequency compensation with the flexibility of external compensation by means of an optional self-contained compensation capacitor.

In gain of ±2 applications the noise gain which must be addressed for stability purposes is actually 4. In this circumstance, the phase margin of the loop will be on the order of 60° without the optional compensation. This condition provides the maximum bandwidth and slew-rate for closed-loop gains of |2| and above.

When the AD630 is used as a multiplexer, or in other configurations where one or both inputs are connected for unity gain feedback, the phase margin will be reduced to less than 20°. This may be acceptable in applications where fast slewing is a first priority, but the transient response will not be optimum. For these applications, the self-contained compensation capacitor may be added by connecting pin 12 to pin 13. This connection reduces the closed loop bandwidth somewhat, and improves the phase margin.

For intermediate conditions, such as gain of ±1 where loop attenuation is 2, use of the compensation should be determined by whether bandwidth or settling response must be optimized. The optional compensation should also be used when the AD630 is driving capacitive loads or whenever conservative frequency compensation is desired.

OFFSET VOLTAGE NULLING

The offset voltages of both input stages and the comparator have been pre-trimmed so that external trimming will only be required in the most demanding applications. The offset adjustment of the two input channels is accomplished by means of a differential and common mode scheme. This facilitates fine adjustment of system errors in switched gain applications. With system input tied to 0V, and a switching or carrier waveform applied to the comparator, a low level square wave will appear at the output. The differential offset adjustment pot can be used to null the amplitude of this square wave (pins 3 and 4). The common mode offset adjustment can be used to zero the residual dc output voltage (pins 5 and 6). These functions should be implemented using 10k trim pots with wipers connected directly to pin 8 as shown in Figures 19a and 19b.

CHANNEL STATUS OUTPUT

The channel status output, pin 7, is an open collector output referenced to $-V_S$ which can be used to indicate which of the two input channels is active. The output will be active (pulled low) when channel A is selected. This output can also be used to supply positive feedback around the comparator. This produces hysteresis which serves to increase noise immunity. Figure 17 shows an example of how hysteresis may be implemented. Note that the feedback signal is applied to the inverting (−) terminal of the comparator to achieve positive feedback. This is because the open collector channel status output inverts the output sense of the internal comparator.

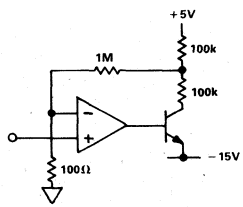


Figure 17. Comparator Hysteresis

The channel status output may be interfaced with TTL inputs as shown in Figure 18. This circuit provides appropriate level shifting from the open-collector AD630 channel status output to TTL inputs.

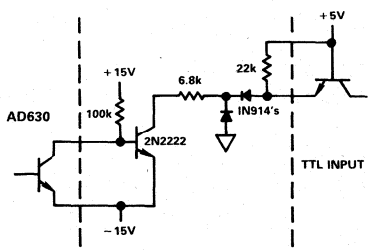


Figure 18. Channel Status – TTL Interface

APPLICATIONS:
BALANCED MODULATOR

Perhaps the most commonly used configuration of the AD630 is the balanced modulator. The application resistors provide precise symmetric gains of ±1 and ±2. The ±1 arrangement is shown in Figure 19a and the ±2 arrangement is shown in Figure 19b. These cases differ only in the connection of the 10k feedback resistor (pin 14) and the compensation capacitor (pin 12). Note the use of the 2.5kΩ bias current compensation resistors in these examples. These resistors perform the identical function in the ±1 gain case. Figure 20 demonstrates the performance of the AD630 when used to modulate a 100kHz square wave carrier with a 10kHz sinusoid. The result is the double sideband suppressed carrier waveform.

These balanced modulator topologies accept two inputs, a signal (or modulation) input applied to the amplifying channels, and a reference (or carrier) input applied to the comparator.

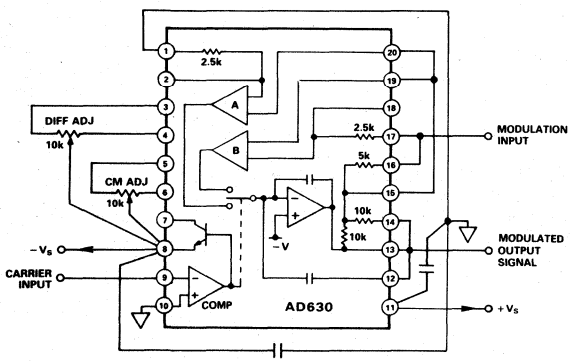


Figure 19a. AD630 Configured as a Gain-of-One Balanced Modulator

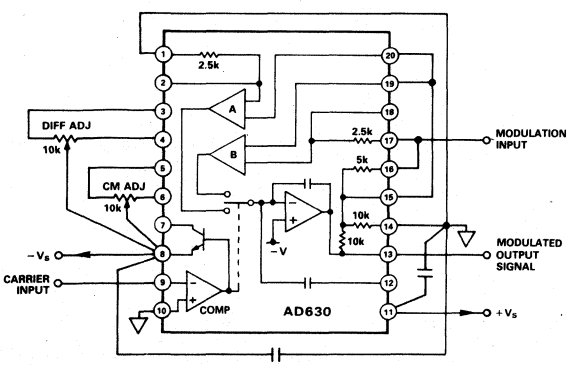


Figure 19b. AD630 Configured as a Gain-of-Two Balanced Modulator

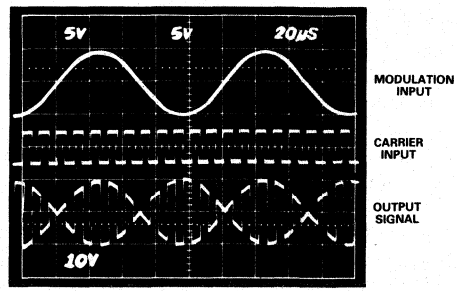


Figure 20. Gain-of-Two Balanced Modulator Sample Waveforms

BALANCED DEMODULATOR

The balanced modulator topology described above will also act as a balanced demodulator if a double sideband suppressed carrier waveform is applied to the signal input and the carrier signal is applied to the reference input. The output under these circumstances will be the baseband modulation signal. Higher order carrier components will also be present which can be removed with a low-pass filter. Other names for this function are synchronous demodulation and phase-sensitive detection.

PRECISION PHASE COMPARATOR

The balanced modulator topologies of Figures 19a and 19b can also be used as precision phase comparators. In this case, an ac waveform of a particular frequency is applied to the signal input and a waveform of the same frequency is applied to the reference input. The dc level of the output (obtained by low pass filtering) will be proportional to the signal amplitude and phase difference between the input signals. If the signal amplitude is held constant, then the output can be used as a direct indication of the phase. When these input signals are 90° out of phase, they are said to be in quadrature and the AD630 dc output will be zero.

PRECISION RECTIFIER-ABSOLUTE VALUE

If the input signal is used as its own reference in the balanced modulator topologies, the AD630 will act as a precision rectifier. The high frequency performance will be superior to that which can be achieved with diode feedback and op amps. There are no diode drops which the op amp must "leap over" with the commutating amplifier.

LVDT SIGNAL CONDITIONER

Many transducers function by modulating an ac carrier. A Linear Variable Differential Transformer (LVDT) is a transducer of this type. The amplitude of the output signal corresponds to core displacement. Figure 21 shows an accurate synchronous demodulation system which can be used to produce a dc voltage which corresponds to the LVDT core position. The inherent precision and temperature stability of the AD630 reduce demodulator drift to a second order effect.

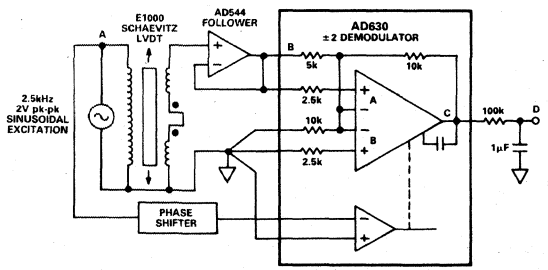


Figure 21. LVDT Signal Conditioner

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

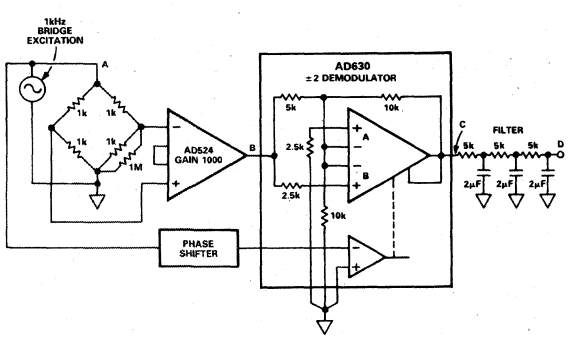


Figure 22. AC Bridge System

Figure 22 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper-middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 3.2mV change in the low pass filtered dc output, well above the RTO drifts and noise.

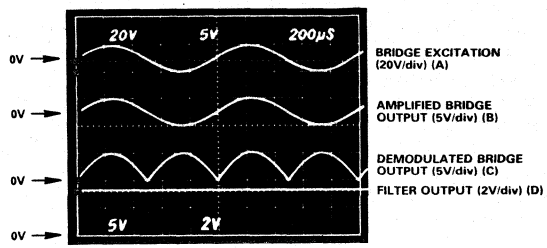


Figure 23. AC Bridge Waveforms

LOCK-IN AMPLIFIER APPLICATIONS

Lock-in amplification is a technique which is used to separate a small, narrow band signal from interfering noise. The lock-in amplifier acts as a detector and narrow band filter combined. Very small signals can be detected in the presence of large amounts of uncorrelated noise when the frequency and phase of the desired signal are known.

The lock-in amplifier is basically a synchronous demodulator followed by a low pass filter. An important measure of performance in a lock-in amplifier is the dynamic range of its demodulator. The schematic diagram of a demonstration circuit which exhibits the dynamic range of an AD630 as it might be used in a lock-in amplifier is shown in Figure 24. Figure 25 is an oscilloscope photo showing the recovery of a signal modulated at 400Hz from a noise signal approximately 100,000 times larger; a dynamic range of 100dB.

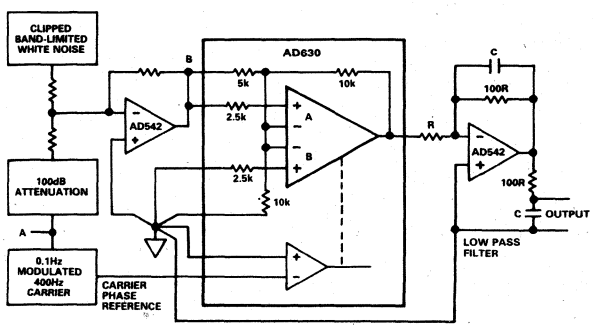


Figure 24. Lock-In Amplifier

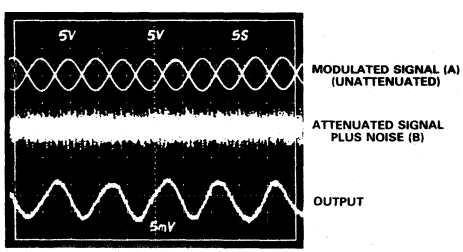


Figure 25. Lock-In Amplifier Wave Forms

The test signal is produced by modulating a 400Hz carrier with a 0.1Hz sine wave. The signals produced, for example, by chopped radiation (IR, optical, etc.) detectors may have similar low frequency components. A sinusoidal modulation is used for clarity of illustration. This signal is produced by a circuit similar to Figure 19b and is shown in the upper trace of Figure 25. It is attenuated 100,000 times normalized to the output, B, of the summing amplifier. A noise signal which might represent, for example, background and detector noise in the chopped radiation case, is added to the modulated signal by the summing amplifier. This signal is simply band limited clipped white noise. Figure 25 shows the sum of attenuated signal plus noise in the center trace. This combined signal is demodulated synchronously using phase information derived from the modulator, and the result is low pass filtered using a 2-pole simple filter which also provides a gain of 100 to the output. This recovered signal is the lower trace of Figure 25.

The combined modulated signal and interfering noise used for this illustration is similar to the signals often requiring a lock-in amplifier for detection. The precision input performance of the AD630 provides more than 100dB of signal range and its dynamic response permits it to be used with carrier frequencies more than two orders of magnitude higher than in this example. A more sophisticated low pass output filter will aid in rejecting wider bandwidth interference.

ANALOG DEVICES

Internally Trimmed Precision I.C. Multiplier

AD632

PRELIMINARY TECHNICAL DATA

FEATURES

- Pretrimmed to ±0.5% Max 4-Quadrant Error
- All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10] + Z_2$ Transfer Function
- Scale-Factor Adjustable to Provide up to X10 Gain
- Low Noise Design: 90μV rms, 10Hz-10kHz
- Low Cost, Monolithic Construction
- Excellent Long Term Stability

APPLICATIONS

- High Quality Analog Signal Processing
- Differential Ratio and Percentage Computations
- Algebraic and Trigonometric Function Synthesis
- Accurate Voltage Controlled Oscillators and Filters

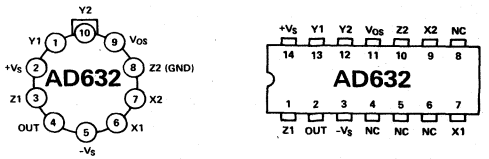
PRODUCT DESCRIPTION

The AD632 is an internally-trimmed monolithic four-quadrant multiplier/divider. The AD632B has a maximum multiplying error of ±0.5% without external trims.

Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions. The simplicity and flexibility of use provide an attractive alternative approach to the solution of complex control functions.

The AD632 is pin for pin compatible with the industry standard AD532 with improved specifications and a fully differential high impedance Z-input. The AD632 is capable of providing gains of up to X10, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD632 can be effectively employed as a variable gain differential input amplifier with high common mode rejection. The effectiveness of the variable gain capability is enhanced by the inherent low noise of the AD632: 90μV rms.

AD632 PIN CONFIGURATION



PRODUCT HIGHLIGHTS

Guaranteed Performance Over Temperature: The AD632A and AD632B are specified for maximum multiplying errors of ±1.0% and ±0.5% of full scale, respectively at +25°C and are rated for operation from -25°C to +85°C. Maximum multiplying errors of ±2.0% (AD632S) and ±1.0% (AD632T) are guaranteed over the extended temperature range of -55°C to +125°C.

6

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, $R \geq 2k\Omega$ unless otherwise noted)

Model	AD632A			AD632B			AD632S			AD632T			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)+Z_2}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)+Y_2}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)+Z_2}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)+Y_2}{10V}$		
Total Error[1] ($-10V \leq X, Y \leq +10V$)			±1.0			**±0.5**			**±1.0**			**±0.5**	%
T_A = min to max			±1.5			**±1.0**			**±2.0**			**±1.0**	%
Total Error vs Temperature			±0.02			±0.01			±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.25			±0.1		%
Temperature-Coefficient of Scaling-Voltage		±0.02						±0.2				±0.005	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.08	±0.5		±0.8	±0.25		±0.08	±0.5		±0.08	±0.25	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.01			±0.1	±0.1		±0.01			±0.01	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.15	±0.3		±0.05	±0.15		±0.15	±0.3		±0.15	±0.15	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01	±0.1		±0.01	±0.1		±0.01	±0.1		±0.01	±0.1	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift		200	400		200	400			**500**			**300**	µV/°C
DYNAMICS													
Small Signal BW, (V_{OUT} = 0.1rms)		1			1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2			2		µs
NOISE													
Noise Spectral-Density SF = 10V		0.08			0.08			0.08			0.08		µV/√Hz
SF = 3V[4]		0.04			0.04			0.04			0.04		µV/√Hz
Wideband Noise A = 10Hz to 5MHz		1.0			1.0			1.0			1.0		µV/rms
P = 10Hz to 10kHz		90			90			90			90		µV/rms
OUTPUT													
Output Voltage Swing	**±11**			**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]													
Signal Voltage Range (Diff. or CM		±10			±10			±10			±10		V
Operating Diff.)		±12			±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z		200	400		100	200			500			300	µV/°C
CMRR	**60**	80		**70**	90		**60**	80		**70**	90		dB
Bias Current		0.8	2		0.8	2		0.8	2		0.8	2	µA
Offset Current		0.1			0.1			0.1			0.1		µA
Differential Resistance		10			10			10			10		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1]													
(X − 10V, −10V ≤ Z ≤ +10V)		±0.75			±0.35			±0.75			±0.35		%
(X − 1V, −1V ≤ Z ≤ +1V)		±2.0			±1.0			±2.0			±1.0		%
(0.10V ≤ X ≤ 10V, −10V ≤ Z ≤ 10V													
SQUARER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)^2}{(10V)}+Z_2$			$\frac{(X_1-X_2)^2}{(10V)}+Z_2$			$\frac{(X_1-X_2)^2}{(10V)}+Z_2$			$\frac{(X_1-X_2)^2}{(10V)}+Z_2$		
Total Error (−10V ≤ X ≤ 10V)		±0.6			±0.3			±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function, ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[6] (1V ≤ Z ≤ 10V)		±1.0			±0.5			±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS													
Supply Voltage													
Rated Performance		±15			±15			±15			±15		V
Operating	**±8**		**±20**	**±8**		**±20**	**±8**		**±22**	**±8**		**±22**	V
Supply Current													
Quiescent		4	**6**		4	6		4	**6**		4	6	mA

NOTES
[1]Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
[6]With external Z-offset adjustment, Z ≤ ±X.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

	AD632A, B	AD632S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD632A

PACKAGE OPTIONS[1]

AD632AD: TO-116 – (D14A)
AD632AH: TO-100
AD632BD: TO-116 – (D14A)
AD632BH: TO-100
AD632SD: TO-116 – (D14A)
AD632SH: TO-100
AD632TD: TO-116 – (D14A)
AD632TH: TO-100

NOTE
[1] See Section 19 for package outline information.

6

Typical Performance Curves

(typical at +25°C with $\pm V_S$ = 15V)

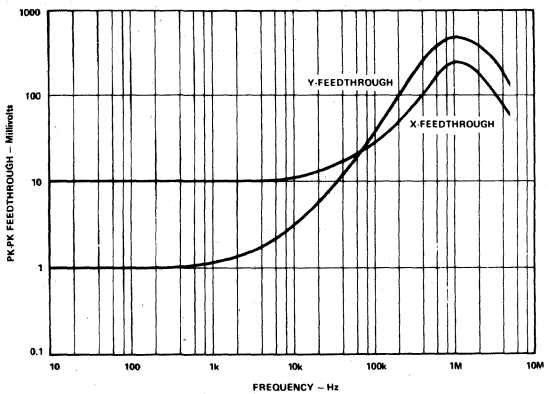


Figure 1. AC Feedthrough vs. Frequency

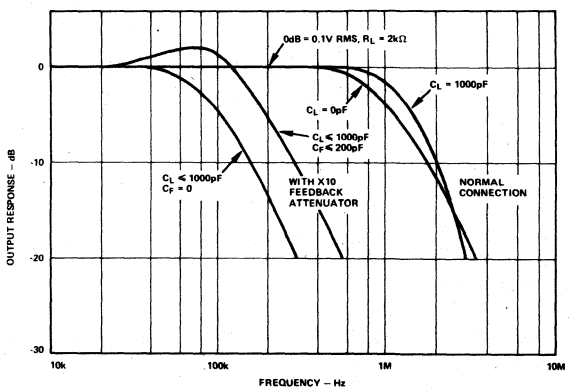


Figure 2. Frequency Response as a Multiplier

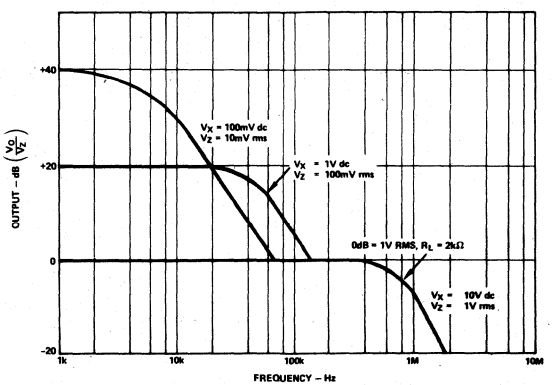


Figure 3. Frequency Response vs. Divider Denominator Input Voltage

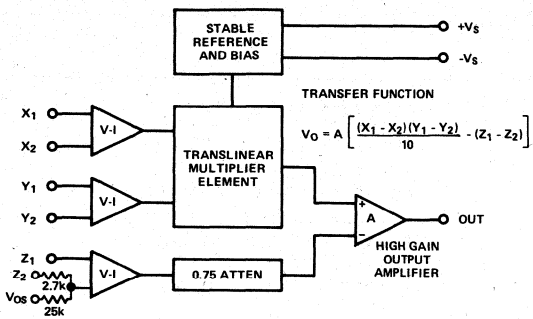


Figure 4. AD632 Functional Block Diagram

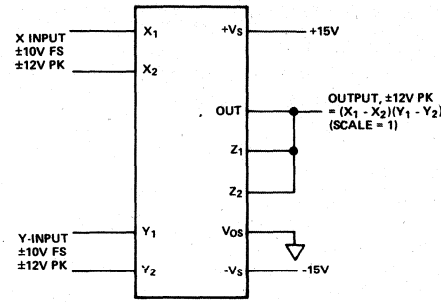


Figure 6. Connections for Scale-Factor of Unity

OPERATION AS A MULTIPLIER

Figure 5 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

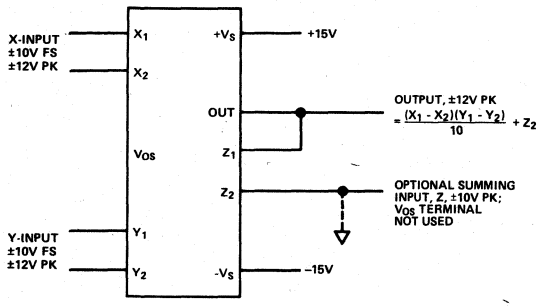


Figure 5. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input. Curve 1 shows the typical ac feedthrough with this adjustment mode. Note that the feedthrough of the Y input is a factor of 10 lower than that of the X input and should be used in applications where null suppression is critical.

The Z_2 terminal of the AD632 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective signal common potentials to realize the full accuracy of the AD632.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 6. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the Z_1 terminal where they are amplified by -10 or to the common ground connection where they are amplified by -1. Input signals may also be applied to the lower end of the 2.7kΩ resistor, giving a gain of +9.

OPERATION AS A DIVIDER

Figure 7 shows the connection required for division. Unlike earlier products, the AD632 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 3.

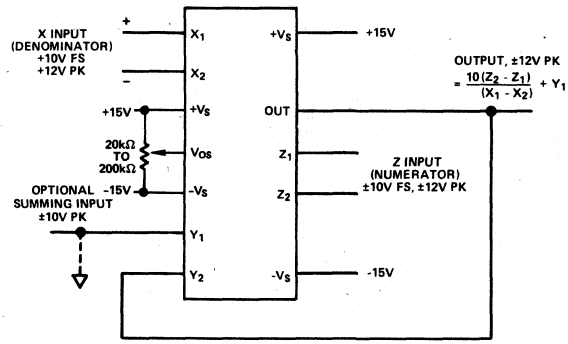


Figure 7. Basic Divider Connection

Without additional trimming, the accuracy of the AD632B is sufficient to maintain a 1% error over a 10V to 1V denominator range (The AD535 is functionally equivalent to the AD632 and has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications).

This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input. To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

*See the AD535 Data Sheet for more details.

ANALOG DEVICES

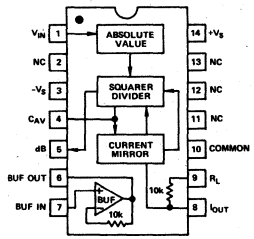
Low Level True rms-to-dc Converter

AD636

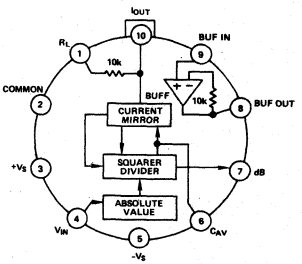
FEATURES

- True rms-to-dc Conversion
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz -3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit

AD636 FUNCTIONAL BLOCK DIAGRAMS



TO-116
TOP VIEW



TO-100
TOP VIEW

PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. The AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±12V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. Thus no external trims are required to achieve full rated accuracy.

The AD636 is available in two accuracy grades; the AD636J has a total error of ±0.5mV ±1.0% of reading, and the AD636K is accurate within ±0.2mV ±0.5% of reading. Both versions are specified for the 0 to 70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10 pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery-powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5V to +24V or split ±2.5V to ±12V sources. A standard 9V battery will provide several hundred hours of continuous operation.

SPECIFICATIONS (typical @ +25°C, $+V_S$ = +3V, $-V_S$ = -5V, unless otherwise specified)

Model	AD636J	AD636K
TRANSFER EQUATION	$V_{OUT} = \sqrt{\text{avg. } (V_{IN})^2}$	*
CONVERSION ACCURACY		
Total Error, Internal Trim[1,2]	±0.5mV ±1.0% of Reading, max	±0.2mV ±0.5% of Reading, max
vs. Temperature, 0 to +70°C	±(0.1mV ±0.01% of Reading)/°C max	±(0.1mV ±0.005% of Reading)/°C max
vs. Supply Voltage	±(0.1mV ±0.01% of Reading)/V	*
dc Reversal Error	±0.2% of Reading	±0.1% of Reading
Total Error, External Trim[1]	±0.3mV ±0.3% of Reading	±0.1mV ±0.2% of Reading
ERROR vs. CREST FACTOR[3]		
Crest Factor 1 to 2	Specified Accuracy	*
Crest Factor = 3	-0.2%	*
Crest Factor = 6	-0.5%	*
FREQUENCY RESPONSE[2,4]		
Bandwidth for 1% Additional Error (0.2dB)		
V_{IN} = 10mV	12kHz	*
V_{IN} = 100mV	80kHz	*
V_{IN} = 200mV	130kHz	*
±3dB Bandwidth		
V_{IN} = 10mV	80kHz	*
V_{IN} = 100mV	800kHz	*
V_{IN} = 200mV	1.3MHz	*
AVERAGING TIME CONSTANT	25ms/μF	*
INPUT CHARACTERISTICS		
Signal Range		
+3, -5V Supply	±2.8V Peak	*
±2.5V Supply	±2V Peak	*
±5V Supply	±5V Peak	*
Safe Input, All Supply Voltage	±12V max	*
Input Resistance	6.7kΩ ±20%	*
Input Offset Voltage	0.5mV max	0.2mV max
OUTPUT CHARACTERISTICS[2]		
Offset Voltage	0.5mV max	0.2mV max
vs. Temperature	±10μV/°C	*
vs. Supply	±0.1mV/V	*
Voltage Swing		
+3, -5V Supply	0 to 1V typ (0.3V min)	*
±5V Supply	0 to 1.4V typ (0.3V min)	*
Output Impedance	10kΩ ±20% typ	*
dB OUTPUT		
Error, 7mV ≤ V_{IN} ≤ 300mV rms	±0.5dB max	±0.2dB max
Scale Factor	-3mV/dB	*
Scale Factor Temperature Coefficient	+0.3%/°C(-0.03dB/°C)	*
I_{REF} for 0dB = 0.1V rms	4μA (2μA min, 8μA max)	*
I_{REF} Range	1μA to 50μA	*
I_{OUT} TERMINAL		
I_{OUT} Scale Factor	100μA/V rms	*
I_{OUT} Scale Factor Tolerance	±20%	*
Output Resistance	10^8 Ω	*
Voltage Compliance	$-V_S$ to ($+V_S$ -2V)	*
BUFFER AMPLIFIER		
Input and Output Voltage Range	$-V_S$ to ($+V_S$ -2V) min	*
Input Offset Voltage, R_S = 10k	2mV max	1mV max
Input Current	100nA typ (300nA max)	*
Input Resistance	10^8 Ω	*
Output Current	(+5mA, -130μA) min	*
Short Circuit Current	20mA	*
Small Signal Bandwidth	1MHz	*
Slew Rate[5]	5V/μs	*
POWER SUPPLY		
Voltage, Rated Performance	+3, -5V	*
Dual Supply	+2/-2.5V to ±12V	*
Single Supply	+5V to +24V	*
Quiescent Current[6]	800μA (1mA max)	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Storage	-55°C to +150°C	*
PACKAGE OPTIONS[7]		
"H" Package: TO-100	AD636JH	AD636KH
"D" Package: TO-116 Style D14A	AD636JD	AD636KD

NOTES
[1] Accuracy is specified for 0 to 200mV rms, dc or 1kHz sinewave input. Accuracy is degraded at higher rms signal levels.
[2] Measured at pin 8 of DIP (I_{OUT}), with pin 9 tied to common.
[3] Error vs. crest factor is specified as additional error for a 200mV rms rectangular pulse train, pulse width = 200μs.
[4] Input voltages are expressed in volts rms.
[5] With 10kΩ pull-down resistor from pin 6 (BUF OUT) to $-V_S$.
[6] With BUF input tied to $-V_S$.
[7] See Section 19 for package outline information.
*Specifications same as AD636J.

Specifications subject to change without notice.

STANDARD CONNECTION

The AD636 is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD636 will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD636 is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible. C_F is an optional output ripple filter, as discussed elsewhere in this data sheet.

The input and output signal ranges are a function of the supply voltages as detailed in the specifications. The AD636 can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 10k resistor. The buffer amplifier can then be used for other purposes. Further, the AD636 can be used in a current output mode by disconnecting the 10k resistor from the ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 100μA per volt rms input, positive out.

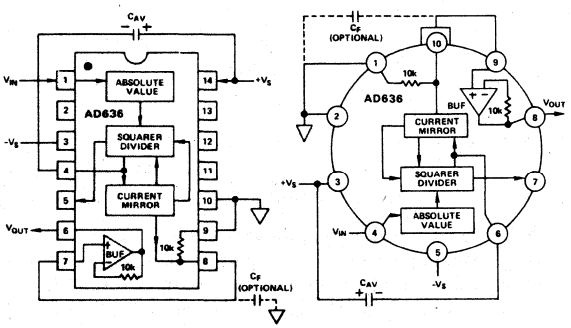


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD636, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. The scale factor is trimmed by using R_1 as shown. The insertion of R_2 allows R_1 to either increase or decrease the scale factor.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 200mV dc input should give 200mV dc output. Of course, a ±200mV peak-to-peak sinewave should give a 141.4mV dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 assume the use of dual power supplies. The AD636 can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 1 microamp of current flows into pin 10 (pin 2 on the "H" package). Alternately, the COM pin of some CMOS ADCs provides a suitable artificial ground for the AD636. AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 6.7kΩ; for a cut-off at 10Hz, C_2 should be 3.3μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The load resistor, R_L, is necessary to provide current sinking capability.

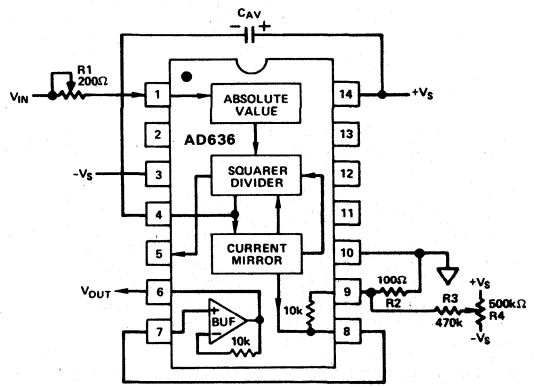


Figure 2. Optional External Gain and Output Offset Trims

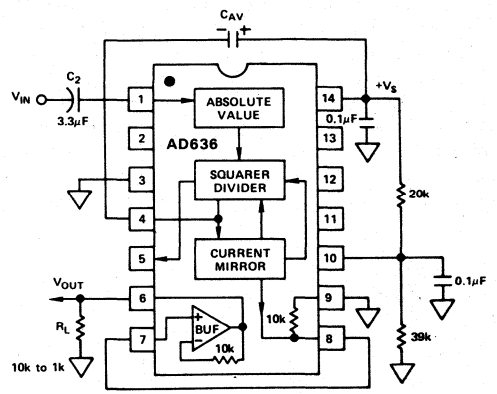


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD636 will compute the rms of both ac and dc signals. If the input is a slowly-varying dc voltage, the output of the AD636 will track the input exactly. At higher frequencies, the average output of the AD636 will approach the rms value of the input signal. The actual output of the AD636 will differ from the ideal output by an average (or dc) error and some amount of ripple, as demonstrated in Figure 4.

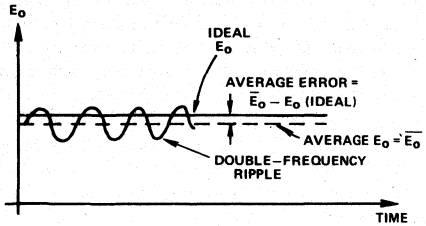


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% dc error above a given frequency. For example, if a 60Hz waveform is to be measured with a dc error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

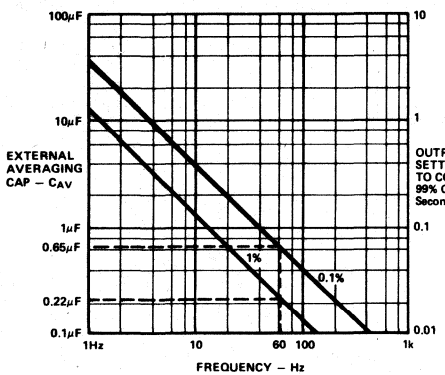


Figure 5. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

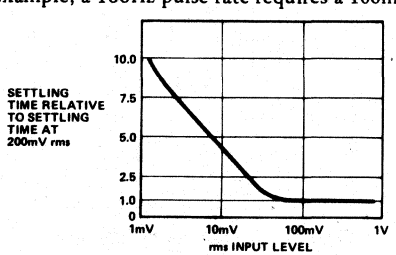


Figure 6. Settling Time vs. Input Level

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 4.7μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

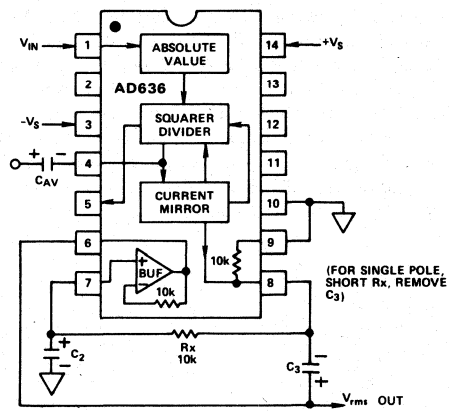


Figure 7. 2 Pole "Post" Filter

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

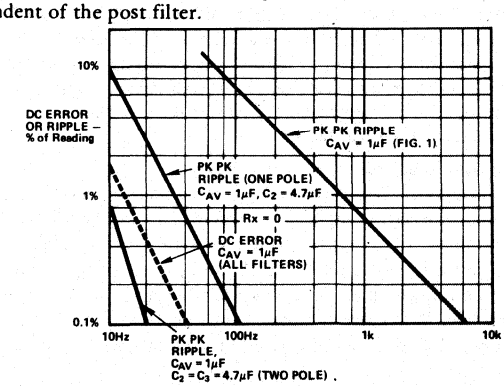


Figure 8. Performance Features of Various Filter Types

AD636 PRINCIPLE OF OPERATION

The AD636 embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD636 follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD636; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.}\ [I_1^2/I_4] = I_1\ \text{rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD636 thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

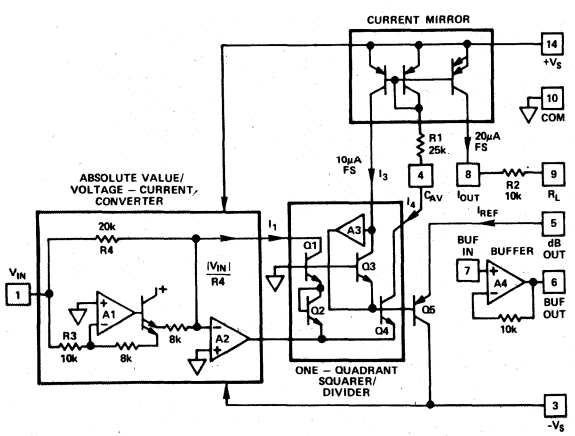


Figure 9. Simplified Schematic

THE AD636 BUFFER AMPLIFIER

The buffer amplifier included in the AD636 offers the user additional application flexibility. It is important to understand some of the characteristics of this amplifier to obtain optimum performance. Figure 10 shows a simplified schematic of the buffer.

Since the output of an rms-to-dc converter is always positive, it is not necessary to use a traditional complementary Class AB output stage. In the AD636 buffer, a Class A emitter follower is used instead. In addition to excellent positive output voltage swing, this configuration allows the output to swing fully down to ground in single-supply applications without the problems associated with most IC operational amplifiers.

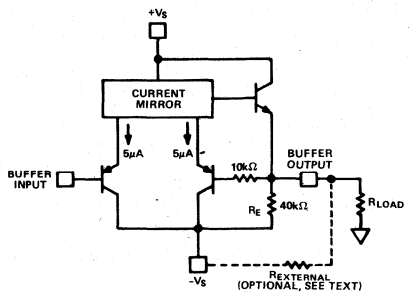


Figure 10. AD636 Buffer Amplifier Simplified Schematic

When this amplifier is used in dual-supply applications as an input buffer amplifier driving a load resistance referred to ground, steps must be taken to insure an adequate negative voltage swing. For negative outputs, current will flow from the load resistor through the 40kΩ emitter resistor, setting up a voltage divider between $-V_S$ and ground. This reduced effective $-V_S$ will limit the available negative output swing of the buffer. Addition of an external resistor in parallel with R_E alters this voltage divider such that increased negative swing is possible.

Figure 11 shows the value of $R_{EXTERNAL}$ for a particular ratio of V_{PEAK} to $-V_S$ for several values of R_{LOAD}. Addition of $R_{EXTERNAL}$ increases the quiescent current of the buffer amplifier by an amount equal to $R_{EXT}/-V_S$. Nominal buffer quiescent current with no $R_{EXTERNAL}$ is 30μA at $-V_S = -5V$.

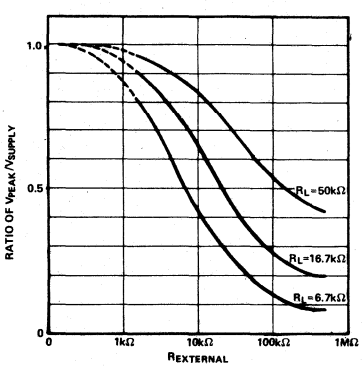


Figure 11. Ratio of Peak Negative Swing to $-V_S$ vs. $R_{EXTERNAL}$ for Several Load Resistances

FREQUENCY RESPONSE

The AD636 utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD636 at input levels from 1 millivolt to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and ±3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 200kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to 12kHz.

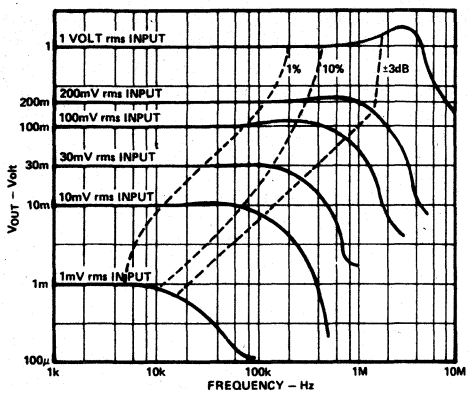


Figure 12. AD636 Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 13 is a curve of reading error for the AD636 for a 200mV rms input signal with crest factors from 1 to 7. A rectangular pulse train (pulse width 200μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 7 while maintaining a constant 200mV rms input amplitude.

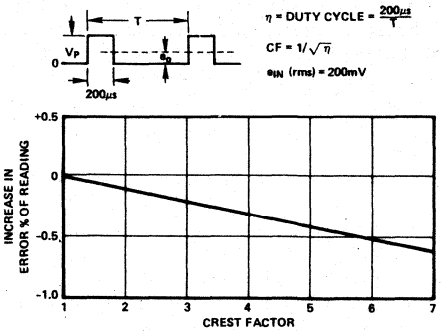


Figure 13. Error vs. Crest Factor

A COMPLETE AC DIGITAL VOLTMETER

Figure 14 shows a design for a complete low power ac digital voltmeter circuit based on the AD636. The 10MΩ input attenuator allows full scale ranges of 200mV, 2V, 20V and 200V rms. Signals are capacitively coupled to the AD636 buffer amplifier, which is connected in an ac bootstrapped configuration to minimize loading. The buffer then drives the 6.7kΩ input impedance of the AD636. The COM terminal of the ADC chip provides the false ground required by the AD636 for single supply operation. An AD589 1.2 volt reference diode is used to provide a stable 100 millivolt reference for the ADC in the linear rms mode; in the dB mode, a 1N4148 diode is inserted in series to provide correction for the temperature coefficient of the dB scale factor. Calibration of the meter is done by first adjusting offset pot R17 for a proper zero reading, then adjusting the R13 for an accurate readout at full scale.

Calibration of the dB range is accomplished by adjusting R9 for the desired 0dB reference point, then adjusting R14 for the desired dB scale factor (a scale of 10 counts per dB is convenient).

Total power supply current for this circuit is typically 2.8mA using a 7106-type ADC.

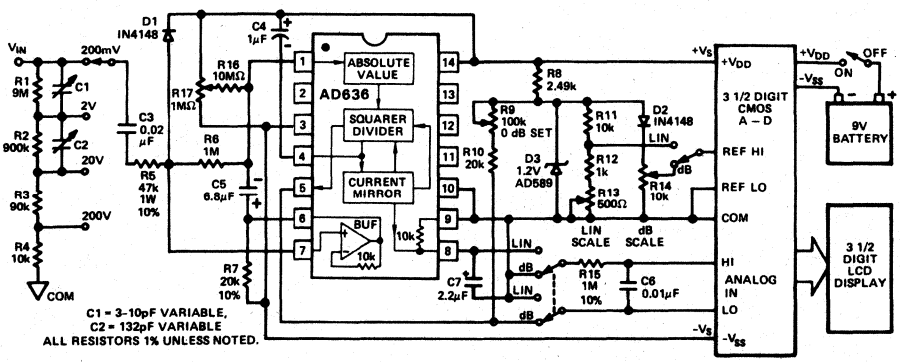


Figure 14. 3 1/2 Digit True rms ac Voltmeter

ANALOG DEVICES

High Precision Wideband rms-to-dc Converter

AD637

FEATURES

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V rms Input**
- **0.10% Max Error to Crest Factor of 3**

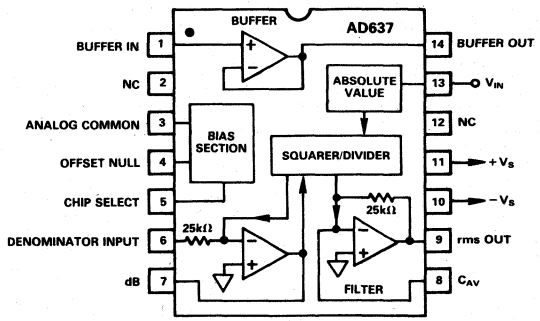
Wide Bandwidth
- **8MHz at 2V rms Input**
- **600kHz at 100mV rms**

Computes:
- **True rms**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (−60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiesent Current Reduction from 2.2mA to 350μA**

AD637 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms to dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms to dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600kHz with inputs of 200mV rms and up to 8MHz when the input levels are above 2V rms.

As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60dB. An externally programmed reference current allows the user to select the 0dB reference voltage to correspond to any. level between 0.1V and 2.0V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2mA to 350μA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

The AD637 is available in two accuracy grades (J, K) for commercial (0 to +70°C) temperature range applications and one (S) rated over the −55°C to +125°C temperature range. All versions are available in ceramic 14-lead DIP packages.

PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD637AJ Min	AD637AJ Typ	AD637AJ Max	AD637AK Min	AD637AK Typ	AD637AK Max	AD637AS Min	AD637AS Typ	AD637AS Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig. 2)[1]			±1 ±0.5			±0.5 ±0.2			±1 ±0.5	mV ± % of Reading
T_{min} to T_{max}			±3.0 ±0.6			±2.0 ±0.3			±6 ±0.7	mV ± % of Reading
vs. Supply +		30	150		30	150		30	150	μV
vs. Supply −		100	300		100	300		100	300	μV
dc Reversal Error			0.25			0.1			0.25	% of Reading
Nonlinearity 2V Full Scale[2]			0.04			0.02			0.04	% of FSR
Nonlinearity 7V Full Scale			0.05			0.05			0.05	% of FSR
Total Error, External Trim		±0.5 ±0.1			±0.25 ±0.05			±0.5 ±0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0.1			±0.1			±0.1		% of Reading
Crest Factor = 10		±1.0			±1.0			±1.0		% of Reading
AVERAGING TIME CONSTANT		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15V Supply										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±15			±15			±15	V p-p
Signal Range, ±5V Supply										
Continuous rms Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input			±6			±6			±6	V p-p
Maximum Continuous Non-Destructive										
Input Level (All Supply Voltages)			±15			±15			±15	V p-p
Input Resistance		8			8			8		kΩ
Input Offset Voltage			±0.5			±0.2			±0.5	mV
FREQUENCY RESPONSE[4]										
Bandwidth for 1% additional error (0.1dB)										
V_{IN} = 20mV		11			11			11		kHz
V_{IN} = 200mV		66			66			66		kHz
V_{IN} = 2V		97			200			200		kHz
= 3dB Bandwidth										
V_{IN} = 20mV		150			150			150		kHz
V_{IN} = 200mV		1			1			1		MHz
V_{IN} = 2V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			±1			±0.5			±1	mV
vs. Temperature		±0.05			±0.05			±0.05		mV/°C
Voltage Swing, ±15V Supply,										
2kΩ Load	0 to +13.5			0 to +13.5			0 to +13.5			V
Voltage Swing, ±5V Supply,										
2kΩ Load	0 to +2			0 to +2			0 to +2			V
Output Current	5			5			5			mA
Short Circuit Current		20			20			20		mA
Resistance, Chip Select "High"		0.5			0.5			0.5		Ω
Resistance, Chip Select "Low"		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±1			±1			±1		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC		−0.3			−0.3			−0.3		% of Reading/°C
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	μA
I_{REF} Range	1		100	1		100	1		100	μA
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			V
Input Offset Voltage		±0.8	±2		±0.8	±1		±0.8	±2	mV
Input Current		±2	±10		±2	±5		±2	±10	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[5]		5			5			5		V/μs
DENOMINATOR INPUT										
Input Range		0 to 2			0 to 2			0 to 2		V
Input Impedance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage			±0.5			±0.5			±0.5	mV
CHIP SELECT PROVISION (CS)										
rms "ON" Level	Open or $+2.4V < V_C < +V_S$			Open or $+2.4V < V_C < +V_S$			Open or $+2.4V < V_C < +V_S$			
rms "OFF" Level	$V_C < +0.2V$			$V_C < +0.2V$			$V_C < +0.2V$			
I_{OUT} of Chip Select										
CS "LOW"	10			10			10			μA
CS "HIGH"	Zero			Zero			Zero			
On Time	10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			
Off Time	10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			10μs + ((25kΩ) × C_{AV})			

Model	AD637AJ			AD637AK			AD637AS			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY										
Operating Voltage Range	±3.0		±18	±3.0		±18	±3		±18	V
Quiescent Current		2.2	3		2.2	3		2.2	3	mA
Standby Current		350	450		350	450		350	450	mA

NOTES
[1]Accuracy specified 0-7V rms dc with AD637 connected as shown in Figure 1.
[2]Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10mV and 2V.
[3]Error vs. crest factor is specified as additional error for 1V rms.
[4]Input voltages are expressed in volts rms. % are in % of reading.
[5]With external 2kΩ pull down resistor tied to $-V_S$.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature	Package[1]
AD637JD	0 to +70°C	Ceramic DIP (D14A)
AD637KD	0 to +70°C	Ceramic DIP (D14A)
AD637SD	−55°C to +125°C	Ceramic DIP (D14A)

NOTE
[1]See Section 19 for package outline information.

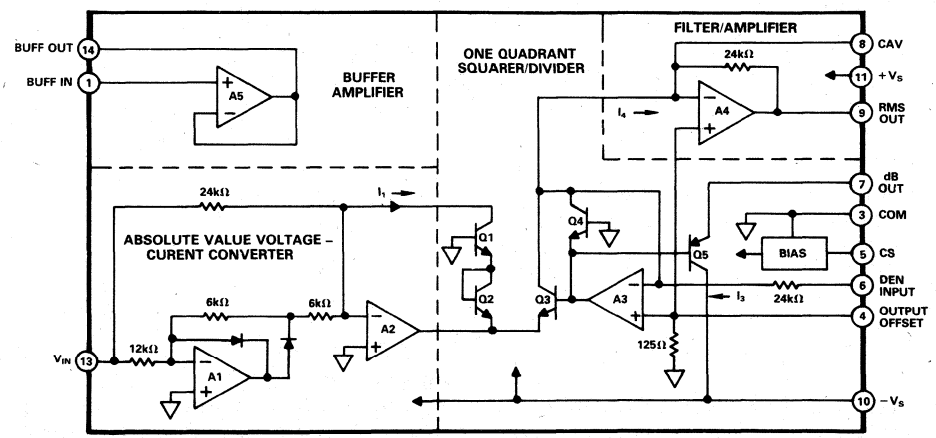


Figure 1. Simplified Schematic

FUNCTIONAL DESCRIPTION

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation

$$V\ rms = Avg\left[\frac{V_{IN}^2}{V\ rms}\right]$$

Figure 1 is a simplified schematic of the AD637, it is subdivided into four major sections; absolute value circuit (active rectifier), square/divider, filter circuit and buffer amplifier. The input voltage V_{IN} which can be ac or dc is converted to a unipolar current I1 by the active rectifier A1, A2. I1 drives one input of the squarer divider which has the transfer function

$$I_4 = \frac{I_1^2}{I_3}$$

The output current of the squarer/divider, I4 drives A4 which forms a low pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal than A4s output will be proportional to the average of I4. The output of this filter amplifier is used by A3 to provide the denominator current I3 which equals Avg. I4 and is returned to the squarer/divider to complete the implicit rms computation.

$$I_4 = Avg\left[\frac{I_1^2}{I_4}\right] = I_1\ rms$$

and

$$V_{OUT} = V_{IN}\ rms$$

If the averaging capacitor is omitted the AD637 will compute the absolute value of the input signal. A nominal 100pF capacitor should be used to insure stability. The circuit operates identically to that of the rms configuration except that I3 is now equal to I4 giving

$$I_4 = \frac{I_1^2}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage, V_{REF}, to pin 6. The circuit operates identically to the rms case except that I3 is now proportional to V_{REF}. Thus:

$$I_4 = Avg\ \frac{I_1^2}{I_3}$$

and

$$V_O = \frac{V_{IN}^2}{V_{DEN}}$$

This is the mean square of the input signal.

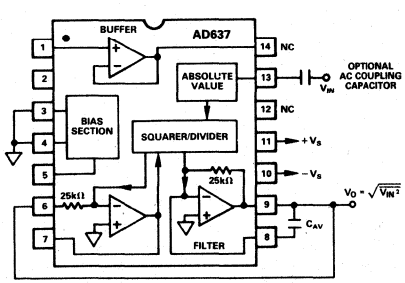


Figure 2. Standard rms Connection

STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 2, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 will compute the true rms of any input signal. An averaging error, the magnitude of which will be dependent on the value of the averaging capacitor will be present at low frequencies. For example, if the filter capacitor C_{AV}, is 4μF this error will be 0.1% at 10Hz and decreases to 1% at 3Hz. If it is desired to measure only ac signals the AD637 can be ac coupled through the addition of a nonpolar capacitor in series with the input as shown in Figure 2.

The performance of the AD637 is tolerant of minor variations in the power supply voltages, however, if the supplies being used exhibit a considerable amount of high frequency ripple it is advisable to bypass both supplies to ground through a 0.1μF ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 3. The output signal can be used buffered or nonbuffered depending on the characteristics of the load. The output of the AD637 is capable of driving 5mA into a 2kΩ load without degrading the accuracy of the device.

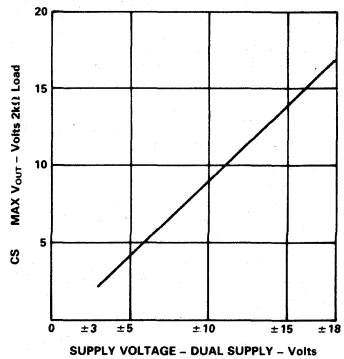


Figure 3. AD637 max V_{OUT} vs. Supply Voltage

CHIP SELECT

The AD637 includes a chip select feature which allows the user to decrease the quiescent current of the device from 2.2mA to 350μA. This is done by driving the CS, pin 5, to below 0.2V dc. Under these conditions, the output will go into a high impedance state. In addition to lowering power consumption, this feature permits bussing the outputs of a number of AD637s to form a wide bandwidth rms multiplexer. If the chip select is not being used, pin 5 should be tied high or left floating.

OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions to allow the user to trim out both output offset and scale factor errors. These trims will result in significant reduction in the maximum total error as shown in Figure 4. This remaining error is due to a nontrimmable input offset in the absolute value circuit and the irreducible nonlinearity of the device.

The trimming procedure on the AD637 is as follows:

1. Ground the input signal, V_{IN} and adjust R1 to give 0V output from pin 9. Alternatively R1 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input to V_{IN}, using either a dc or a calibrated ac signal, trim R3 to give the correct output at pin 9, i.e., 1V dc should give 1.000V dc output. Of course, a 2V peak-to-peak sine wave should give 0.707V dc output. Remaining errors are due to the nonlinearity.

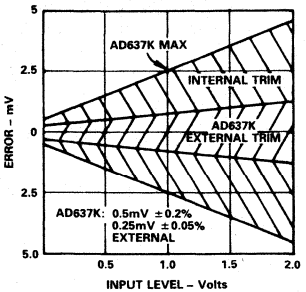


Figure 4. Max Total Error vs. Input Level AD637K Internal and External Trims

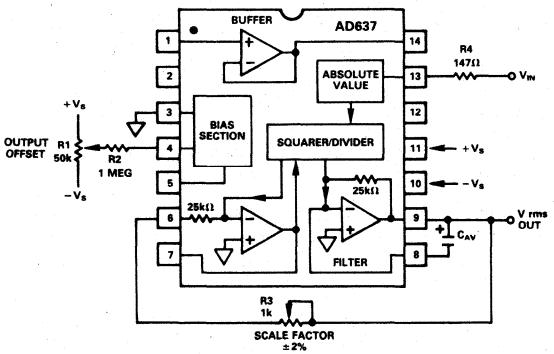


Figure 5. Optional External Gain and Offset Trims

CHOOSING THE AVERAGING TIME CONSTANT

The AD637 will compute the true rms value of both dc and ac input signals. At dc the output will track the absolute value of the input exactly; with ac signals the AD637's output will approach the true rms value of the input. The deviation from the ideal rms value is due to an averaging error. The averaging error is comprised of an ac and dc component. Both components are functions of input signal frequency f, and the averaging time constant τ (τ: 25ms/μF of averaging capacitance). As shown in Figure 6, the averaging error is defined as the peak value of the ac component, ripple, plus the value of the dc error.

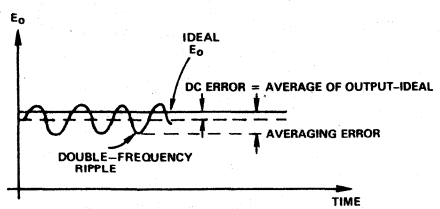


Figure 6. Typical Output Waveform for a Sinusoidal Input

The peak value of the ac ripple component of the averaging error is defined approximately by the relationship:

$$\frac{50}{6.3\tau f} \text{ in \% of reading where } (\tau > 1/f)$$

This ripple can add a significant amount of uncertainty to the accuracy of the measurement being made. The uncertainty can be significantly reduced through the use of a post filtering network or by increasing the value of the averaging capacitor.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the equation:

$$\frac{1}{0.16 + 6.4\tau^2 f^2} \text{ in \% of reading}$$

Since the averaging time constant, set by C_{AV}, directly sets the time that the rms converter "holds" the input signal during computation, the magnitude of the dc error is determined only by C_{AV} and will not be affected by post filtering.

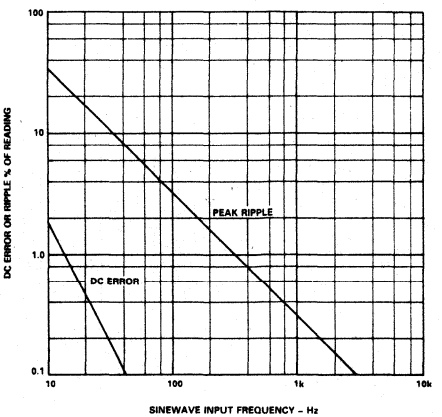


Figure 7. Comparison of Percent dc Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard rms Connection with a 1μF C_{AV}

The ac ripple component of averaging error can be greatly reduced by increasing the value of the averaging capacitor. There are two major disadvantages to this: first, the value of the averaging capacitor will become extremely large and second, the settling time of the AD637 increases in direct proportion to the value of the averaging capacitor (Ts = 115ms/μF of averaging capacitance). A preferrable method of reducing the ripple is through the use of the post filter network, shown in Figure 8. This network can be used in either a one or two pole configuration. For most applications the single pole filter will give the best overall compromise between ripple and settling time.

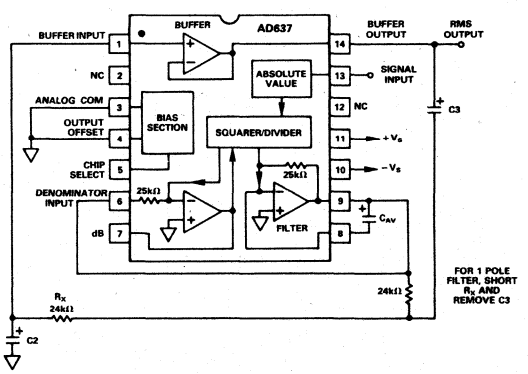


Figure 8. Two Pole Sallen-Key Filter

Figure 9a shows values of C_{AV} and the corresponding averaging error as a function of sine-wave frequency for the standard rms connection. The 1% settling time is shown on the right side of the graph.

Figure 9b shows the relationship between averaging error, signal frequency settling time and averaging capacitor value. This graph is drawn for filter capacitor values of 3.3 times the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50Hz. As an example, by using a 1μF averaging capacitor and a 3.3μF filter capacitor the ripple for a 60Hz input signal will be reduced from 5.3% of reading using the averaging capacitor alone to 0.15% using the single pole filter. This gives a factor of thirty reduction in ripple and yet the settling time would only increase by a factor of three. The values of C_{AV} and C_2, the filter capacitor, can be calculated for the desired value of averaging error and settling time by using Figure 9b.

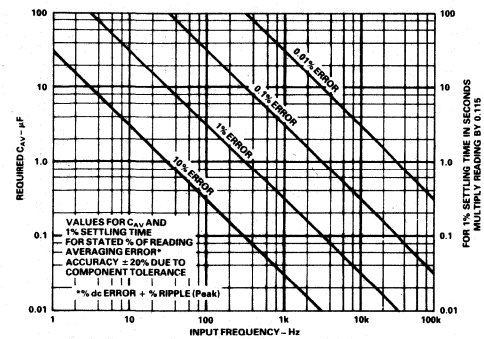


Figure 9a.

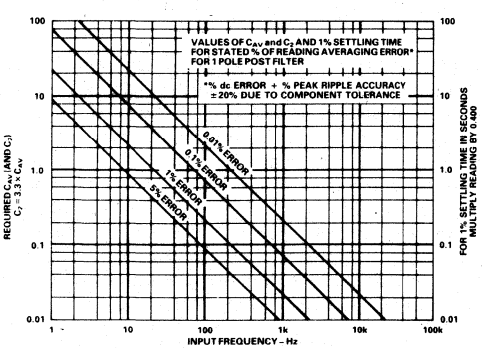


Figure 9b.

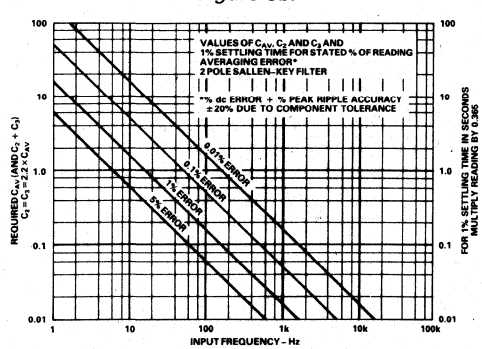


Figure 9c.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table I gives practical component values for various types of 60Hz input signals. These capacitor values can be directly scaled for frequencies other than 60Hz, i.e., for 30Hz double these values, for 120Hz they are halved.

	Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum $R \times C_{AV}$ Time Constant	Recommended C_{AV} and C2 Values for 1% Averaging Error@ 60Hz with T = 16.6ms		1% Settling Time
				Recommended Standard Value C_{AV}	Recommended Standard Value C2	
A	Symmetrical Sine Wave	1/2T	1/2T	0.47μF	1.5μF	181ms
B	Sine Wave with dc Offset	T	T	0.82μF	2.7μF	325ms
C	Pulse Train Waveform	T_2	$10(T-T_2)$	6.8μF	22μF	2.67sec
D		T_2	$10(T-2T_2)$	5.6μF	18μF	2.17sec

Table I. Practical Values of C_{AV} and C2 for Various Input Waveforms

For applications that are extremely sensitive to ripple, the two pole configuration is suggested. This configuration will minimize capacitor values and settling time while maximizing performance.

Figure 9c can be used to determine the required value of C_{AV}, C_2 and C_3 for the desired level of ripple and settling time.

FREQUENCY RESPONSE

The frequency response of the AD637 at various signal levels is shown in Figure 10. The dashed lines show the upper frequency limits for 1%, 10% and ±3dB of additional error. For example, note that for 1% additional error with a 2V rms input the highest frequency allowable is 200kHz. A 200mV signal can be measured with 1% error at signal frequencies up to 100kHz.

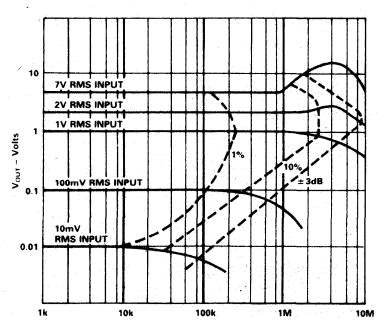


Figure 10. Frequency Response

To take full advantage of the wide bandwidth of the AD637 care must be taken in the selection of the input buffer amplifier. To insure that the input signal is accurately presented to the converter, the input buffer must have a −3dB bandwidth that is wider than that of the AD637. A point that should not be overlooked is the importance of slew rate in this application. For example, the minimum slew rate required for a 1V rms 5MHz sine-wave input signal is 44V/μs. The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier as

some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD381 is recommended as a precision input buffer.

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (≤ 2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

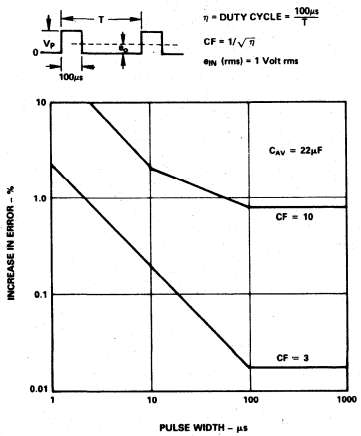


Figure 11. AD637 Error vs. Pulse Width Rectangular Pulse

Figure 12 is a curve of additional reading error for the AD637 for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100µs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

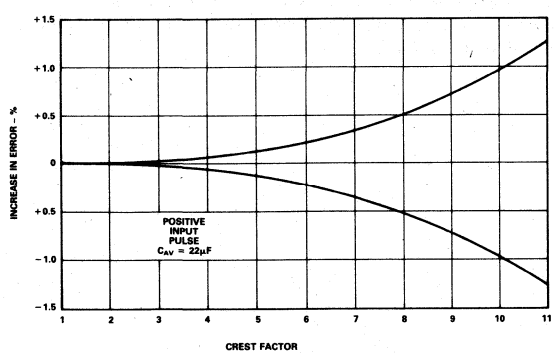


Figure 12. Additonal Error vs. Crest Factor

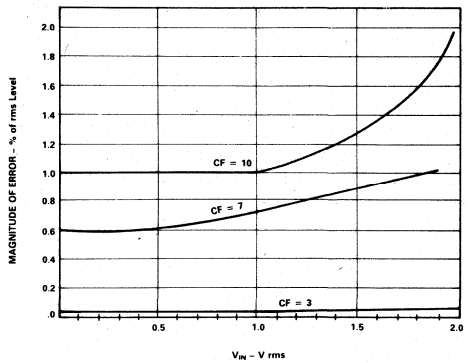


Figure 13. Error vs. rms Input Level for Three Common Crest Factors

CONNECTION FOR dB OUTPUT

Another feature of the AD637 is the logarithmic or decibel output. The internal circuit which computes dB works well over a 60dB range. The connection for dB measurement is shown in Figure 14. The user selects the 0dB level by setting R1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer/divider circuit at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor R3 is available from Tel Labs in Londenderry, New Hampshire (model Q-81) and from Precision Resistor Inc., Hillside, N.J. (model PT146).

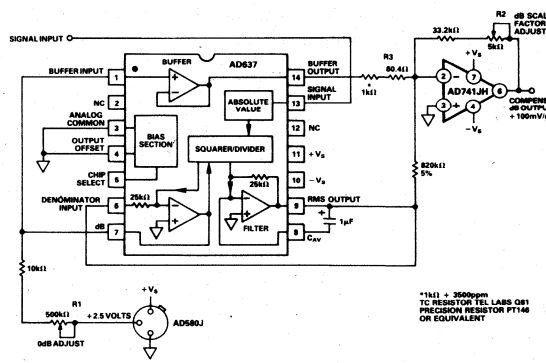


Figure 14. dB Connection

dB CALIBRATION

1. Set V_{IN} = 1.00V dc
2. Adjust R1 for 0dB out = 0.00V
3. Set V_{IN} = 0.1V dc
4. Adjust R2 for dB out = 2.00V

Any other dB reference can be used by setting V_{IN} and R1 accordingly.

LOW FREQUENCY MEASUREMENTS

If the frequencies of the signals to be measured are below 10Hz, the value of the averaging capacitor required to deliver even 1% averaging error in the standard rms connection becomes extremely large. The circuit shown in Figure 15 shows an alternative method of obtaining low frequency rms measurements. The averaging time constant is determined by the product of R and C_{AV1}, in this circuit 0.5ms/μF of C_{AV}. This circuit permits a 20:1 reduction in the value of the averaging capacitor, permitting the use of high quality tantalum capacitors. It is suggested that the two pole Sallen-Key filter shown in the diagram be used to obtain a low ripple level and minimize the value of the averaging capacitor.

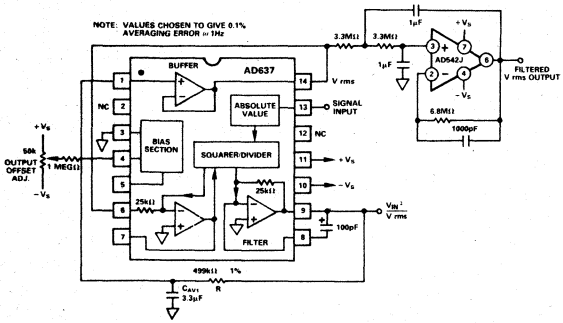


Figure 15. AD637 as a Low Frequency rms Converter

If the frequency of interest is below 1Hz, or if the value of the averaging capacitor is still too large, the 20:1 ratio can be increased. This is accomplished by increasing the value of R. If this is done it is suggested that a low input current, low offset voltage amplifier like the AD542 be used instead of the internal buffer amplifier. This is necessary to minimize the offset error introduced by the combination of amplifier input currents and the larger resistance.

VECTOR SUMMATION

Vector summation can be accomplished through the use of two AD637s as shown in Figure 16. Here the averaging capacitors are omitted (nominal 100pF capacitors are used to insure stability of the filter amplifier), and the outputs are summed as shown. The output of the circuit is

$$V_O = \sqrt{V_X^2 + V_Y^2}$$

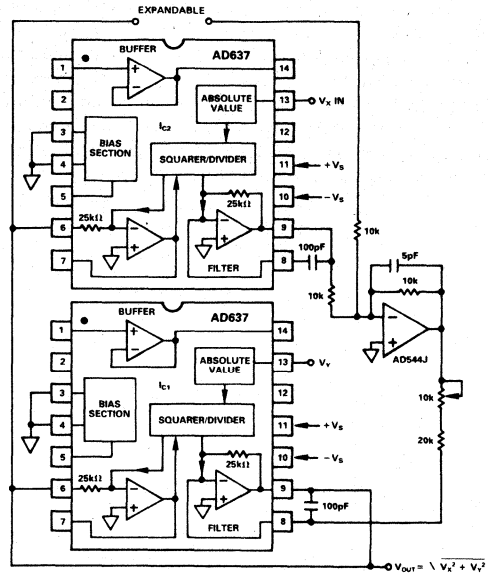


Figure 16. AD637 Vector Sum Configuration

This concept can be expanded to include additional terms by feeding the signal from pin 9 of each additional AD637 through a 10kΩ resistor to the summing junction of the AD544, and tying all of the denominator inputs (pin 6) together.

If C_{AV} is added to IC1 in this configuration the output is $\sqrt{V_X^2 + V_Y^2}$ If the averaging capacitor is included on both IC1 and IC2 the output will be $\sqrt{\overline{V_X^2} + \overline{V_Y^2}}$

This circuit has a dynamic range of 10V to 10mV and is limited only by the 0.5mV offset voltage of the AD637. The useful bandwidth is 100kHz.

Voltage References

Contents

Selection Guide
Voltage References

		AD589	AD580	AD1403	AD581	AD584	AD2700	AD2710
Output Voltage Range	1.235V	●				●		
	2.5V		●	●		●		
	5.0V					●		
	7.5V					●		
	+10.00V				●	●	●	●
	−10.00V						●	
	±10.00V						●	●
Output Voltage Tolerance	⩽±0.4%		●	●	●	●	●	●
	⩽±0.05%				●	●	●	●
	⩽±0.025%						●	●
	⩽±0.012%							●
Temperature Stability	⩽25ppm/°C	●	●	●	●	●	●	●
	⩽10ppm/°C		●		●	●	●	●
	⩽5ppm/°C				●	●	●	●
	⩽1ppm/°C							●
Temperature Range	0 to +70°C	●	●	●	●	●	●	●
	−25°C to +85°C						●	
	−55°C to +125°C	●	●		●	●		
Package Style	Hermetic Package	●	●		●	●	●	●
	Plastic Package			●				
Dice Available		●	●		●	●		
Volume I Page		7–25	7–5	7–29	7–9	7–17	7–33	7–37

Orientation
Voltage References

A voltage reference is used to provide an accurately known voltage which can be utilized in a circuit or system. For example, measurement systems rely on precision references in order to establish a basis for absolute measurement accuracy. Any reference inaccuracy will undermine the accuracy of the overall system. Thus, ideal references are characterized by accurately set (and traceable to recognized fundamental standards) constant output voltage, independent of temperature, load changes, input voltage variation, and time.

Types of References

The majority of available IC reference circuits use the bandgap principle: the V_{BE} of any silicon transistor has a negative tempco of about 2mV/°C, which can be extrapolated to approximately 1.2 volts at absolute zero (the *bandgap* voltage of silicon). Since identical transistors operating at constant current densities will have predictably different temperature coefficients of base-emitter voltage, it is possible to arrange circuit elements so as to null out the temperature coefficients associated with the two phenomena and produce a constant voltage (usually 1.2 volts). This temperature-invariant voltage can be amplified and buffered to produce a standard voltage value, such as 2.5V or 10.0V. The bandgap types catalogued here include the AD1403 and the AD580 (2.5V), the AD581 (10.0V), and the multi-output AD584 (2.5, 5.0, 7.5, and/or 10.0V).

Another popular form of reference circuit uses a selected low-drift Zener diode, followed by a buffer-amplifier-and-precision-gain stage to provide a standard output voltage. The AD2710, AD2712 families provide +10V and ±10V (dual output) using this technique. Laser-trimmed thin-film resistors are essential to secure ±1mV accuracy and ±1ppm/°C max drift in these hybrid devices.

The AD589 family are two-terminal 1.2V bandgap ICs used like Zener diodes. They are ideally suited to battery-powered instruments or portable equipment where low power consumption (and often low supply voltages) are essential. Power requirements as low as 60μW, combined with low temperature drift, provide precision performance at low cost.

Definitions of Specifications

Line regulation. The change in output voltage due to a specified change in input voltage. It is usually expressed in percent per volt or microvolts per volt of input change.

Load regulation. The change in output voltage for a specified change in load current. It is generally expressed in microvolts per milliampere, or ohms of dc output resistance. This specification includes the effect of self-heating due to increased power dissipation at higher load currents.

Output voltage tolerance. The deviation from the nominal output voltage at 25°C and specified input voltage as measured by a device traceable to a recognized fundamental voltage standard.

Output voltage change with temperature. The change in output voltage from the value at 25°C ambient; it is independent of variations in the other operating conditions. Analog Devices specifies both an error band and an equivalent temperature coefficient (in ppm/°C) for most references. The error band (e.g., ±5mV, −55°C to +125°C), is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{max} and 25°C to T_{min}, with a slope equal to the stated temperature coefficient. Thus, the total absolute error for a particular reference over its specified temperature range is equal to the output voltage tolerance at 25°C plus the error band.

Turn-on settling time. The time, from a cold start, for the reference output to settle within a specified error band. This definition relates only to the electrical turn-on of the chip, and does not include thermal settling time, which depends on the package, heat-sinking, and load-current change.

ANALOG DEVICES

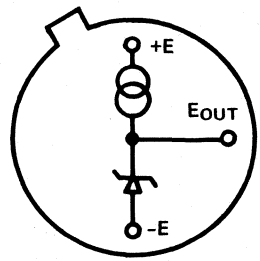
High Precision 2.5 Volt IC Reference

AD580*

FEATURES

- Laser Trimmed to Higher Accuracy: 2.500V ±0.4%, Improved from ±1.0% (AD580M)
- 3-Terminal Device: Voltage In/Voltage Out
- Excellent Temperature Stability: 10ppm/°C (AD580M, U)
- Excellent Long Term Stability: 250μV (25μV/Month)
- Low Quiescent Current: 1.5mA max
- Small, Hermetic IC Package: TO-52 Can

AD580 FUNCTIONAL BLOCK DIAGRAM



TO-52
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD580 is an improved three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output for inputs between 4.5V and 30V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provide the AD580 with an improved initial tolerance of ±0.4%, a temperature stability of better than 10ppm/°C and long term stability of better than 250μV. In addition, the low quiescent current drain of 1.5mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580 allows operation with 5 volt logic supplies making the AD580 ideal for digital panel meter applications or whenever only a single logic power supply is available.

The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of −55°C to +125°C.

*Covered by Patent Nos. 3,887,863; RE30,586.

PRODUCT HIGHLIGHTS

1. Laser-trimming the thin-film resistors has reduced the AD580 output error. For example, AD580L output tolerance is now ±10mV, improved from ±50mV.
2. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
3. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for systems that contain a single logic power supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities to 10ppm/°C and long term stability better than 250μV.
5. The low quiescent current drain of the AD580 makes it ideal for CMOS and other low power applications.

SPECIFICATIONS (@ E_{IN} and 25°C)

Model	AD580J Min	AD580J Typ	AD580J Max	AD580K Min	AD580K Typ	AD580K Max	AD580L Min	AD580L Typ	AD580L Max	AD580M Min	AD580M Typ	AD580M Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			**±75**			**±25**			**±10**			**±10**	mV
OUTPUT VOLTAGE CHANGE													
T_{min} to T_{max}			**15**			**7**			**4.3**			**1.75**	mV
			85			40			25			10	ppm/°C
LINE REGULATION													
$7V \le V_{IN} \le 30V$		1.5	**6**		1.5	**4**			**2**			**2**	mV
$4.5V \le V_{IN} \le 7V$		0.3	**3**		0.3	**2**			**1**			**1**	mV
LOAD REGULATION													
ΔI = 10mA			**10**			**10**			**10**			**10**	mV
QUIESCENT CURRENT		1.0	**1.5**		1.0	**1.5**		1.0	**1.5**		1.0	**1.5**	mA
NOISE (0.1Hz to 10Hz)		60			60			60			60		µV (p-p)
STABILITY													
Long Term		250			250			250			250		µV
Per Month		25			25			25			25		µV
TEMPERATURE PERFORMANCE													
Specified	0		+70	0		+70	0		+70	0		+70	°C
Operating	−55		+125	−55		+125	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION[1] – TO-52	AD580JH			AD580KH			AD580LH			AD580MH			

Model	AD580S Min	AD580S Typ	AD580S Max	AD580T Min	AD580T Typ	AD580T Max	AD580U Min	AD580U Typ	AD580U Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			**±25**			**±10**			**±10**	mV
OUTPUT VOLTAGE CHANGE										
T_{min} to T_{max}			**25**			**11**			**4.5**	mV
			55			25			10	ppm/°C
LINE REGULATION										
$7V \le V_{IN} \le 30V$		1.5	**6**			**2**			**2**	mV
$4.5V \le V_{IN} \le 7V$		0.3	**3**			**1**			**1**	mV
LOAD REGULATION										
ΔI = 10mA			**10**			**10**			**10**	mV
QUIESCENT CURRENT		1.0	**1.5**		1.0	**1.5**		1.0	**1.5**	mA
NOISE (0.1Hz to 10Hz)		60			60			60		µV (p-p)
STABILITY										
Long Term		250			250			250		µV
Per Month		25			25			25		µV
TEMPERATURE PERFORMANCE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−55		+150	−55		+150	−55		+150	°C
Storage	−65		+175	−65		+175	−65		+175	°C
ABSOLUTE MAXIMUM RATINGS										
Input Voltage	40V									
Power Dissipation @ +25°C										
Ambient Temperature	350mW									
Derate above +25°C	2.8mW/°C									
Lead Temperature (Soldering, 10 sec)	300°C									
Thermal Resistance										
Junction-to-Case	100°C/W									
Junction-to-Ambient	360°C/W									
PACKAGE OPTION[1] – TO-52	AD580SH			AD580TH			AD580UH			

NOTES

[1]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

THEORY OF OPERATION

Most precision IC references use complex multichip hybrid designs based on expensive temperature-compensated zener diodes. Others are monolithic with on-chip zener diodes; these often require more than one power supply and, with the zener breakdown occuring near 6.3 volts, will not operate from a low voltage logic supply.

The AD580 family (AD580, AD581, AD584, AD589) uses the "bandgap" concept to produce a stable, low-temperature-coefficient voltage reference suitable for high accuracy data-acquisition components and systems. The device makes use of the underlying physical nature of a silicon transistor base-emitter voltage in the forward-biased operating region. All such transistors have approximately a $-2mV/^{\circ}C$ temperature coefficient, unsuitable for use directly as a low TC reference; however, extrapolation of the temperature characteristic of any one of these devices to absolute zero (with emitter current proportional to absolute temperature) reveals that it will go to a V_{BE} of 1.205 volts 0K, as shown in Figure 1. Thus, if a voltage could be developed with an opposing temperature coefficient to sum with V_{BE} to total 1.205 volts, a zero-TC reference would result and operation from a single, low-voltage supply would be possible. The AD580 circuit provides such a compensating voltage, V_1 in Figure 2, by driving two transistors at different current densities and amplifying the resulting V_{BE} difference (ΔV_{BE} – which now has a positive TC); the sum (V_Z) is then buffered and amplified up to 2.5 volts to provide a usable reference-voltage output. Figure 3 is the schematic diagram of the AD580.

The AD580 operates as a three-terminal reference, that means that no additional components are required for biasing or current setting. The connection diagram, Figure 4 is quite simple.

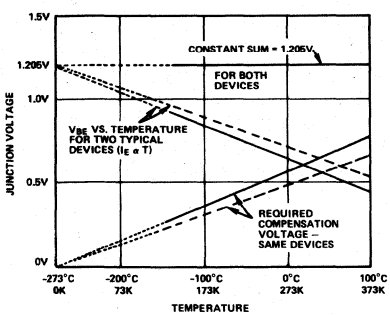


Figure 1. Extrapolated Variation of Base-Emitter Voltage with Temperature ($I_E \alpha T$), and Required Compensation, Shown for Two Different Devices

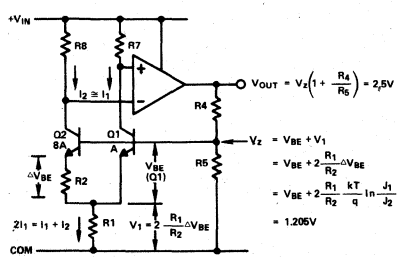


Figure 2. Basic Bandgap-Reference Regulator Circuit

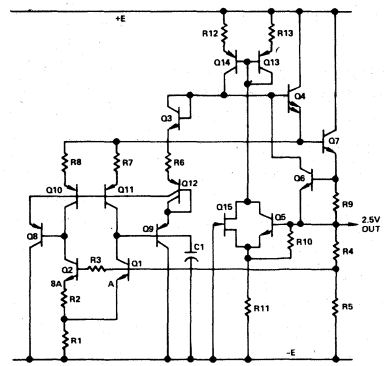


Figure 3. AD580 Schematic Diagram

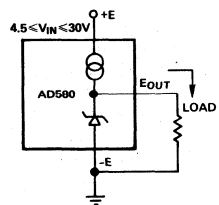


Figure 4. AD580 Connection Diagram

VOLTAGE VARIATION VS. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD580 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

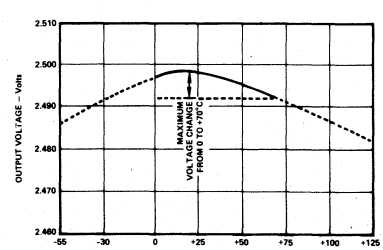


Figure 5. Typical AD580K Output Voltage vs. Temperature

The AD580M guarantees a maximum deviation of 1.75mV over the 0 to +70°C temperature range. This can be shown to be equivalent to 10ppm/°C average maximum; i.e. . .

$$\frac{1.75\text{mV max}}{70^\circ\text{C}} \times \frac{1}{2.5\text{V}} = 10\text{ppm}/^\circ\text{C max average}$$

The AD580 typically exhibits a variation of 1.5mV over the power supply range of 7 to 30 volts. Figure 6 is a plot of AD580 line rejection versus frequency.

NOISE PERFORMANCE

Figure 7 represents the peak-to-peak noise of the AD580 from 1Hz (3dB point) to a 3dB high end shown on the horizontal axis. Peak-to-peak noise from 1Hz to 1MHz is approximately 600μV.

THE AD580 AS A CURRENT LIMITER

The AD580 represents an excellent alternative to current limiter diodes which require factory-selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD580 approach is not limited to a specially selected factory set current limit; it can be programmed from 1 to 10mA with the insertion of a single external resistor. The approximate temperature coefficient of current limit for the AD580 used in this mode is 0.13%/°C for I_{LIM} = 1mA and 0.01%/°C for I_{LIM} = 13mA (see Figure 9). Figure 8 displays the high output impedance of the AD580 used as a current limiter for I_{LIM} = 1, 2, 3, 4, 5mA.

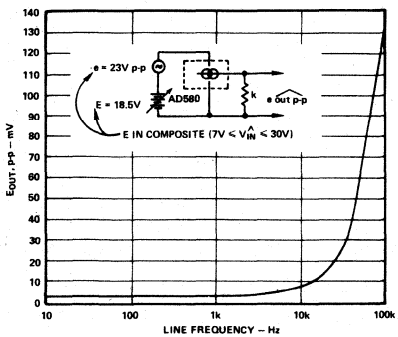


Figure 6. AD580 Line Rejection Plot

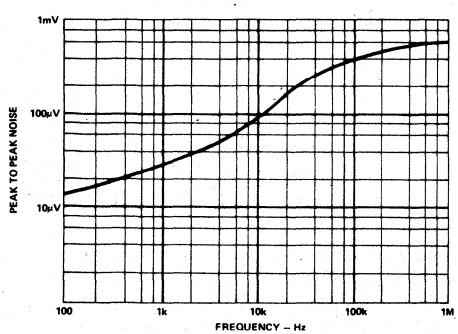


Figure 7. Peak-to-Peak Output Noise vs. Frequency

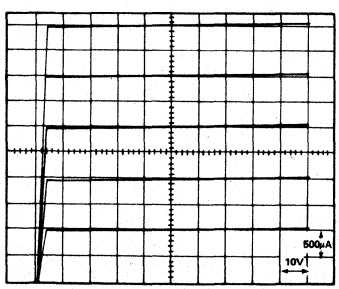


Figure 8. Input Current vs. Input Voltage (Integral Loads)

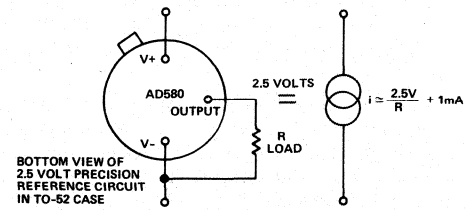


Figure 9. A Two-Component Precision Current Limiter

THE AD580 AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD580 has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

Figure 10 shows the AD580 used as a reference for the AD7542 12-bit CMOS DAC with complete microprocessor interface. The AD580 and the AD7542 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7542 includes three 4-bit data registers, a 12-bit DAC register, and address decoding logic; it may thus be interfaced directly to a 4-, 8- or 16-bit data bus. Only 8mA of quiescent current from the single +5 volt supply is required to operate the AD7542 which is packaged in a small 16-pin DIP. The AD544 output amplifier is also low power, requiring only 2.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7542KN without user trims and it typically settles to ±1/2 LSB in less than 3μs. It will provide the 0 to -2.5 volt output swing from ±5 volt supplies.

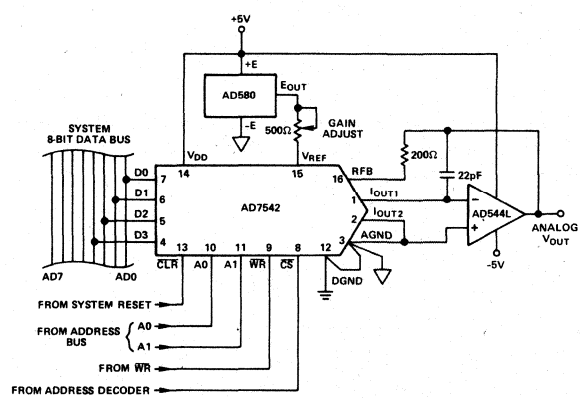


Figure 10. Low Power, Low Voltage Reference for the AD7542 Microprocessor-Compatible 12-Bit DAC

ANALOG DEVICES

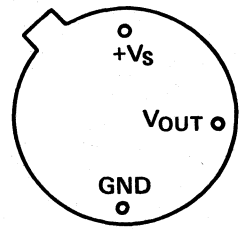
High Precision 10 Volt IC Reference

AD581*

FEATURES

- Laser-Trimmed to High Accuracy:
  - 10.000 Volts ±5mV (L and U)
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (L)
  - 10ppm/°C max, -55°C to +125°C (U)
- Excellent Long-Term Stability:
  - 25ppm/1000 hrs. (Non-Cumulative)
- Negative 10 Volt Reference Capability
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- 3-Terminal TO-5 Package

AD581 PIN CONFIGURATION



TO-5
BOTTOM VIEW

7

PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.

*Covered by Patent Nos. 3,887,863; RE 30,586

SPECIFICATIONS (@ V_{IN} = +15V and 25°C)

Model	AD581J			AD581K			AD581L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			±5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			**±13.5**			**±6.75**			±2.25	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			5	ppm/°C
LINE REGULATION										
$15V \leq V_{IN} \leq 30V$			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
$13V \leq V_{IN} \leq 15V$			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			µA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Specified	0		+70	0		+70	0		+70	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE: TO-5[2]	AD581JH			AD581KH			AD581LH			

NOTES
[1]See Figure 6.
[2]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD581S			AD581T			AD581U			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE										
(Error from nominal 10,000V output)			**±30**			**±10**			**±5**	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			**±30**			**±15**			**±10**	mV
Value, T_{min} to T_{max}										
(Temperature Coefficient)			30			15			10	ppm/°C
LINE REGULATION										
$15V \leq V_{IN} \leq 30V$			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
$13V \leq V_{IN} \leq 15V$			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	200			200			200			µA
Sink −55°C to +85°C	5			5			5			mA
TEMPERATURE RANGE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE: TO-5[2]	AD581SH			AD581TH			AD581UH			

NOTES
[1]See Figure 6.
[2]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Applying the AD581

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

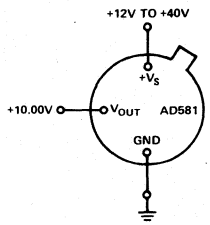
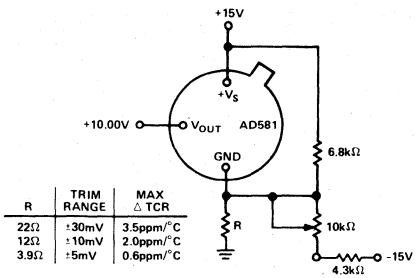


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.



R	TRIM RANGE	MAX Δ TCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration

ABSOLUTE MAXIMUM RATING

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . . . -55°C to +150°C
Lead Temperature
Soldering, 10sec . . . . . 300°C
Thermal Resistance
Junction-to-Ambient . . . . . 150°C/W

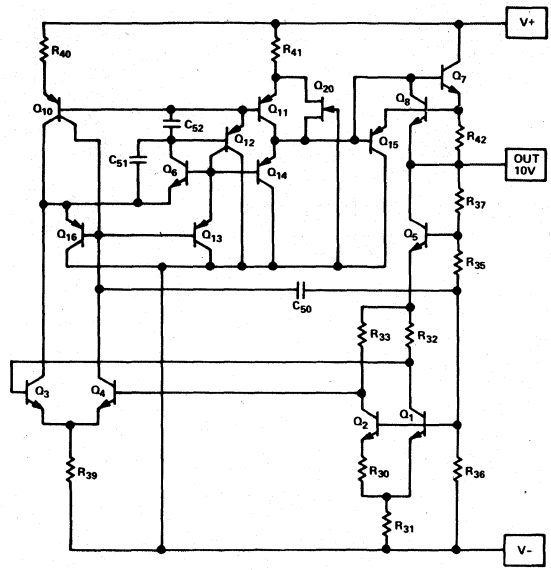
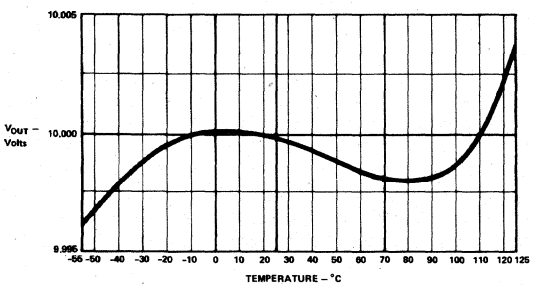


Figure 3. Simplified Schematic

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Five-point measurement of each device guarantees the error band over the -55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).



OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

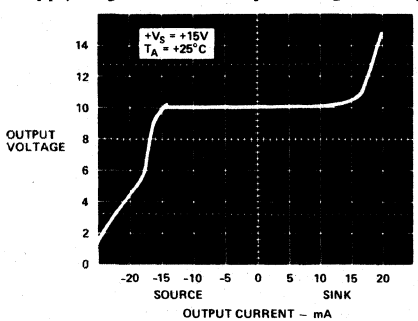


Figure 5. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

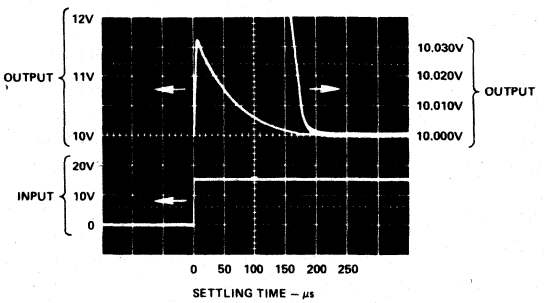


Figure 6. Output Settling Characteristic

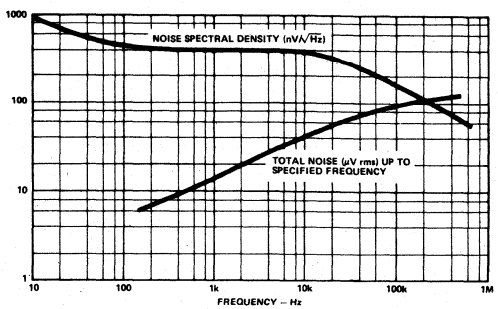


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

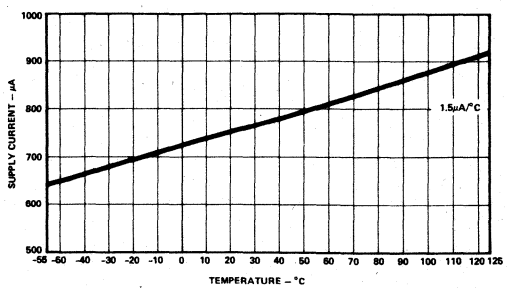


Figure 8. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

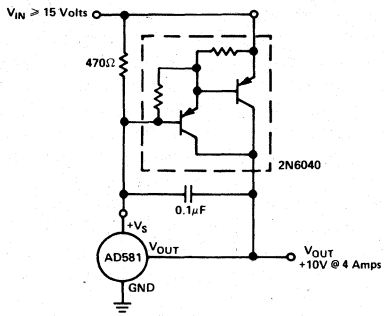


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 10. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

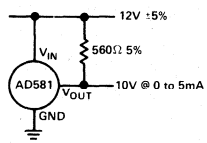


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

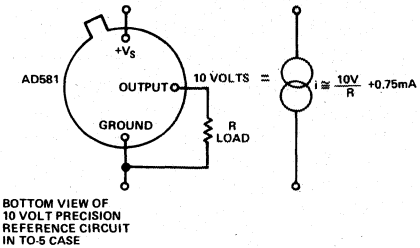


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "zener" mode to provide a precision -10.00 volt reference. As shown in Figure 12, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

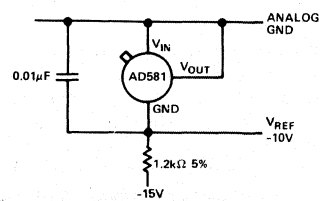


Figure 12. Two-Terminal -10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 13, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to −10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its −10 volt "zener" mode, as shown in Figure 12 (the $-10V_{REF}$ output is connected directly to the $V_{REF\ IN}$ of the CMOS DAC). The AD581 will normally be used in the −10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 14. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

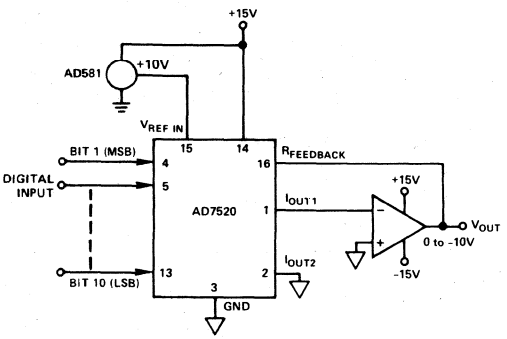


Figure 13. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

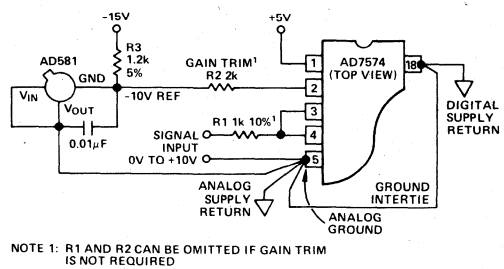


Figure 14. AD581 as Negative 10-Volt Reference for CMOS ADC

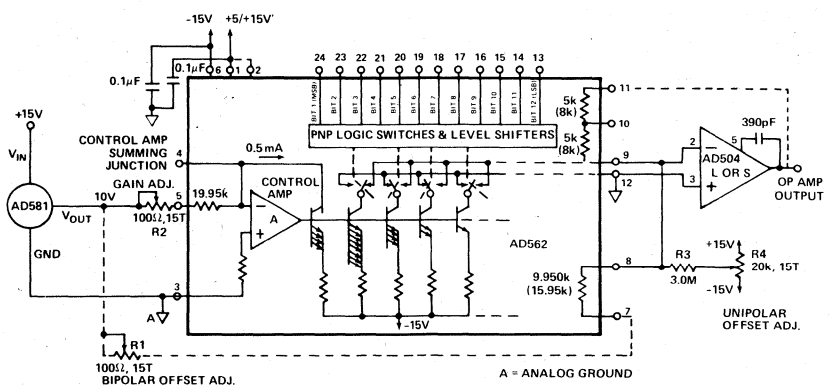


Figure 15. Precision 12-Bit D/A Converter

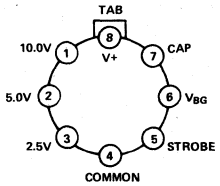
Pin Programmable Precision Voltage Reference

AD584*

FEATURES

- Four Programmable Output Voltages:
  - 10.000V, 7.500V, 5.000V, 2.500V
- Laser-Trimmed to High Accuracies
- No External Components Required
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (AD584LH)
  - 15ppm/°C max, -55°C to +125°C (AD584TH)
- Zero Output Strobe Terminal Provided
- Two Terminal Negative Reference Capability (5V & Above)
- Output Sources or Sinks Current
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability

AD584 PIN CONFIGURATION



TO-99
TOP VIEW

7

PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C; the AD584S and T are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed eight-terminal TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).

SPECIFICATIONS (@ V_{IN} = 15V and 25°C)

Model	AD584J			AD584K			AD584L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE										
Maximum Error[1] for Nominal										
Outputs of:										
10.000V			**±30**			**±10**			**±5**	mV
7.500V			**±20**			**±8**			**±4**	mV
5.000V			**±15**			**±6**			**±3**	mV
2.500V			**±7.5**			**±3.5**			**±2.5**	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C										
Value, T_{min} to T_{max}[2]										
10.000, 7.500, 5.000V Outputs			**30**			**15**			**5**	ppm/°C
2.500V Output			**30**			**15**			**10**	ppm/°C
Differential Temperature										
Coefficients Between Outputs		5			3			3		ppm/°C
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
Temperature Variation		1.5			1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE										
(0.1 to 10Hz)		50			50			50		µV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
LINE REGULATION (No Load)										
$15V \leq V_{IN} \leq 30V$			**0.002**			**0.002**			**0.002**	%/V
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$			**0.005**			**0.005**			**0.005**	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$, All Outputs		20	**50**		20	**50**		20	**50**	ppm/mA
OUTPUT CURRENT										
$V_{IN} \geq V_{OUT} + 2.5V$										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			mA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Operating	0		+70	0		+70	0		+70	°C
Storage	−65		+175	−65		+175	−65		+175	°C
PACKAGE (H08A)[3]	AD584JH			AD584KH			AD584LH			

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD584S			AD584T			
	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE TOLERANCE							
Maximum Error[1] for Nominal Outputs of:							
10.000V			±30			±10	mV
7.500V			±20			±8	mV
5.000V			±15			±6	mV
2.500V			±7.5			±3.5	mV
OUTPUT VOLTAGE CHANGE							
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]							
10.000, 7.500, 5.000V Outputs			30			15	ppm/°C
2.500V Output			30			20	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200		µs
NOISE (0.1 to 10Hz)		50			50		µV p-p
LONG-TERM STABILITY		25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30		mA
LINE REGULATION (No Load)							
$15V \leq V_{IN} \leq 30V$			0.002			0.002	%/V
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$			0.005			0.005	%/V
LOAD REGULATION							
$0 \leq I_{OUT} \leq 5mA$, All Outputs		20	50		20	50	ppm/mA
OUTPUT CURRENT							
$V_{IN} \geq V_{OUT} + 2.5V$							
Source @ +25°C	10			10			mA
Source T_{min} to T_{max}	5			5			mA
Sink T_{min} to T_{max}	200			200			mA
Sink −55°C to +85°C	5			5			mA
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	°C
PACKAGE (H08A)[3]	AD584SH			AD584TH			
ABSOLUTE MAX RATINGS							
Input Voltage V_{IN} to Ground	40V						
Power Dissipation @ +25°C	600mW						
Operating Junction Temp. Range	−55°C to +125°C						
Lead Temperature Soldering, 10sec)	300°C						
Thermal Resistance Junction-to-Ambient	150°C/Watt						

NOTES
[1]At Pin 1
[2]Calculated as average over the operating temperature range.
[3]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Applying the AD584

APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

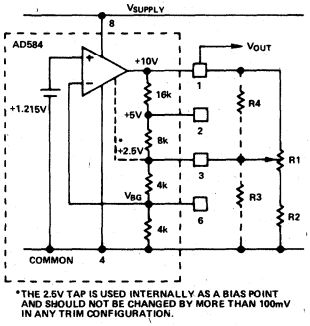


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

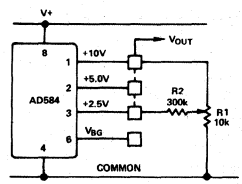


Figure 2. Output Trimming

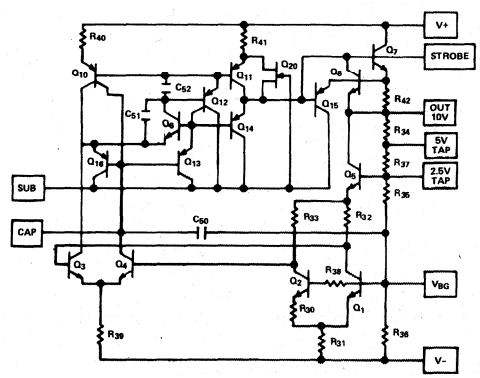


Figure 3. Schematic Diagram

PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at five temperatures over the -55°C to +125°C range to ensure that each device falls within the Maximum Error Band (see Figure 4) specified for a particular grade (i.e., S and T grades); three-point measurement guarantees performance within the error band from 0 to +70°C (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at +25°C. Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is ±10mV and the error band is ±15mV. Hence, the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C.

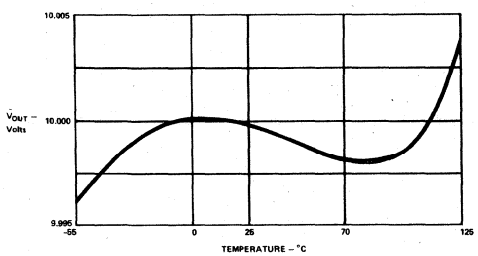


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

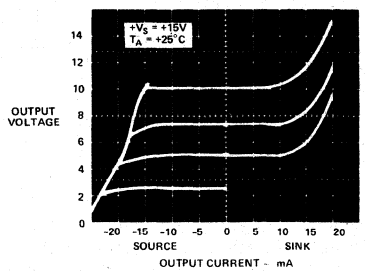


Figure 5. AD584 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD584. Figure 6a is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

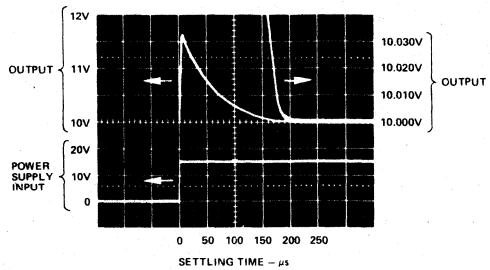


Figure 6. Output Settling Characteristic

NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between 0.01μF and 0.1μF connected between the Cap and V_{BG} terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 8.

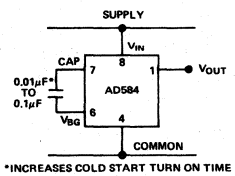


Figure 7. Additional Noise Filtering with an External Capacitor

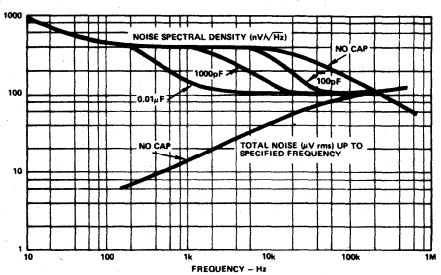


Figure 8. Spectral Noise Density and Total rms Noise vs. Frequency

Applications of the AD584

USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 9 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 9.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

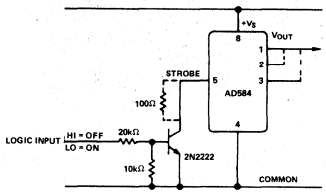


Figure 9. Use of the Strobe Terminal

PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 10 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

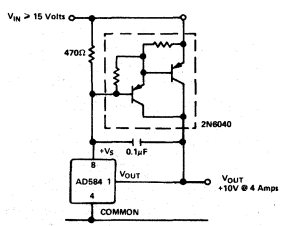


Figure 10. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 11. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 12). Of course, the minimum voltage required to drive the connection is 5 volts.

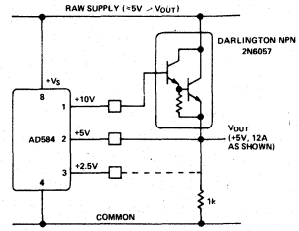


Figure 11. NPN Output Current Booster

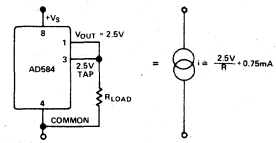


Figure 12. A Two-Component Precision Current Limiter

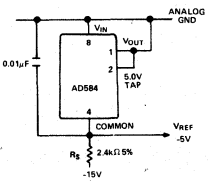


Figure 13. Two-Terminal -5 Volt Reference

NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision -10, -7.5 or -5.0 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of V_{OUT}. With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD584 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD584 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA.

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up as shown in Figure 14, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. The AD584 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

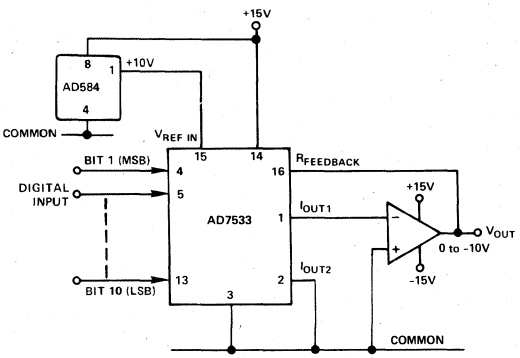
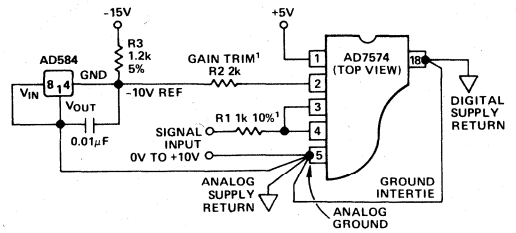


Figure 14. Low Power 10-Bit CMOS DAC Application

PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 15). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD584L (at 5ppm/°C) as the 10 volt reference



NOTE 1: R1 AND R2 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED

Figure 16. AD584 as Negative 10 Volt Reference for CMOS ADC

guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 17 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.

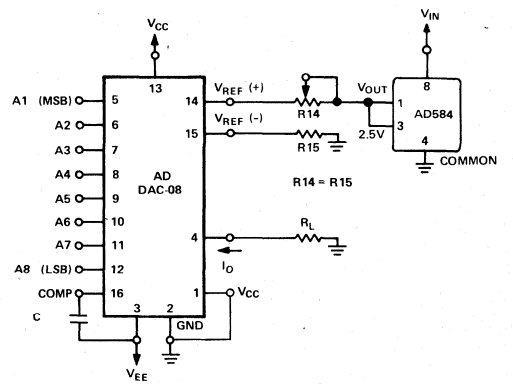


Figure 17. Current Output 8-Bit D/A

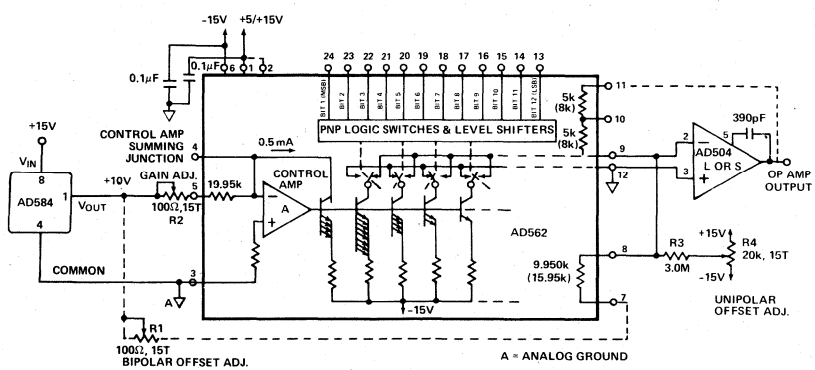


Figure 15. Precision 12-Bit D/A Converter

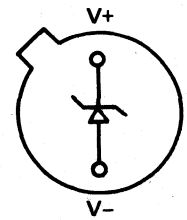
Two-Terminal IC 1.2 Volt Reference

AD589

FEATURES

- **Superior Replacement for Other 1.2V References**
- **Wide Operating Range: 50μA to 5mA**
- **Low Power: 60μW Total P_D at 50μA**
- **Low Temperature Coefficient:**
  - **10ppm/°C max, 0 to +70°C (AD589M)**
  - **25ppm/°C max, -55°C to +125°C (AD589U)**
- **Two Terminal "Zener" Operation**
- **Low Output Impedance: 0.6Ω**
- **No Frequency Compensation Required**
- **Low Cost**

AD589 FUNCTIONAL BLOCK DIAGRAM



BOTTOM VIEW

7

PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0 to +70°C operation, while the S, T and U grades are rated for the full -55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6Ω and temperature coefficients as low as 10ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50μA (60μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589 is an exact replacement for other 1.2V references, offering superior temperature performance and reduced sensitivity to capacitive loading.

SPECIFICATIONS (typical @ I_{IN} = 500μA and T_A = 25°C unless otherwise noted)

Model	AD589JH	AD589KH	AD589LH	AD589MH	AD589SH	AD589TH	AD589UH
ABSOLUTE MAXIMUM RATINGS							
Current	10mA	*	*	*	*	*	*
Reverse Current	10mA	*	*	*	*	*	*
Power Dissipation[1]	125mW	*	*	*	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*	*	*	*
Operating Junction Temperature Range	−55°C to +150°C	*	*	*	*	*	*
Lead Temperature (Soldering, 10sec)	300°C	*	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	*	−55°C to +125°C	**	**
OUTPUT VOLTAGE, T_a = 25°C	1.200V min	*	*	*	*	*	*
	1.235V typ	*	*	*	*	*	*
	1.250V max	*	*	*	*	*	*
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA − 5mA)	5mV max	*	*	*	*	*	*
DYNAMIC OUTPUT IMPEDANCE	0.6Ω typ	*	*	*	*	*	*
	2Ω max	*	*	*	*	*	*
RMS NOISE VOLTAGE 10Hz < f < 10kHz	5μV	*	*	*	*	*	*
TEMPERATURE COEFFICIENT[2] − ppm/°C	100 max	50 max	25 max	10 max	100 max	50 max	25 max
TURN-ON SETTLING TIME TO 0.1%	25μs	*	*	*	*	*	*
OPERATING CURRENT[3]	50μA min	*	*	*	*	*	*
	5mA max	*	*	*	*	*	*
PACKAGE STYLE:[4] H2A	H	*	*	*	*	*	*

NOTES
[1] Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and $\theta_{JA} = 400°C/W$.
[2] See following page for explanation of temperature coefficient measurement method.
[3] Optimum performance is obtained at currents below 500μA. Stray shunt capacitances should be minimized. If strays cannot be avoided, a shunt capacitor of at least 1000pF is recommended.
[4] See Section 19 for package outline information.

*Specifications same as AD589J.
**Specifications same as AD589S.
Specifications subject to change without notice.

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD589 consistently follows the curve shown in Figure 1. Three-point measurement guarantees the error band over the specified temperature range. The temperature coefficients specified on page 2 represent the slopes of the diagonals of the error band from +25°C to T_{min} and +25°C to T_{max}.

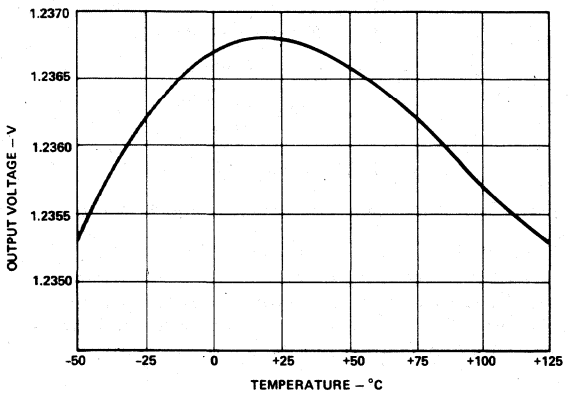


Figure 1. Typical AD589 Temperature Characteristics

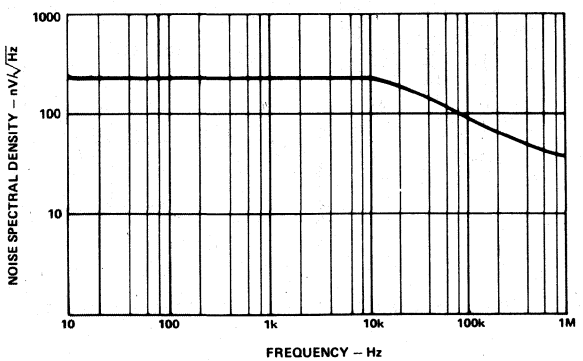


Figure 2. Noise Spectral Density

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 3 displays the turn-on characteristic of the AD589. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 25μs, and there is no long thermal tail appearing after that point.

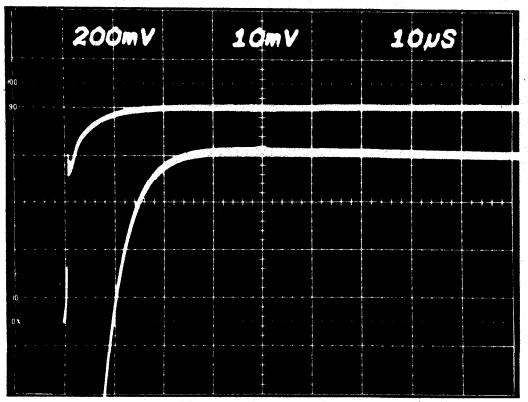


Figure 3. Output Settling Characteristics

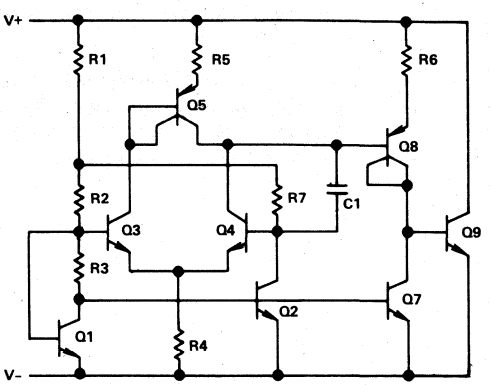


Figure 4. Schematic Diagram

APPLICATION INFORMATION

The AD589 functions as a two-terminal shunt-type regulator. It provides a constant 1.23V output for a wide range of input current from 50μA to 5mA. Figure 5 shows the simplest configuration for an output voltage of 1.2V or less. Note that no frequency compensation is required. If additional filtering is desired for ultra low noise applications, minimum recommended capacitance is 1000pF.

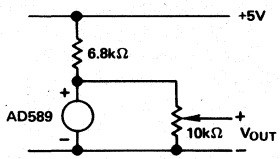


Figure 5. Basic Configuration for 1.2V or Less

The AD589 can also be used as a building block to generate other values of reference voltage. Figure 6 shows a circuit which produces a buffered 10V output. Total supply current for this circuit is approximately 2mA.

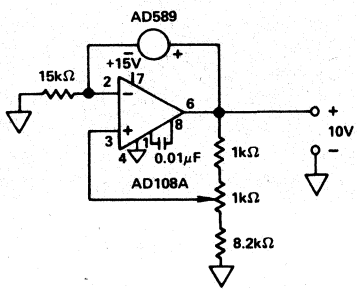
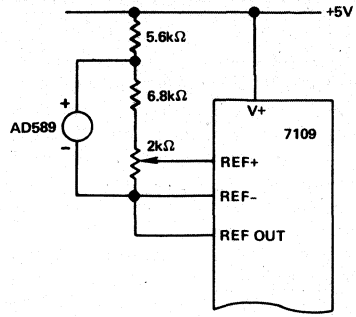
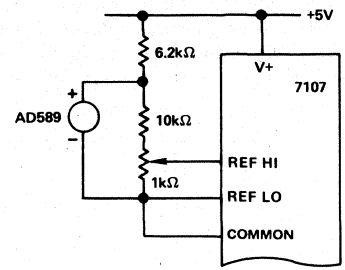


Figure 6. Single-Supply Buffered 10V Reference

The low power operation of the AD589 makes it ideal for use in battery operated portable equipment. It is especially useful as a reference for CMOS analog-to-digital converters. Figure 7 shows the AD589 used in conjunction with two popular integrating type CMOS A/D converters.



a. With 7109 12-Bit Binary A/D



b. With 7107 Panel Meter A/D

Figure 7. AD589 Used as Reference for CMOS A/D Converters

The AD589 also is useful as a reference for CMOS multiplying DACs such as the AD7533. These DACs require a negative reference voltage in order to provide a positive output range. Figure 8 shows the AD589 used to supply an equivalent −1.0V reference to an AD7533.

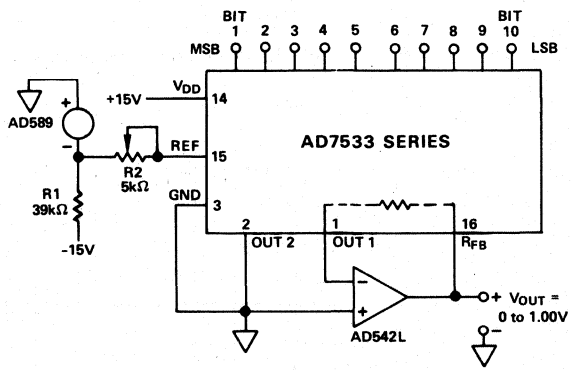


Figure 8. AD589 as Reference for 10-Bit CMOS DAC

ANALOG DEVICES

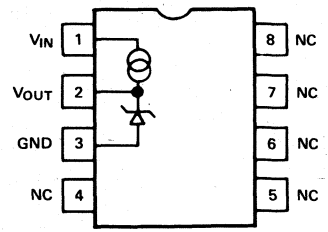
Low Cost, Precision 2.5 Volt IC Reference

AD1403/AD1403A*

FEATURES

Improved, Lower Cost, Replacements for Standard 1403, 1403A
3-Terminal Device: Voltage In/Voltage Out
Laser Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)
Excellent Temperature Stability: 25ppm/°C (AD1403A)
Low Quiescent Current: 1.5mA max
10mA Current Output Capability
Convenient MINI-DIP Package

AD1403/AD1403A
FUNCTIONAL BLOCK DIAGRAM



8-PIN MINI-DIP

7

PRODUCT DESCRIPTION

The AD1403 and AD1403A are improved three-terminal, low cost, temperature compensated, bandgap voltage references that provide a fixed 2.5V output voltage for inputs between 4.5V and 40V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provides the AD1403/AD1403A with an initial tolerance of ±10mV and a temperature stability of better than 25ppm/°C. In addition, the low quiescent current drain of 1.5mA (max) offers a clear advantage over classical zener techniques.

The AD1403 or AD1403A is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD1403/AD1403A allows operation with 5 volt logic supplies, making these devices ideal for digital panel meter applications and when only a single logic supply is available.

The AD1403 and AD1403A are specified for operation over the 0 to +70°C temperature range. The AD580 series of 2.5 volt precision IC references is recommended for applications where operation over the −55°C to +125°C range is required.

*Covered by Patent Numbers: 3,887,863; RE30,586.

PRODUCT HIGHLIGHTS

1. The AD1403A offers improved initial tolerance over the industry-standard 1403A: ±10mV versus ±25mV at a lower cost.
2. The three-terminal voltage in/voltage out operation of the AD1403/AD1403A provides a regulated output voltage without any external components.
3. The AD1403/AD1403A provides a stable 2.5V output voltage for input voltages between 4.5V and 40V making these devices ideal for systems that contain a single logic supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD1403A with temperature stabilities of 25ppm/°C.
5. The low 1.5mA maximum quiescent current drain of the AD1403 and AD1403A makes them ideal for CMOS and other low power applications.

SPECIFICATIONS (V_{IN} = 15V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0mA)	V_O				
AD1403		2.475	2.500	2.525	V
AD1403A		2.490	2.500	2.510	
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
AD1403		–	10	40	
AD1403A		–	10	25	
Output Voltage Change, 0 to +70°C	ΔV_O				mV
AD1403		–	–	7.0	
AD1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15V≤V_{IN}≤40V)		–	1.2	4.5	
(4.5≤V_{IN}≤15V)		–	0.6	3.0	
Load Regulation (0mA<I_O<10mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0mA)	I_I	–	1.2	1.5	mA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Storage Temperature	T_{STG}	-25 to 100	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

Specifications subject to change without notice.

ORDERING INFORMATION

Device	Initial Tolerance	Package[1]
AD1403N	±25mV	N8A
AD1403AN	±10mV	N8A

NOTE
[1] See Section 19 for package outline information.

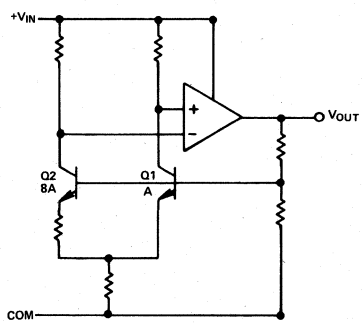


Figure 1. AD1043/AD1403A Functional Diagram

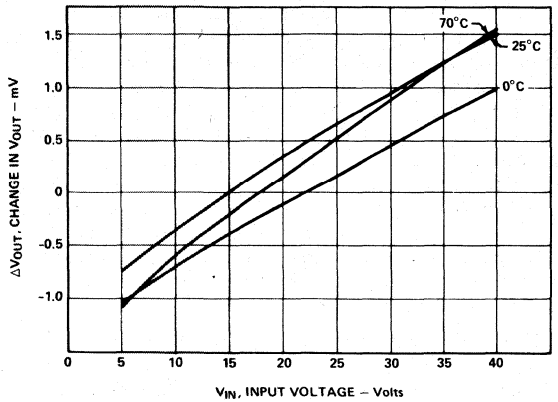


Figure 2. Typical Change in V_{OUT} vs. V_{IN} (Normalized to V_{OUT} @ V_{IN} = 15V @ T_C = 25°C)

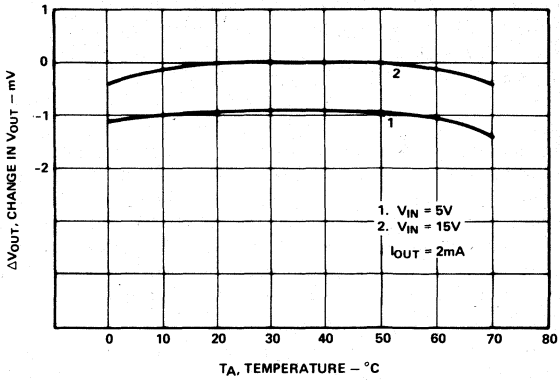


Figure 5. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V)

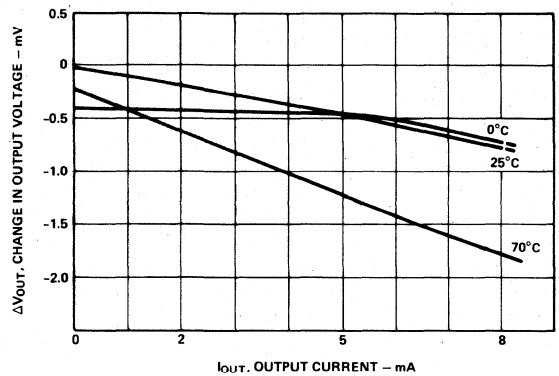


Figure 3. Change in Output Voltage vs. Load Current (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

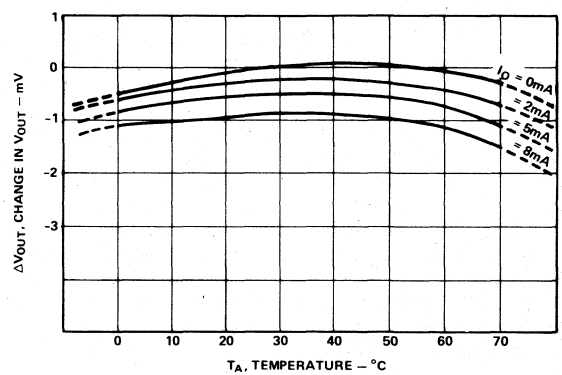


Figure 6. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

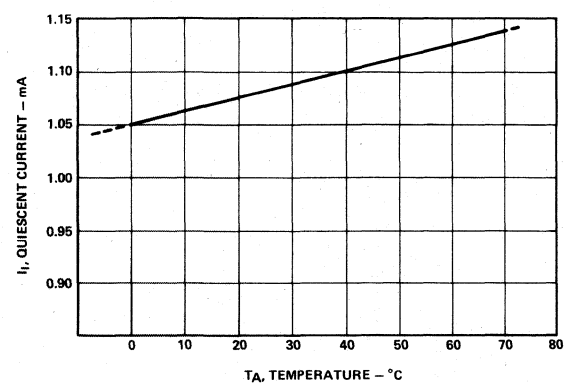


Figure 4. Quiescent Current vs. Temperature (V_{IN} = 15V, I_{OUT} = 0mA)

Applying the AD1403/AD1403A

VOLTAGE VARIATION VS. TEMPERATURE AND LINE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consisten Voltage vs. Temperature performance of a typical AD1403 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

The AD1403 exhibits a worst-case shift of 7.5mV over the entire range of operating input voltage, 4.5 volts to 40 volts. Typically, the shift is less than 1mV as shown in Figure 2.

THE AD1403A AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD1403A has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1.5mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

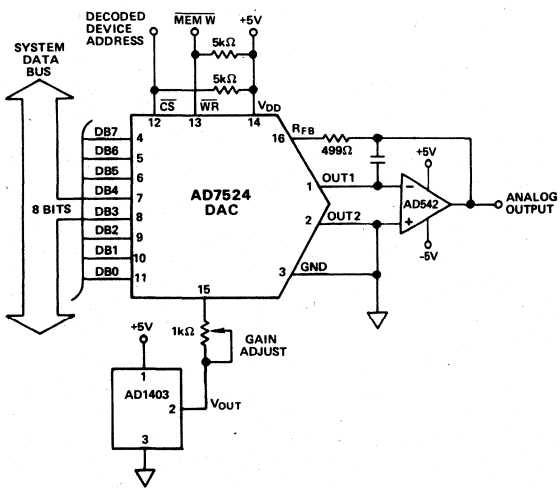


Figure 7. Low Power, Low Voltage Reference for the AD7524 Microprocessor-Compatible 8-Bit DAC

Figure 7 shows the AD1403A used as a reference for the AD7524 low-cost 8-bit CMOS DAC with complete microprocessor interface. The AD1403A and the AD7524 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7524 includes an 8-bit data register, and address decoding logic; it may thus be interfaced directly to an 8- or 16-bit data bus. Only 300μA of quiescent current from the single +5 volt supply is required to operate the AD7524 which is packaged in a small 16 pin DIP. The AD542 output amplifier is also low power, requiring only 1.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7524KN without user trims and it typically settles to ±1/2LSB in less than 5 microseconds. It will provide the 0 volt to -2.5 volt output swing from ±5 volt supplies.

THE AD1403 AS A PRECISION PROGRAMMABLE CURRENT SOURCE

The AD1403 is an excellent building block for precision current sources. Its wide range of operating voltages, 4.5V to 40V, along with excellent line regulation over that range (7.5mV) result in high insensitivity to varying load impedances. The low quiescent current (I_I) of 1.5mA (max) and the maximum specified maximum load current of 10mA allows the user to program current to any value between 1.5mA and 10mA.

Figure 8a shows the AD1403 connected as a current source. Total current is equal to the quiescent current plus the load current. Most of the temperature coefficient comes from the quiescent current term I_I, which has a typical TC of 0.13%/°C (1300ppm/°C). The load voltage (and hence current) TC is much lower at ±40ppm/°C max (AD1403). Therefore, the overall temperature coefficient decreases rapidly as the load current is increased. Figure 8b shows the typical temperature coefficient for currents between 1.5mA and 10mA. Use of an AD1403A will improve the TC appreciably.

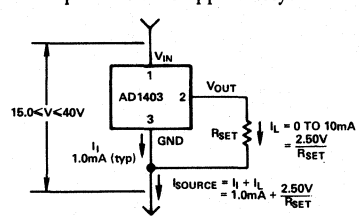


Figure 8a. The AD1403 as a Precision Programmable Current Source.

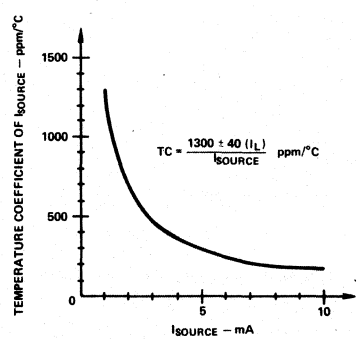


Figure 8b. Typical Temperature Coefficient of Current Source

ANALOG DEVICES

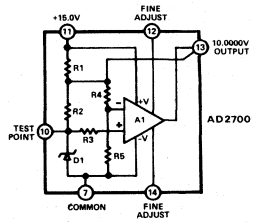
±10 Volt Precision Reference Series

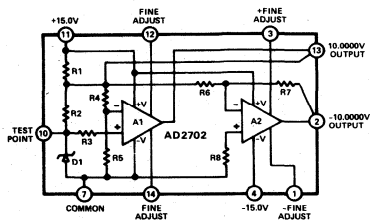
AD2700, AD2701, AD2702

FEATURES

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed -55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected

AD2700 SERIES FUNCTIONAL BLOCK DIAGRAMS





14-PIN DIP

PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with 52XX Series 12-bit A/D converters which require -10V external references for high accuracy over wide temperature ranges.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature performance results in very high accuracy over the temperature range without external components. The AD2700/01/02 LD grades have a maximum output voltage error at 25°C of ±2.5mV with no external adjustments.
2. The performance of the AD2700 series is achieved by a well-characterized design and precise control over the manufacturing process.
3. The AD2700 series is well suited for a broad range of applications requiring an accurate, stable reference source such as high resolution data converters (12 or 14 bits), test and measurement systems and calibration standards.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

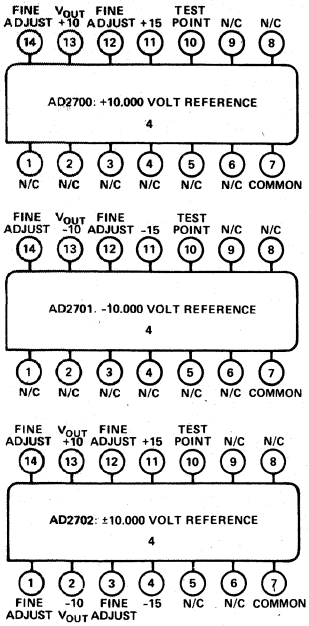
SPECIFICATIONS (maximum or minimum @ E_{IN} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted)

MODEL	JD	LD	SD	UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissipation @ +25°C – AD2700, 01	300mW	*	*	*
– AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE ERROR @ +25°C				
AD2700 10.000V	±0.005V	±0.0025V	*	**
AD2701 -10.000V	±0.005V	±0.0025V	*	**
AD2702 ±10.000V	±0.005V	±0.0025V	*	**
OUTPUT CURRENT[1] – @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE ERROR – AD2700,01	10ppm/°C	3ppm/°C	**	**
(T_{min} to T_{max})[2]	±11.0mV	±4.3mV	±8mV	±5.5mV
AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300μV/V	*	*	*
LOAD REGULATION				
0 to ±10mA	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT – AD2700, 01	±14mA	*	*	*
– AD2702	+17mA, -4mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. (typ)	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust (typ)	*	*	*
PACKAGE[3,4]	HY14B	HY14B	HY14D	HY14D

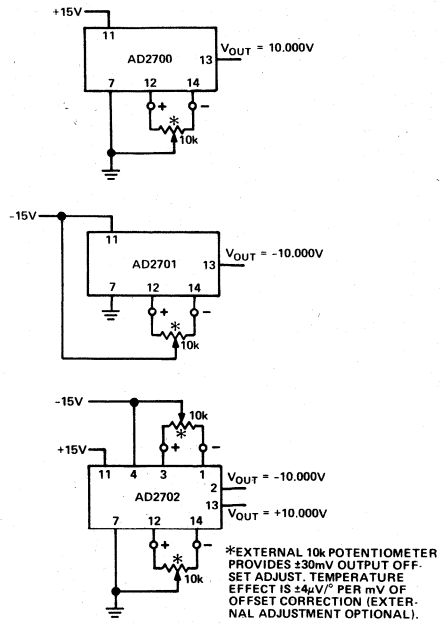
NOTES
*Same as "JD" grade performance.
**Same as "LD" grade performance.
***Same as "SD" grade performance.

[1] Specified with resistive load to common.
[2] Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.
[3] Analog Devices reserves the right to ship metal packages in lieu of the standard ceramic packages for J and L grade parts.
[4] See Section 19 for package outline information.

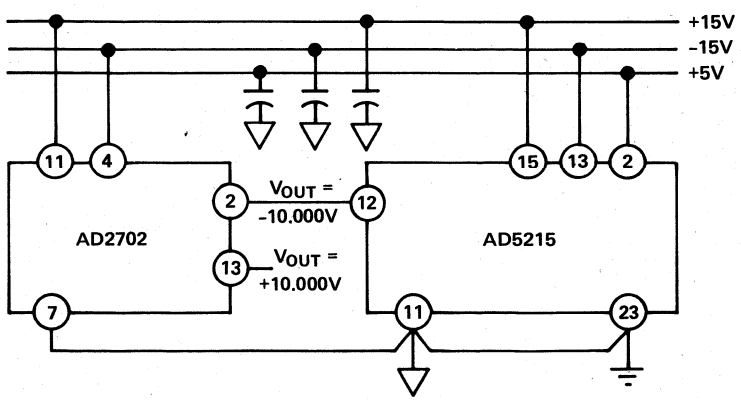
Specifications subject to change without notice.



Pin Designations



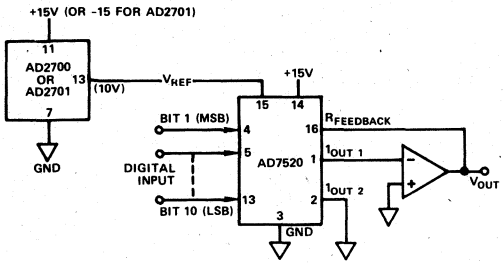
Fine Trim Connections



Using AD2702 Reference with the Fast, High Accuracy AD5215 – 12-Bit ADC

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to -10 volt output range. Alternatively, using the -10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of -10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 Data Sheet.

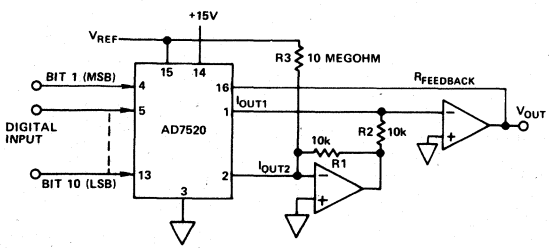


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

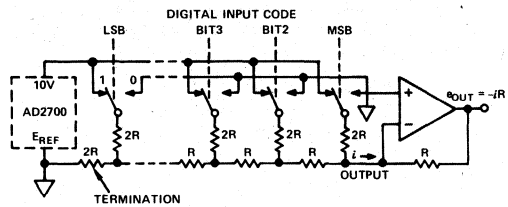
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

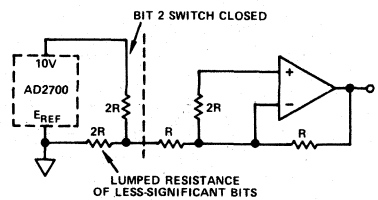
Table II. Code Table — Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

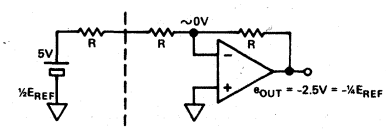
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4}E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence — because the amplifier summing point is at virtual ground — the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to 2^{-n} E_{REF}.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

ANALOG DEVICES

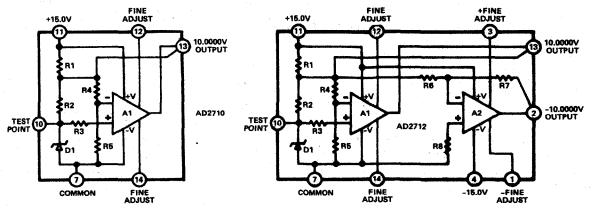
±10.000 Volt Ultra High Precision Reference Series

AD2710, AD2712

FEATURES

- **Laser Trimmed to High Accuracy: 10.000V ± 1.0mV**
- **Low Temperature Coefficient: 1ppm/°C (L Grade)**
- **Excellent Long Term Stability: 25ppm/1000hrs.**
- **5mA Output Current Capability**
- **Low Noise: 30μV p-p**
- **Short Circuit Protected**
- **No Heater Utilized**
- **Small Size (Standard 14-Pin DIP Package)**

AD2710, AD2712 FUNCTIONAL BLOCK DIAGRAMS



7

PRODUCT DESCRIPTION

The AD2710 and AD2712 are temperature-compensated, hybrid voltage references which provide precise 10.000V output from an unregulated input level from 13.5 to 16.5 volts. Active laser trimming is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in ultra high precision performance previously available only in oven-regulated modules. The 1.0mV maximum initial error and 1ppm/°C guaranteed maximum temperature coefficient of the AD2710L and AD2712L represent the best performance combination available without using ovens or heated substrates for temperature regulation.

The AD2710 series of precision 10.000 volt references offer the user unequalled accuracy and stability with performance guaranteed over the 0 to +70°C temperature range. The devices combine the recognized advantages of thin film technology and active laser trimming with a unique integrated ceramic package design to provide an excellent reference for use in applications requiring high accuracy and stability.

The AD2710 is recommended for use as a reference for 10-, 12- and 14-bit D/A converters which require an external reference. The device is also suitable for many types of high resolution A/D converters, either successive approximation or integrating designs. The 5mA output drive capability of the device also makes the AD2710 ideal for use as a master system reference.

For systems requiring a dual tracking reference, the AD2712 offers both positive and negative outputs in a single package. All units are packaged in an integrated ceramic 14-pin side-brazed package offering superior reliability over other package designs.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature coefficient results in very high accuracy over the temperature range without the use of external components. AD2710 has a maximum deviation from 10.000 volts of ±1.00mV at 25°C with no external adjustments.
2. The AD2710 and AD2712 are well suited for a broad range of applications requiring an accurate, stable reference source such as data converters, test and measurement systems and calibration standards.
3. The performance of the AD2710 series is achieved by a well-characterized design and close control over the manufacturing process. This eliminates the need for temperature-controlled ovens to provide stability.
4. The advanced multilayer integrated ceramic package results in superior electrical performance as well as inherent high reliability.

SPECIFICATIONS (typical @ V_S ±15V after a 5 minute warm-up at +25°C, no load condition unless otherwise specified)

Model		AD2710KN	AD2710LN	AD2712KN	AD2712LN
ABSOLUTE MAXIMUM RATINGS					
Input Voltage (for applicable supply)		±18V	*	*	*
Power Dissipation @ +25°C		300mW	*	450mW	**
Operating Temperature Range		0 to +70°C	*	*	*
Storage Temperature Range		−55°C to +100°C	*	*	*
Lead Temperature (soldering, 20s)		+260°C	*	*	*
Short Circuit Protection (to GND)		Continuous	*	*	*
OUTPUT VOLTAGE ERROR[1]					
+25°C		±1.0mV max	*	*	*
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT[2]					
+10V Output	+25°C to +70°C	±2ppm/°C max	±1ppm/°C max	±2ppm/°C max	±1ppm/°C max
	0 to +25°C	±5ppm/°C max	*[3]	*	*[3]
−10V Output[4]	+25°C to +70°C	Not Applicable	Not Applicable	±3ppm/°C max	±2ppm/°C max
	0 to +25°C	Not Applicable	Not Applicable	±5ppm/°C max	**
LINE REGULATION					
V_S = ±13.5 to ±16.5[5]		125μV/V(200μV/V max)	*	*	*
OUTPUT CURRENT		10mA	*	*	*
LOAD REGULATION					
I_O = 0 to ±5mA		50μV/mA(100μV/mA max)	*	*	*
OUTPUT RESISTANCE		0.05Ω	*	*	*
INPUT VOLTAGE[5]					
Operating Range		±13V to ±18V	*	*	*
Specified Performance		±13.5V to ±16.5V	*	*	*
QUIESCENT SUPPLY CURRENT					
V_S+		9mA(14mA max)	*	12mA (16mA max)	**
V_S−[5]		Not Applicable	Not Applicable	2mA (4mA max)	**
NOISE					
0.1 to 10Hz		30μV p-p	*	*	*
LONG TERM STABILITY					
T_A = +25°C		25ppm/1000 Hours	*	*	*
EXTERNAL TRIM RANGE[6]		±10mV	*	*	*
PACKAGE OPTION[7]		HY14B	*	*	*

NOTES
*Same as AD2710KN. **Same as AD2712KN performance.
[1] Specifications apply to both outputs of the AD2712.
[2] Refer to next page for definition of temperature-related error specifications.
[3] The AD2710LN and AD2712LN outputs are guaranteed for a maximum ±2ppm/°C temperature coefficient over the +15°C to +25°C temperature range. Refer to Figure 1.
[4] The +10V and −10V outputs of the AD2712 typically track within ±1ppm/°C over the specified temperature range.
[5] Negative power supply not required for AD2710.
[6] Use of the output trim will change the temperature coefficient approximately 0.3ppm/°C for each millivolt of adjustment.
[7] See Section 19 for package outline information.

Specifications subject to change without notice.

UNDERSTANDING THE SPECIFICATIONS

The AD2710 and AD2712 precision references are designed for applications requiring both the lowest possible initial error at room temperature and the lowest possible temperature drift. The specification for initial error is relatively straight-forward, and is the absolute error from exactly 10.000V. The specification for temperature drift, however, must be explained.

Various methods have been used to specify the temperature drift of voltage references, including the "butterfly", "box", and "modified-box" (or total error) methods. The AD2710 and AD2712 are specified with the "butterfly" method.

Using three or more temperatures provides the user with a tighter drift specification, eliminating possible mid-range excursions. The AD2710 and AD2712 have been designed and characterized as having a smooth drift curve with a virtually straight segment from +25°C to +70°C. The typical curve as shown is concave downward and gradually increases slope near 0°C.

As can be seen from Figure 1, the AD2710L and AD2712L +10V outputs will exhibit a maximum temperature coefficient of ±1ppm/°C (±2ppm/°C for "K" grade) from +25°C to +70°C. Over the short range between +15°C and +25°C, the AD2710L and AD2712L +10V outputs have a maximum drift of only ±2ppm/°C and a maximum drift of ±5ppm/°C from 0 to +15°C. The negative output of the AD2712L has a similar temperature coefficient characteristic with a maximum slope of ±2ppm/°C from +25°C to +70°C. This limit continues from +25°C to +15°C and then increases to a ±5ppm/°C maximum slope from +15°C and 0°C. Every unit is 100 percent tested and guaranteed to meet these specifications over the full 0 to +70°C temperature range.

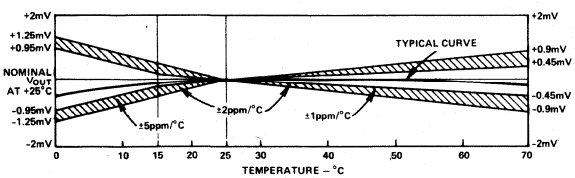


Figure 1. Maximum Change from +10V Output from +25°C Value vs. Temperature

All grades of the AD2710 and AD2712 are tested after a five minute warm-up period. This warm-up allows the entire circuit to attain thermal equilibrium. The warm-up drift is approximately 500 microvolts and is completely settled approximately three minutes after turn-on. Figure 2 shows the typical warm-up characteristics of the AD2710.

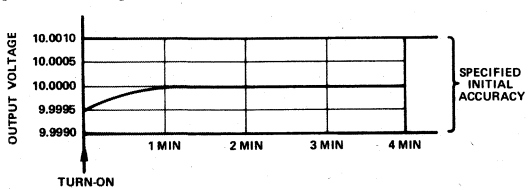


Figure 2. AD2710 Typical Warm-Up Drift

USING THE AD2710 AS A DAC REFERENCE

Digital-to-analog converters require a reference to establish the full scale output range. It is this reference which will ultimately determine the absolute accuracy of the converter. While many converters include internal reference sources, better overall performance can be obtained if a higher precision external reference is used.

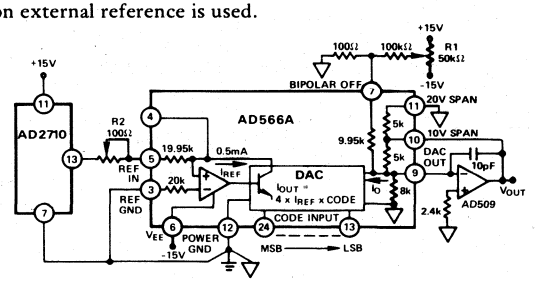


Figure 3. Low Drift 12-Bit D/A Converter

Figure 3 shows the AD2710 used with the AD566A high-speed 12-bit DAC. The AD566AKD is laser trimmed for ±1/4LSB maximum nonlinearity, and exhibits a gain temperature coefficient of 3ppm/°C. Use of the AD2710LN reference will result in a worst case total gain temperature coefficient of 4ppm/°C. After initial calibration of the DAC scale factor at room temperature, 12-bit absolute accuracy can be maintained over the +15°C to +70°C temperature range. The high output current capability of the AD2710 allows it to serve as a reference for up to 10 such converters in a system.

The resolution of the AD566A can be extended as shown in Figure 3 by summing the output of another DAC. In this example, an AD559 is used to provide 4 additional bits. Since the AD559 is driven from the same AD2710 reference as the AD566A which provides the higher-order bits, and uses a similar internal thin-film resistor ladder, it will exhibit first-order temperature tracking. While this circuit provides 16-bits of resolution, it is only as accurate as the AD566A used for the most significant bits. Use of an AD566AKD will typically achieve ±0.003% accuracy (±1/2LSB at 14 bits).

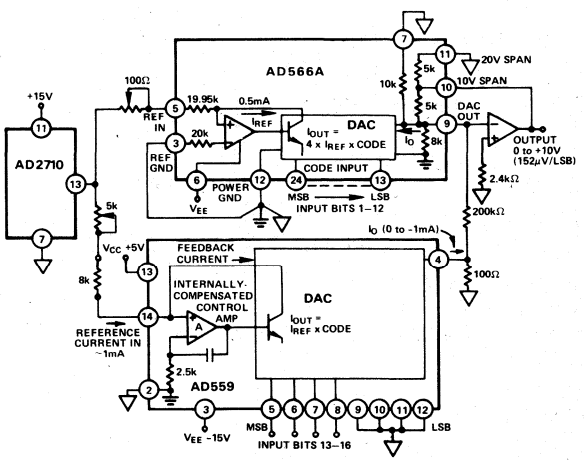


Figure 4. 16-Bit Binary DAC with AD2710 Reference

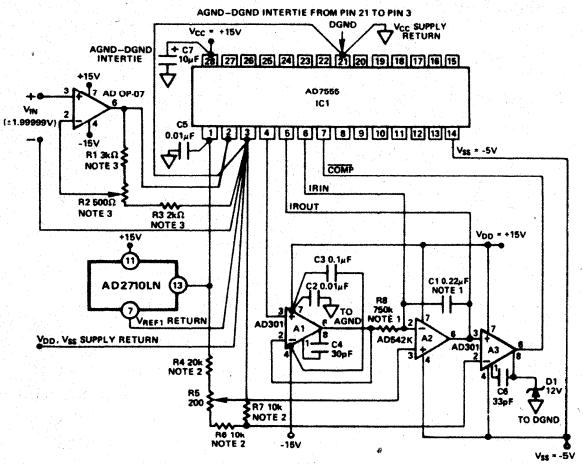
HIGH RESOLUTION ANALOG-TO-DIGITAL CONVERSION

The AD2710 is well-suited to both system and instrument-level analog-to-digital converter reference requirements. The excellent absolute accuracy and low temperature drift allow low-cost measurement systems to offer high levels of performance.

The AD7555 is a 4½/5½ digit ADC subsystem which uses the quad-slope conversion technique to achieve high accuracy at low cost. This patented conversion process performs automatic correction for offsets and other errors in the analog circuitry as a part of each conversion. Total scale factor drift 1.2ppm/°C is possible using the AD2710L reference and medium-precision external amplifiers. This represents a full scale drift of less than ±10 counts in ±200,000 from +15°C to +45°C. Less than 1 count of drift will occur in the 4 1/2 digit mode.

The AD7555 was designed for use with a 4.096V reference, which produces a ±2 volt input range. When the AD2710 is used, the input range is increased to ±4.88281V (24.4μV/count). The new scaling can be handled either by using a precision gain stage before the AD7555 analog input as shown or by using a microprocessor to digitally correct the scale. The actual input signal value can be computed by multiplying the count produced by the AD7555 by V_{REF1} (10 volts in this case), and dividing the result by 409600. Details of the digital circuitry of the AD7555 can be found on the AD7555 data sheet.

It should be noted that when the AD7555 is used with the AD2710 10 volt reference, it is necessary to use a V_{CC} greater than 10 volts. Thus the digital inputs and outputs of the ADC will be compatible with CMOS logic levels.



NOTES:
1. R8 C1 VALUES SHOWN ARE FOR 5 1/2 DIGIT MODE. FOR 4 1/2 DIGIT MODE R_8 = 360k, C_1 = 0.22μF. SUITABLE CAPACITORS AVAILABLE FROM COMPONENT RESEARCH CO. INC., 1655 26th STREET, SANTA MONICA, CA. 90404. (STOCK NUMBER FOR 0.22μF CAPACITOR IS D118224KXW).
2. R4, R6, R7 1% TOLERANCE
3. R1, R3 SHOULD TRACK WITHIN 0.5ppm/°C. EITHER BULK METAL OR WIRE-WOUND RESISTORS (OR A THIN-FILM NETWORK) SHOULD BE USED. R2 SHOULD BE A LOW-TC TYPE POTENTIOMETER OR A SELECTED LOW DRIFT FIXED RESISTOR.

Figure 5. High Accuracy Low Drift A/D Converter

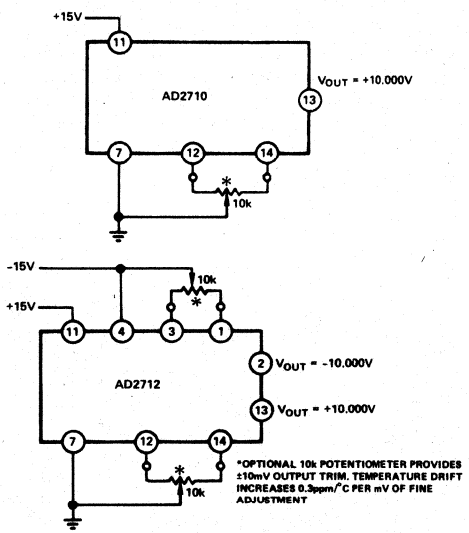


Figure 6. Optional Fine Trim Connections

CMOS Monolithic DC-DC Voltage Converter & Reference

AD7560

PRELIMINARY TECHNICAL DATA

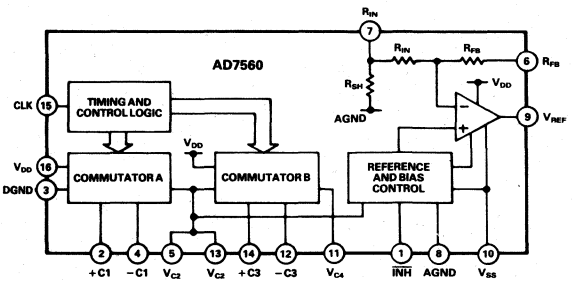
FEATURES

- Efficient Series Stacked dc/dc Converters Which Provide Multiple Outputs From a Single +5V Supply (−5V, −10V, −15V, +10V, +15V)
- On-Chip −10V Reference Voltage Output
- High Reference Voltage Power Supply Rejection
- Minimum Circuit Requires Only Two Low Cost Capacitors

APPLICATIONS

- Negative Reference Voltage Generation for Data Acquisition Systems, from a Single +5V Supply
- Op-Amp Supply Generation; ±5V, ±15V
- Low Power, High Efficiency Voltage Converter for Battery Operation

AD7560 FUNCTIONAL BLOCK DIAGRAM



7

GENERAL DESCRIPTION

The AD7560 is a monolithic CMOS voltage converter plus voltage reference circuit. It performs both voltage inversion and subsequent voltage multiplication of the incoming positive supply voltage. It contains two converter circuits, A and B, in series to provide two negative output voltages of approximately $-V_{DD}$ and $-3V_{DD}$ from the $+V_{DD}$ input. The unregulated $-3V_{DD}$ output from converter B is used to generate an internal reference voltage of −5V. This is buffered and amplified to provide a temperature compensated −10V output (V_{REF}, pin 9) which can sink over 1.0mA. In applications where the reference output is not required this section can be powered down via the reference inhibit input $\overline{INH}$, pin 1.

An on-chip oscillator is provided to drive the converters. The oscillator frequency is determined by the addition of an external capacitor. Additionally, if converter synchronization to an external clock source is required, the clock input can be driven directly from a 5V CMOS compatible clock source.

ORDERING INFORMATION

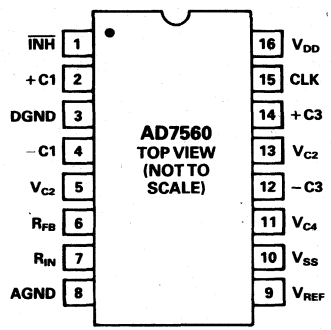
Reference Voltage Accuracy (T_{min} to T_{max})	Reference Voltage T.C. (max)	Temperature Range & Package[1] −25°C to +70°C Plastic
±500mV	±200ppm/°C	AD7560JN

NOTE
[1]Plastic DIP Package – N16B
See Section 19 for package outline information.

PRODUCT HIGHLIGHTS

1. The AD7560 produces multiple output voltages with a minimum number of external components, e.g., basic configurations require only two or four low cost general purpose electrolytic capacitors.
2. A −10V voltage reference output which can be powered down if not required.
3. The 5V CMOS compatible clock input can be driven from an external clock source (for synchronization) or can be made to oscillate with the addition of an external capacitor.
4. All outputs are short-circuit proof and latch-up free.

PIN CONFIGURATION



SPECIFICATIONS

(V_{DD} = +5V[1], F_{CLK} = 6kHz external clock, $0 \le I_{REF} \le 1mA$ (see test circuits, Figures 1 & 2). All specifications T_{min} to T_{max}[2] unless otherwise noted)

Parameter	$\overline{INH}$ = 0V[3]	$\overline{INH}$ = V_{DD}[4]	Units	Conditions/Comments
CONVERTER A, V_{C2} (Pins 5 & 13)				
Voltage Conversion Factor, α_A				
T_A = +25°C	0.90	0.68	min	$I_{C2} = I_{C4} = 0mA$
	0.95	0.80	typ	
T_{MIN}, T_{MAX}	0.85	0.65	min	
	0.90	0.75	typ	
V_{C2} Output Source Resistance				
T_A = +25°C	160	N.A.	Ω max	$I_{C2} = 5mA, I_{C4} = 0mA, I_{REF}$ = N.A. (Not Applicable)
	120	N.A.	Ω typ	
T_{MIN}, T_{MAX}	200	N.A.	Ω max	
T_A = +25°C	N.A.	160	Ω max	$I_{C2} = 1mA, I_{C4} = 0mA, 0 \le I_{REF} \le 0.25mA$
	N.A.	120	Ω typ	
T_{MIN}, T_{MAX}	N.A.	200	Ω max	
V_{C2} Short Circuit Current	30	30	mA typ	Short Circuit to DGND
CONVERTER B, V_{C4} (Pin 11)				
Voltage Conversion Factor, α_B				
T_A = +25°C	2.80	2.35	min	$I_{C2} = I_{C4} = 0mA$
	2.90	2.45	typ	
T_{MIN}, T_{MAX}	2.75	2.30	min	
	2.85	2.35	typ	
V_{C4} Output Source Resistance				
T_A = +25°C	900	N.A.	Ω max	$I_{C2} = 0mA, I_{C4} = 2.5mA, I_{REF}$ = N.A.
	750	N.A.	Ω typ	
T_{MIN}, T_{MAX}	1200	N.A.	Ω max	
T_A = +25°C	N.A.	900	Ω max	$I_{C2} = 0mA, I_{C4} = 0.25mA, 0 \le I_{REF} \le 0.25mA$
	N.A.	750	Ω typ	
T_{MIN}, T_{MAX}	N.A.	1200	Ω max	
V_{C4} Short Circuit Current	20	20	mA typ	Short Circuit to DGND
VOLTAGE REFERENCE[5], V_{REF} (Pin 9)				
Reference Voltage Output	N.A.	−10.00	V	
Reference Voltage Accuracy	N.A.	±500	mV max	
Reference Temperature Coefficient[6]	N.A.	±200	ppm/°C max	
Reference Voltage Drift	N.A.	±60	mV typ	1,000 hours, +70°C
Reference Sink Current, I_{REF}	N.A.	1.0	mA min	
		1.5	mA typ	
Reference Output Resistance	–	3	Ω max	
	20	1	kΩ typ	
Reference Short Circuit Current	0.4	5	mA max	Short Circuit to AGND
Power Supply Rejection				
V_{REF}/V_{DD}	N.A.	±12	mV/V max	
		±6	mV/V typ	
Buffer Amplifier Resistor Values				
R_{IN} and R_{FB}	30/50/75	30/50/75	kΩ min/typ/max	
Input Shunt Resistance, R_{SH}	75	75	kΩ typ	R_{SH} is Approximately $1.5R_{FB}$
DIGITAL INPUTS				
INH (Pin 1)				
V_{IH} Input High Voltage	+3.0	+3.0	V min	
V_{IL} Input Low Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	±10	±10	μA max	V_{IN} = 0V or V_{DD}
C_{IN} Input Capacitance[7]	7	7	pF max	
CLK (Pin 15)				
V_{IH} Input High Voltage	+3.0	+3.0	V min	
V_{IL} Input Low Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	±25	±25	μA max	V_{IN} = 0V or V_{DD}
	±15	±15	μA typ	
POWER REQUIREMENTS				
Power Supply Current, I_{DD}	6	22	mA max	$I_{C2} = I_{C4} = 0mA$
	3	15	mA typ	
	16	N.A.	mA max	$I_{C2} = 0mA, I_{C4} = 2.5mA$
	12	N.A.	mA typ	
V_{DD} Operating Range	+4.5/+5.5	+4.75/+5.5	V	Specifications not guaranteed outside V_{DD} = +5V ±5%
	+4.5/+7.5	+4.75/+7.5	V	Degraded performance over this range. External limit resistors required. See Figure 15.

NOTES

[1] V_{DD} = +5V ±5%.

[2] Temperature range of AD7560JN is −25°C to +70°C.

[3] See test circuit, Figure 1.

[4] See test circuit, Figure 2.

[5] To meet this voltage reference specification (T_{min} to T_{max}) external loading on V_{C2} (pins 5 & 13) and V_{C4} (pin 11) should be restricted to satisfy conditions $|V_{C4}| \ge |V_{REF}| + 0.5V$. Refer to Figures 4 and 9.

[6] Using internal resistors R_{FB} and R_{IN}.

[7] Guaranteed by design, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND	−0.3V, +8V
V_{DD} to V_{C2}	−0.3V, +16V
V_{DD} to V_{C4}	−0.3V, +32V
V_{DD} to V_{SS}	−0.3V, +32V
V_{C2}, −C1, (DGND = 0V)	V_{DD}, −8V
V_{C4}, −C3, (DGND = 0V)	V_{DD}, −24V
+C1 (DGND = 0V)	−0.3V, V_{DD}
+C3 (DGND = 0V)	V_{C2}, V_{DD}
AGND to DGND	V_{SS}, V_{DD}
CLK, $\overline{INH}$, (DGND = 0V)	V_{DD}, −5V
V_{REF}	V_{DD}, V_{SS}
R_{IN}, R_{FB} (AGND = 0V)	±15V
I_{DD}	100mA dc
I_{REF} Short Circuit Duration to V_{DD}	Continuous
I_{C2} Short Circuit Duration to DGND	Continuous
I_{C4} Short Circuit Duration to DGND	Continuous
Operating Temperature Range, JN	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Package) to +50°C	450mW
Derate Above +50°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational selections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TEST CIRCUITS

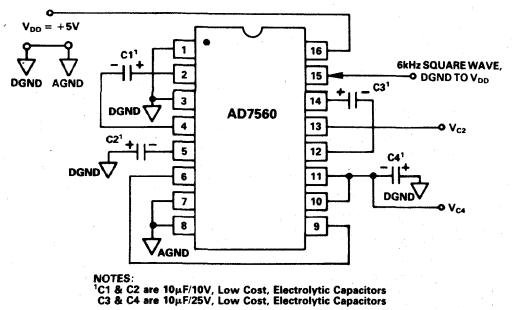


Figure 1. Test Circuit for dc-dc Converter Only, $\overline{INH}$ = 0V

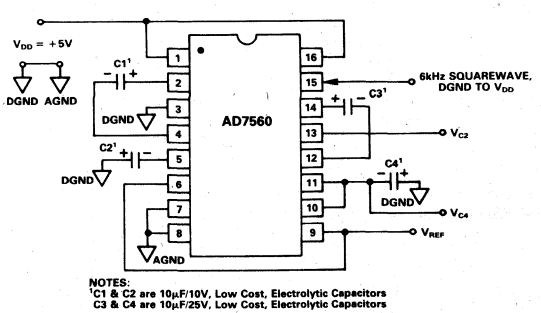


Figure 2. Test Circuit for dc/dc Converter & Voltage Reference, $\overline{INH}$ = V_{DD}

Typical Performance Characteristics

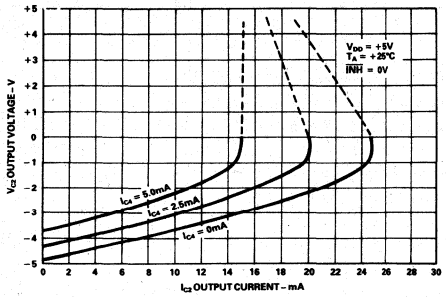


Figure 3. V_{C2} Output Voltage vs. I_{C2} Output Current for Different Values of I_{C4} (See Figure 1)

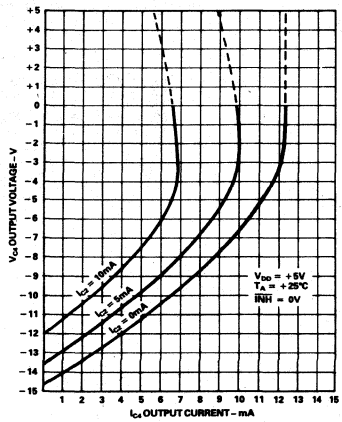


Figure 4. V_{C4} Output Voltage vs. I_{C4} Output Current for Different Values of I_{C2} (see Figure 1)

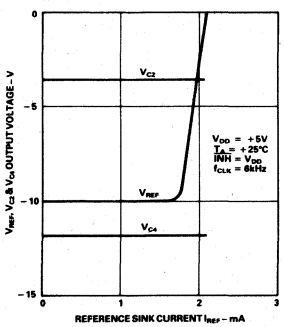


Figure 5. V_{REF}, V_{C2} and V_{C4} Output Voltage Levels vs. Reference Sink Current I_{REF} (see Figure 2)

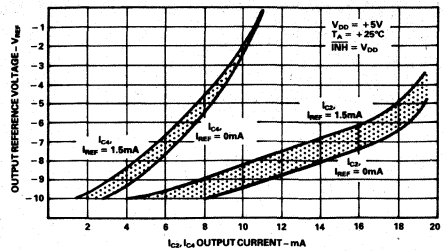


Figure 6. Output Reference Voltage V_{REF} vs. I_{C2} and I_{C4} Load Currents (see Figure 2)

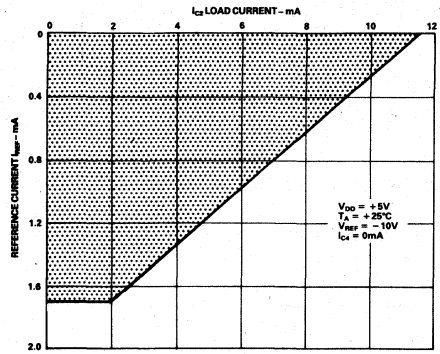


Figure 7. I_{C2} vs. I_{REF} Operating Area (Shaded) for V_{REF} = −10V (see Figure 2)

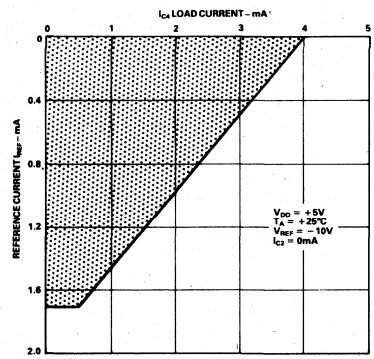


Figure 8. I_{C4} vs. I_{REF} Operating Area (Shaded) for V_{REF} = −10V (see Figure 2)

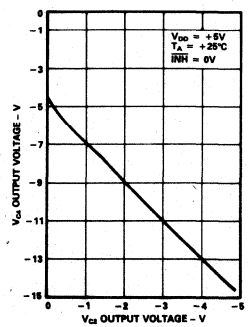


Figure 9. V_{C4} Output Voltage vs. V_{C2} Output Voltage i.e., V_{C4} Output Voltage as a Function of Current Loading on V_{C2} (see Figure 1)

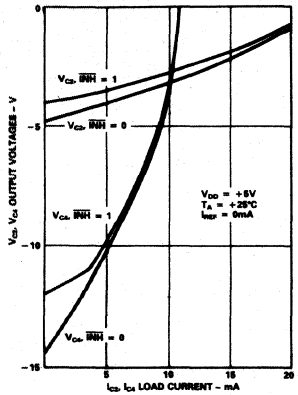


Figure 10. Effect of INHIBIT Input ($\overline{INH}$, Pin 1) on Converter Efficiency

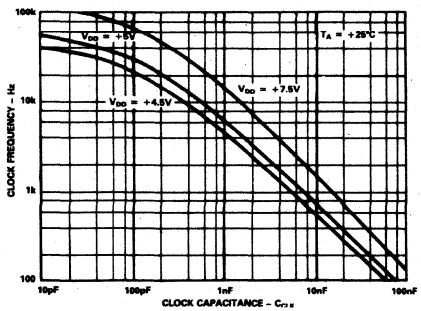


Figure 11. Typical Clock Frequency vs. Clock Capacitance

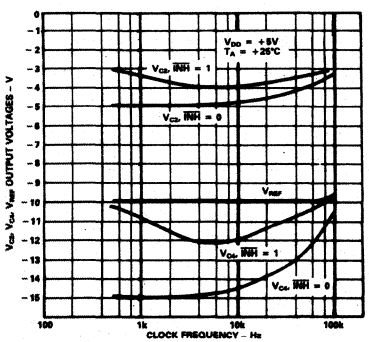


Figure 12. V_{C2}, V_{C4} and V_{REF} Output Voltages vs. Clock Frequency

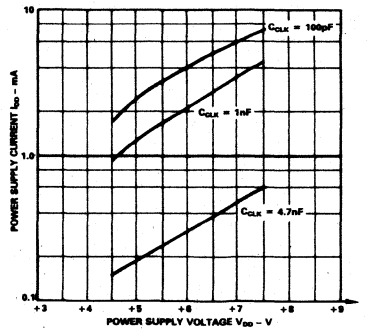


Figure 13. Power Supply Current vs. Power Supply Voltage for Different Values of C_{CLK}

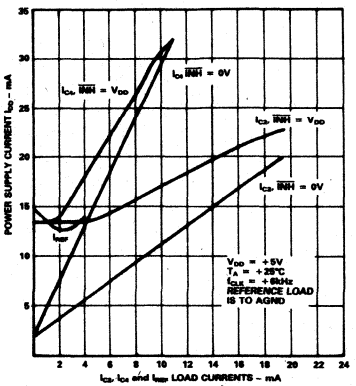


Figure 14. Power Supply Current I_{DD} vs. I_{C2}, I_{C4} and I_{REF} Load Currents

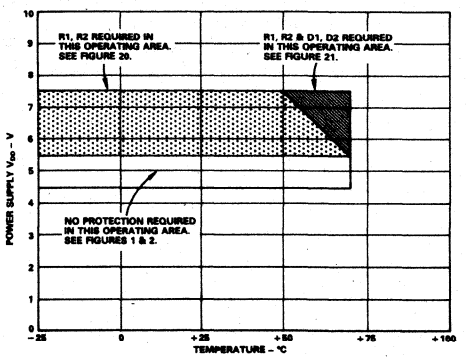


Figure 15. Operating Areas as a Function of Supply Voltage and Temperature

CIRCUIT DESCRIPTION

The AD7560 consists of two separate dc-to-dc converters which are driven in series plus a precision voltage reference with buffer amplifier. The voltage conversion circuitry of the AD7560 may best be understood by referring to Figure 16. This shows the two converters A, and B, each comprising four switches and two external capacitors.

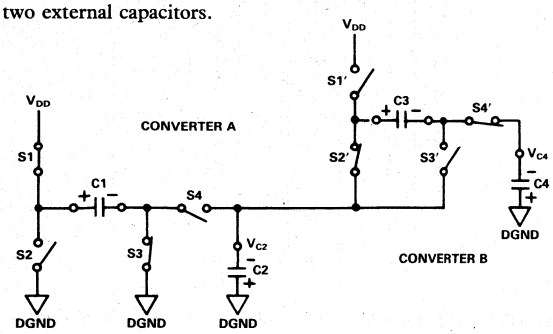


Figure 16. Converter Circuitry with External Capacitors Included

Consider initially converter A, switches S1 through S4, and capacitors C1 and C2. The oscillator and voltage-level translator sections provide the control signals to the four switches. During the charge phase, capacitor C1 is charged through S1 and S3 (S2 and S4 open) to a voltage equal to the supply voltage V_{DD}. In the pump phase, S2 and S4 are closed (S1 and S3 open) and the charge is pumped or transferred from capacitor C1 to C2. The voltage on C2 (V_{C2}, pins 5 and 13) is equal in value and opposite in polarity to $+V_{DD}$ with respect to DGND (assuming ideal switches and no load on C2). Since a finite time is required after power-on for the voltage to build up across C2 this discussion has assumed that steady state conditions have been reached.

Operation of the second converter is identical with the first except that capacitor C3 is now charged between $+V_{DD}$ and $-V_{DD}$.

This means that during the charge phase capacitor C3 will charge to $(+V_{DD}) - (-V_{DD})$ or $+2V_{DD}$. This voltage is then pumped to capacitor C4. The subsequent voltage on C4 (V_{C4}, pin 11) is ideally $3V_{DD}$ and is negative with respect to DGND. When the first converter is in the charge phase, the second is in the pump phase and vice versa. Converter timing is derived from an on-chip oscillator which can be free-running or synchronized with an externally applied clock.

Figures 3 and 4 in the Typical Performance section show output voltage vs. load current characteristics for converter A (V_{C2}) and converter B (V_{C4}) outputs respectively.

The reference portion of the AD7560 consists of an internal reference voltage circuit and an output buffer amplifier (see Figure 17). Both the reference circuit and the amplifier obtain their bias conditions from a bias controller which is powered by V_{C2} (converter A output) via an internal connection and from an externally applied negative voltage to V_{SS} (pin 10). The amplifier operating current is supplied from V_{DD} and V_{SS}. Normally the voltage output V_{C4} available on C4 (converter B output) is used as the V_{SS} supply. The reference voltage circuit, which is referenced to analog ground (AGND, pin 8), provides a stable temperature compensated $-5V$ reference voltage at the noninverting input of the buffer amplifier A1. R_{IN} and R_{FB} are two thin film resistors with nominal value of 50kΩ each. With R_{IN} (pin 7) tied to AGND and R_{FB} (pin 6) tied to the amplifier output V_{REF} (pin 9), the amplifier provides a noninverting gain of 2 for the internal reference. The amplifier thus supplies a precision reference

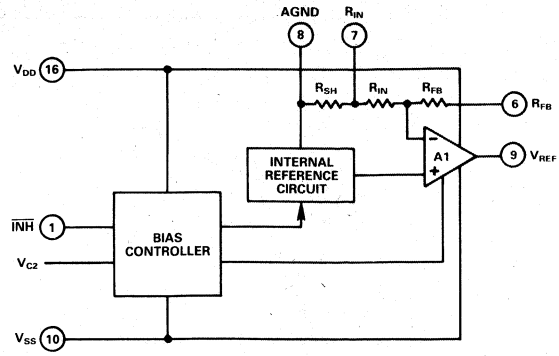


Figure 17. Reference Voltage Circuitry

voltage output of $-10V$ with a current sink capability of over 1.0mA. The R_{IN} pin is internally tied to AGND via a shunt resistor R_{SH} which is approximately equal to 1.5 R_{FB}.

The entire reference voltage circuitry can be powered down via the INHIBIT input ($\overline{INH}$, pin 1). This reduces current loading on V_{C2} and V_{C4} and results in increased conversion efficiency of both dc-to-dc converters. See Figure 10 under Typical Performance Characteristics.

TRIM TECHNIQUES

Normal lot-to-lot variations in fabrication will produce devices whose output reference voltages will be distributed symmetrically around $-10.00V$. With the addition of one fixed resistor and a potentiometer it is possible to adjust every device to provide a $-10.00V$ output (see Figure 18).

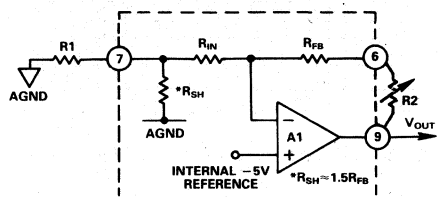


Figure 18. Trim Resistors for Reference Circuit

Trim Resistor	AD7560JN
R1 (Fixed)	10kΩ
R2 (Variable)	20kΩ

R1: thick film metal glaze, tolerance ±2%, T.C. ±100ppm/°C
R2: 20 turn cermet trimmer, tolerance ±10%, T.C. ±100ppm/°C

Table I. Recommended Trim Resistor Values

The fixed resistor R1 must be sufficiently large (when R2 = 0Ω) to ensure that the output reference voltage of any device is less than $-10.00V$. Potentiometer R2 is then increased from 0Ω until the reference voltage equals $-10.00V$. Worst case values of R1 and R2 are indicated in Table I and, therefore, represent the minimum values required which will ensure all devices can be properly trimmed.

In the absence of external gain trim components the output reference voltage is expressed as:

$$V_{REF} = -5 \times \left(1 + \frac{R_{FB}}{R_{IN}}\right) \text{Volts}$$

This reference voltage has a typical temperature coefficient (TC) of 40ppm/°C. The internal thin-film resistors R_{IN} and R_{FB} (and R_{SH}) have typical TCs of -300ppm/°C. However, their

matching and tracking is so tight as to produce no appreciable effect on the output TC.

The inclusion of external gain trim components R1 and R2 (as shown in Figure 18) modifies the overall reference performance since these external trim resistors will have different TCs from the internal thin-film resistors. The lowest values possible for R1 and R2 should be chosen in order to minimize their effect on the overall reference TC. To obtain the lowest possible reference TC the most suitable technique for reference trimming is a "select on test" approach to choosing R1 and/or R2 as opposed to potentiometer trimming.

Referring to Figure 18, if pins 6, 7 and 9 are connected together–omitting R1 and R2–amplifier A1 is configured as a unity gain buffer amplifier making the internal −5V reference available externally. However, the current loading capability of the V_{C4} output is not appreciably increased over normal −10V reference conditions.

OUTPUT VOLTAGE CALCULATION

Since the two converters (A and B), are driven in series, current loading on either of the two storage capacitors will reduce both output voltages, V_{C2} and V_{C4}, as well as the overall converter efficiency. An approximate equivalent circuit for the converter outputs is shown in Figure 19.

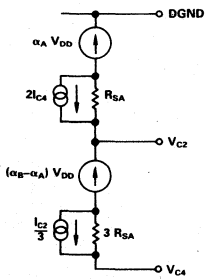


Figure 19. Equivalent Circuit for V_{C2}, V_{C4} Outputs (See Figure 1)

The output voltages using this equivalent circuit and under moderate current loads can be calculated as follows:

$$V_{C2} = -\alpha_A V_{DD} + I_{C2} R_{SA} + 2 I_{C4} R_{SA}$$

$$V_{C4} = -\alpha_B V_{DD} + 2 I_{C2} R_{SA} + 6 I_{C4} R_{SA}$$

Where: α_A is converter A conversion factor,
typically $\alpha_A = 0.95$

$$\alpha_A = \frac{|V_{C2}|}{V_{DD}}$$

α_B is converter B conversion factor,
typically $\alpha_B = 2.90$

$$\alpha_B = \frac{|V_{C4}|}{V_{DD}}$$

I_{C2} = External current load on C2

I_{C4} = External current load on C4

R_{SA} = Converter A output source resistance
$R_{SA} = 120\Omega$ typically.

If only converter B output is loaded the previous expression simplifies to:

$$V_{C4} = -\alpha_B V_{DD} + 6 I_{C4} R_{SA}$$

which is the analysis of a voltage source, $\alpha_B V_{DD}$, with an output impedance of $6R_{SA}$. Refer to the relevant current-voltage characteristics shown under Typical Performance Characteristics.

VOLTAGE CONVERSION EFFICIENCY

The efficiency of the dc-to-dc converters depends upon the switching transient losses which occur during the conversion cycles.These losses increase with increasing supply voltage V_{DD} and with increasing oscillator frequency f_{CLK}. Figure 13 shows typical power supply current I_{DD} vs. power supply voltage V_{DD} for different values of clock capacitor. The choice of values for the pump and reservoir capacitors for both converters depends primarily on the required output current loading and the peak-to-peak output voltage ripple. The AD7560 is specified with C1 = C2 = C3 = C4 = 10μF and a clock frequency of 6kHz as per the test circuit of Figure 1. The efficiency is relatively constant and optimal over a clock frequency range from 2kHz to 20kHz as indicated in Figure 12 which shows the converter output voltages as a function of clock frequency with fixed values for C1 to C4. If maximum efficiency is required at clock frequencies other than 6kHz, then the value of the pump and storage capacitors must be changed to ensure that the capacitive load impedances remain constant, i.e., if the clock frequency is reduced from 6kHz to 600Hz (a reduction of 10) then C1 to C4 values should be increased by 10 (from 10μF to 100μF). Note that the pump frequency is always one half the clock frequency at pin 15.

CLOCK FREQUENCY CONTROL

The conversion cycle time (charge and pump phases) of the dc-to-dc converters may be derived from the on-chip oscillator or else controlled by an externally applied clock signal.

1. External Clock Capacitor: When the clock input (CLK, pin 15) of the AD7560 is left open circuit, the internal oscillator runs at a typical rate of 50kHz. This frequency is lowered by connecting an external capacitor between CLK and V_{DD} or between CLK and DGND.
2. External Clock Signal: The internal oscillator can be over-ridden by an externally applied clock signal. The clock input of the AD7560 is 5V CMOS compatible and sources or sinks typically 15μA of input current. The mark/space ratio of the external clock can be highly asymmetric; minimum clock HIGH level (or LOW level) requirement is 5μs. The conversion phases change state on the negative going edge of the clock signal.

INHIBIT INPUT

As mentioned in the Circuit Description section, the reference and amplifier circuitry of the AD7560 obtains bias and operating current from the converter outputs–internally from converter A and externally (via V_{SS}) from converter B. This total current load is constant and is typically 3.5mA. Note that this 3.5mA includes any reference current that the reference amplifier sinks. In applications where the reference output voltage is not required, this current load can be reduced to negligible values by applying a logic LOW to the inhibit input ($\overline{INH}$, pin 1). The effect of the inhibit control on voltage conversion efficiency is evident from the performance characteristics as shown in Figure 10.

INTERNAL CIRCUIT PROTECTION

Referring to Figure 16, the MOS switches of both converters, S3, S4 and S3′, S4′ are N-channel devices. During normal

charge and pump cycles and also during power-up and output short circuit conditions (see following section), the voltages on the sources and drains of these output transistors vary in amplitude and polarity. To ensure optimum transistor performance (i.e., low R_{ON} and substrate reverse biased with respect to source) under any condition, their substrates must be tied to the most suitable negative potential available. To achieve this, a section of the internal control logic is devoted to sensing the voltages on the transistor sources and drains, and ensuring that their substrates are always correctly biased. This technique prevents the AD7560 from latching up during power-up and overload conditions, and also ensures optimum efficiency of both dc-to-dc converters.

OPERATION AT HIGH VOLTAGES AND ELEVATED TEMPERATURES

Under normal specified conditions, the AD7560 operates efficiently over its full temperature and supply voltage ranges. If any one of the external capacitors short circuits or if the V_{C2} or V_{C4} output is shorted to any low impedance point (e.g., V_{DD} or DGND) the AD7560 internal protection circuitry mentioned previously acts to prevent SCR action and to avoid device destruction. If the AD7560 is to operate under a combination of temperature/supply voltage conditions, as shown in the shaded areas of Figure 15, then external protection circuitry is required both to ensure device operation and, in the event of a short circuit occurring, to preclude device destruction.

Figure 20 shows the protection circuitry required when operating in the dotted area of Figure 15. Due to the inclusion of R1 in series with the V_{C2} output on pin 5, the V_{C2} output on pin 13 should not be used.

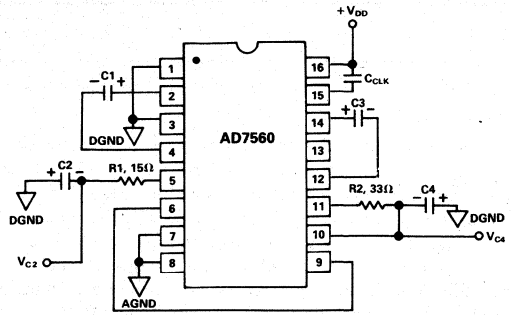


Figure 20. Location of Protection Components R1, R2 Required for Operation in Shaded Area of Figure 15

Figure 21 shows the protection circuitry required when operating in the lined area of Figure 15. Under these conditions of high temperature/high voltage, if the V_{C2} or V_{C4} output is shorted to V_{DD}, then internal parasitic transistors may be turned on leading to SCR action and possible device destruction. Diodes D1 and D2 ensure that the V_{C2} and V_{C4} outputs are never pulled higher than a diode drop above DGND. Note that these diodes will require current limiting protection via the R_{LIMIT} series resistors.

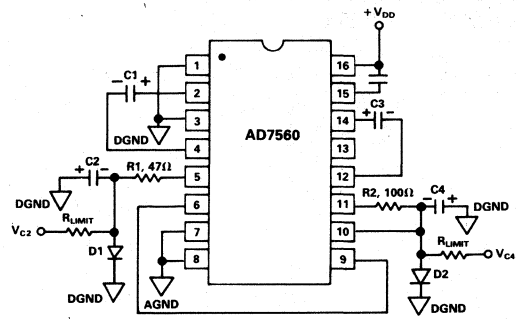


Figure 21. Location of Protection Components R1, R2 and D1, D2 Required for Operation in Lined area of Figure 15

Note that none of the above external protection is required when operating the AD7560 within specified limits of $+4.5 \leq V_{DD} \leq +5.5V$ at any temperature over its $-25°C$ to $+70°C$ range.

The AD7560 can be used in a multitude of configurations to suit different requirements and applications. Table II outlines some of these operating configurations.

Figure	Input Voltage	Nominal Output Voltages
22	+5V	−5V
23	+5V	−5V, −15V
24	+5V	−5V, −15V, −10V Reference
25	+5V	−5V, +10V
26	+5V	−5V, +15V
27	+5V	−5V, −15V, +10V
28	+5V	−5V, −15V, +15V
29	+5V	−5V, −15V, +10V, −10V Reference
30	+5V	−5V, −15V, +15V, −10V Reference

Table II. Typical AD7560 Operating Configurations

+V_{DD} In, −V_{DD} Out (Figure 22)
Figure 22 shows the circuitry required for single voltage conversion. C1 and C2 are standard 10μF/10V electrolytic capacitors. See Figure 3 for typical performance characteristics.

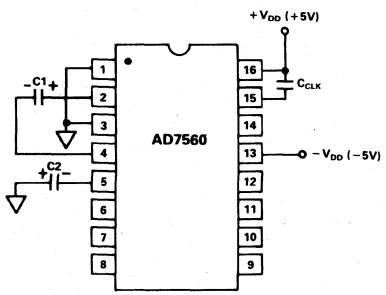


Figure 22. +V_{DD} to −V_{DD}

+V_{DD} In, −V_{DD}, and −3V_{DD} Out (Figure 23)
Figure 23 shows the circuitry required for voltage conversion and negative voltage multiplication. Capacitors C1 and C2 are 10μF/10V, capacitors C3 and C4 are 10μF/25V. All are standard low cost electrolytic types. Typical performance characteristics are shown in Figure 4.

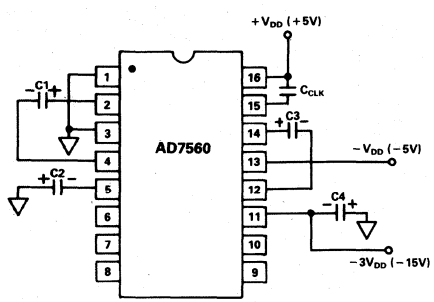


Figure 23. +V_{DD} to −V_{DD} and −3V_{DD}

+V_{DD} In, −V_{DD}, −3V_{DD} and −10V Reference Out (Figure 24)
To allow the voltage reference circuit to operate, the inhibit input ($\overline{INH}$, pin 1) is tied to V_{DD}. The feedback loop of the internal buffer amplifier is closed by tying R_{FB} (pin 6) to V_{REF} (pin 9). The amplifier input resistance R_{IN} (pin 7) is tied to AGND (pin 8) to provide a gain of +2 for the internal −5V reference (see Figure 24).

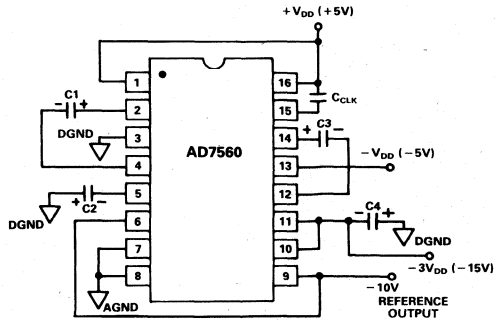


Figure 24. +V_{DD} to −V_{DD}, −3V_{DD} and −10V Reference Output

+V_{DD} In, −V_{DD}, +2V_{DD} Out (Figure 25)
Positive voltage multiplication is possible using a diode pump scheme as shown in Figure 25. In this configuration, the input capacitor (C5) of the diode pump is switched between +V_{DD} and DGND by the action of converter A. During its pump phase (pin 2 at AGND) C5 is charged to +V_{DD} −V_F (where V_F is the forward diode drop of D1.) During the charge phase (pin 2 at +V_{DD}) the voltage on C5 plus the supply voltage is applied through D2 to capacitor C6. Thus the output voltage on C6 is +2V_{DD} −2V_F.

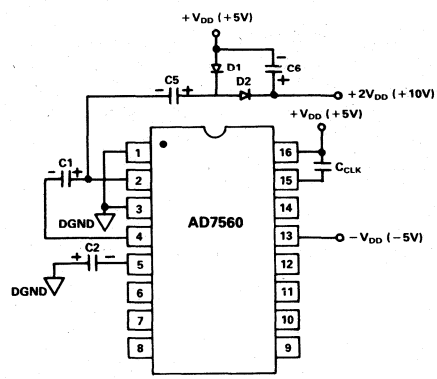


Figure 25. +V_{DD} to −V_{DD} and +2V_{DD}

+V_{DD} In, −V_{DD}, +3V_{DD} Out (Figure 26)
In this configuration, multiplication of +V_{DD} to +3V_{DD} is achieved by switching the input of the diode pump capacitor (C5) between +V_{DD} and V_{C2}. During the pump phase of converter B capacitor C5 is charged to +V_{DD} + V_{C2} − V_F (where V_F is the forward diode drop of D1). During the charge phase the voltage on C5 plus the supply voltage is applied through diode D2 to capacitor C6. The output voltage on C6 is thus 2V_{DD} + V_{C2} −2V_F. Capacitors C5 and C6 are 10μF/25V.

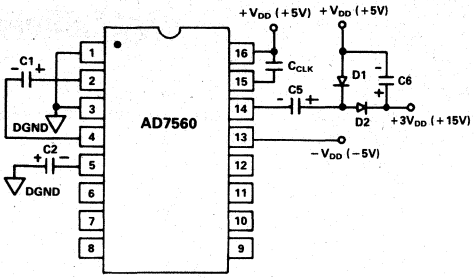


Figure 26. $+V_{DD}$ to $-V_{DD}$ and $+3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ Out (Figure 27)
This configuration uses both converters and a diode pump. Driving the diode pump input capacitor from +C1 (pin 2) provides positive voltage doubling as explained in conjunction with Figure 25.

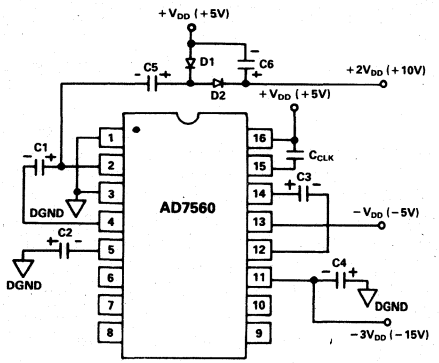


Figure 27. $+V_{DD}$ to $-V_{DD}$, $+3V_{DD}$ and $+2V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ Out (Figure 28)
This circuit is similar to Figure 27 except that the diode pump is now driven from +C3 (pin 14). This provides voltage trebling as explained in conjunction with Figure 26.

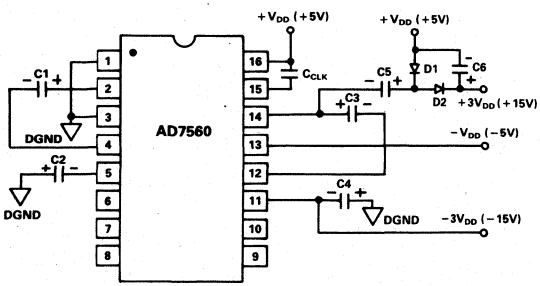


Figure 28. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+2V_{DD}$ and $-10V$ Reference Out (Figure 29)
The configuration shown in Figure 29 uses both converters, reference circuit and diode pump to provide multiple analog outputs.

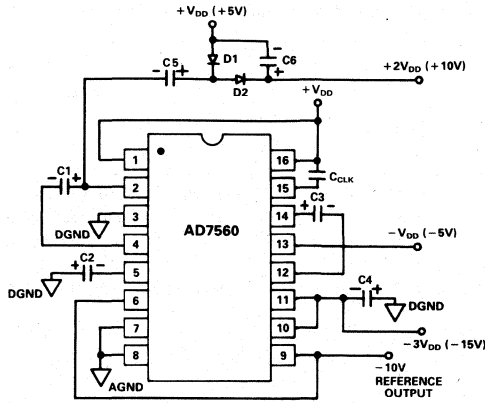


Figure 29. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ and $-10V$ Reference Output

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+3V_{DD}$ and $-10V$ Reference Out (Figure 30)
This circuit is similar to Figure 29 except that the diode pump is now driven from +C3 (pin 14) to provide positive voltage trebling (see Figure 30).

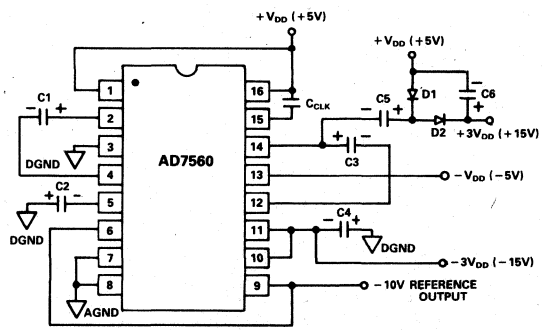


Figure 30. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ and $-10V$ Reference Output

INCREASING OUTPUT CURRENT CAPABILITY

It is possible to run two or more AD7560s in parallel to reduce the output resistance of both V_{C2} and V_{C4}. Figure 31 shows the circuit connections. Each converter has its own pump capacitor while the respective storage capacitors are common. The resultant output resistance of either converter A or converter B is approximately equal to that of a single device divided by the number of devices paralleled.

Each AD7560 in Figure 31 is shown with an individual clock capacitor. Thus each device runs independently at a different conversion frequency leading to increased noise in the reference voltage output. To reduce the generated noise to a minimum drive all CLK inputs in parallel from a common clock signal.

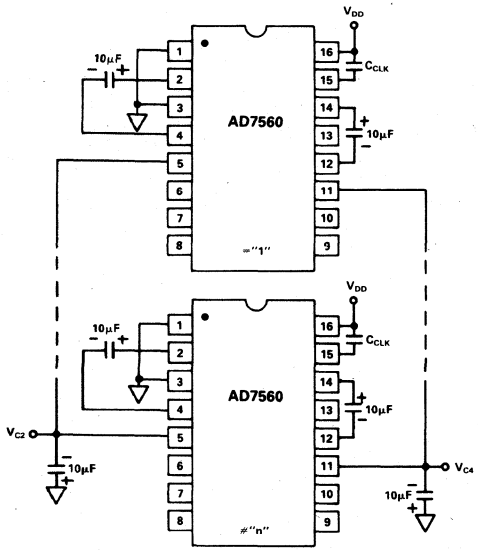


Figure 31. Paralleling Devices to Increase Output Current Capability

The reference voltage output can also benefit from the paralleling of devices. Figure 32 shows how the final AD7560 (e.g., device ≠ "n" in Figure 31) should be connected to boost the available reference current. For example, with two devices in parallel the typical reference current is increased to over 5mA.

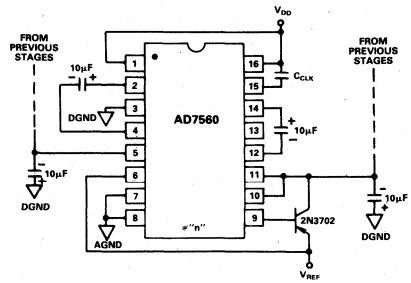


Figure 32. Reference Current Boosting

Note that this reference current boosting technique may also be used with existing −12V to −15V power supplies. Using the single general purpose PNP transistor as indicated in Figure 32 and an existing −12V power supply, one AD7560 can control up to 200mA of reference current (see Figure 33).

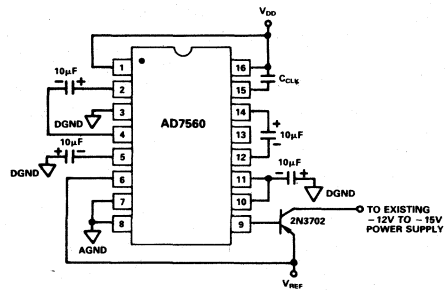


Figure 33. Reference Current Boosting Using Existing −12V to −15V Power Supply